

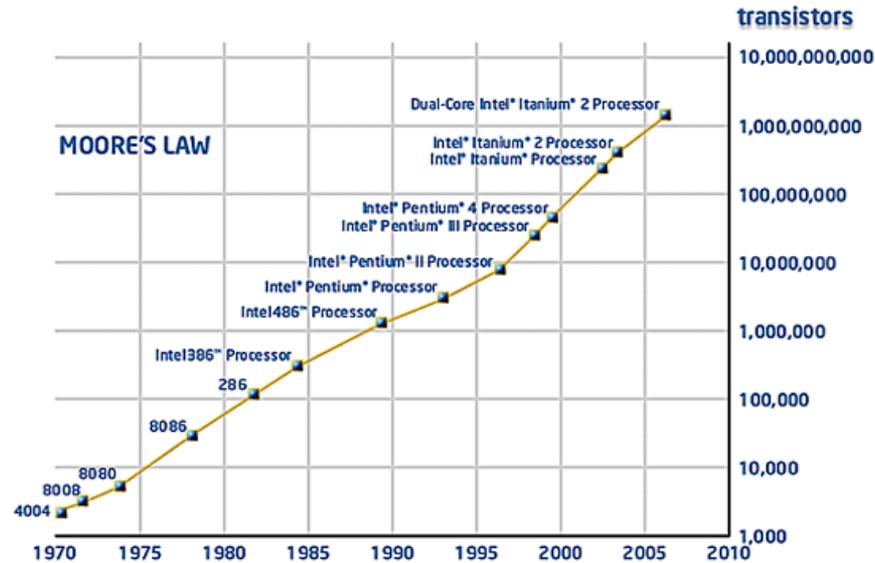
VERIFICATION OF COMPLEX MIXED SIGNAL ASICS

System-Verilog and UVM mini workshop 14th November 2013

T. Hemperek

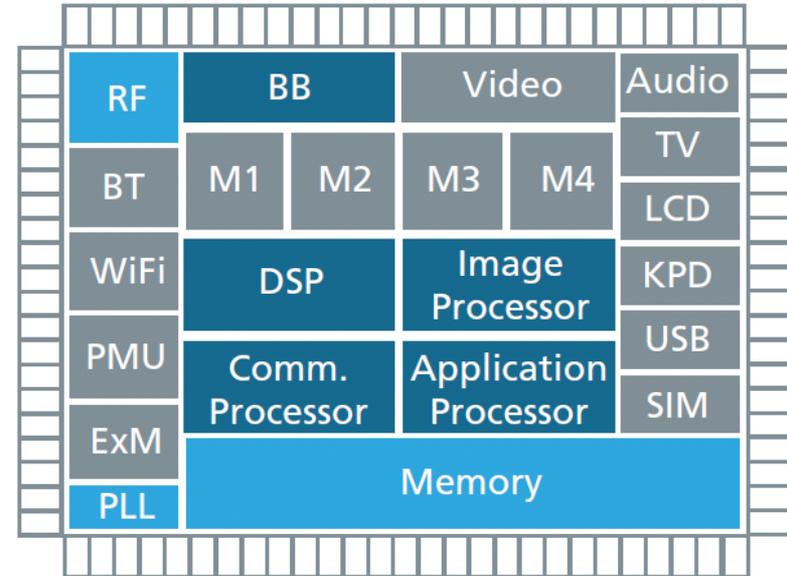
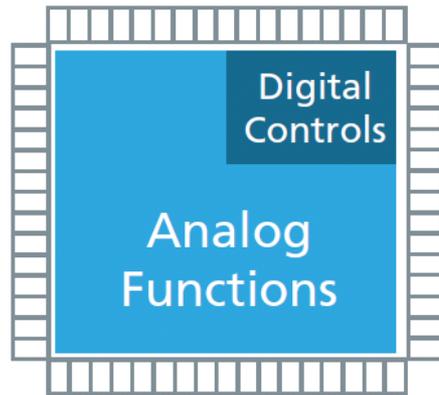


Moore's law in HEP



Name	D-OMEGA Ion	LHC1	FE-I3	FE-I4	FE-I5
Year	1991	~1996	~2005	~2011	???
Technology Node	3 μm	1 μm	0.25 μm	0.13 μm	65 nm??
Chip size	8.3x6.6 mm^2	8x6.35 mm^2	10.8x7.6 mm^2	10.2x19 mm^2	???
Pixel size	75x500 μm^2	50x500 μm^2	50x400 μm^2	50x250 μm^2	25x125 μm^2 ??
Pixel array	16x63	16x127	18x160	80x336	???
Transistor count	???	800k	3.5M	80M	1G?

Switch to big “D”, little “A”



Traditional Mixed-signal Design
Physical hierarchy separates
digital and analog

Modern Mixed-signal Design
Digital and analog distributed
throughout design

Same pattern for HEP

Verification

- **Verification plan**
- **Simulation**
- **Assertion based verification**
- **Formal verification**
- **Mixed signal verification**
- **FE-I4**

Verification Plan

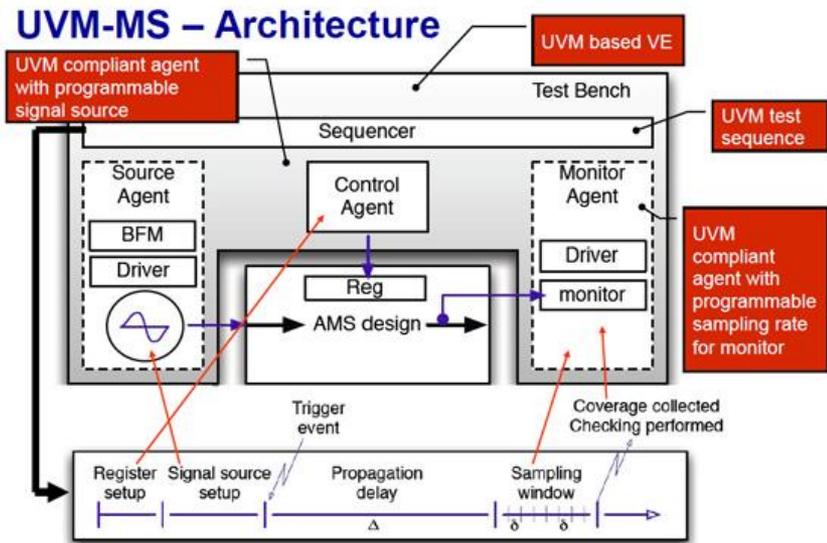
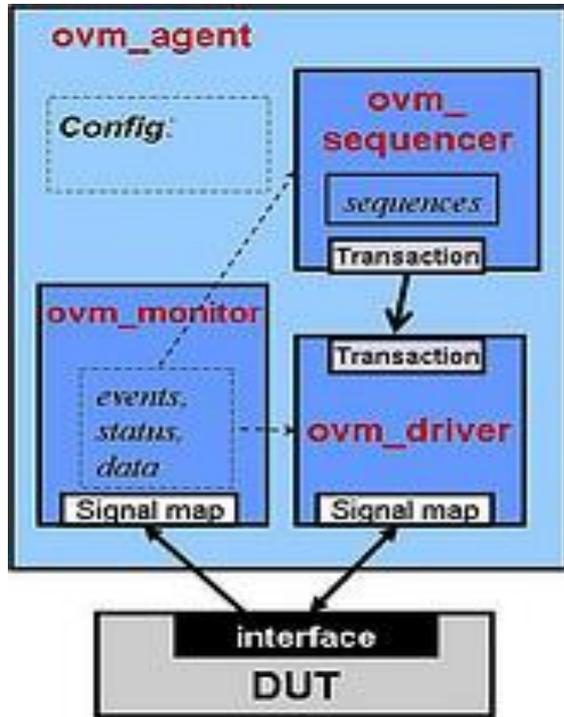
The image shows a side-by-side comparison between a Microsoft Word document titled 'DMA_ETH2.xml' and the vPlan tool interface. Red arrows indicate the mapping between the document's sections and the tool's hierarchy:

- Document Section 1.1 Functional Interfaces** maps to the **3.1 Complete DMA_ETH Block** folder in vPlan.
- Document Section 1.1.1 Ethernet Ports** maps to the **3.1.1 Ethernet Ports** folder.
- Document Section 1.1.2 AMBA AHB Bus** maps to the **3.1.2 AMBA AHB Bus** folder.
- Document Section 1.2.1 DMA Controller** maps to the **3.2 Core Features** folder.
- Document Section 2.1 Code Coverage** maps to the **3.3 Code Coverage** folder.

The vPlan tool interface shows a hierarchical tree with progress bars for each folder:

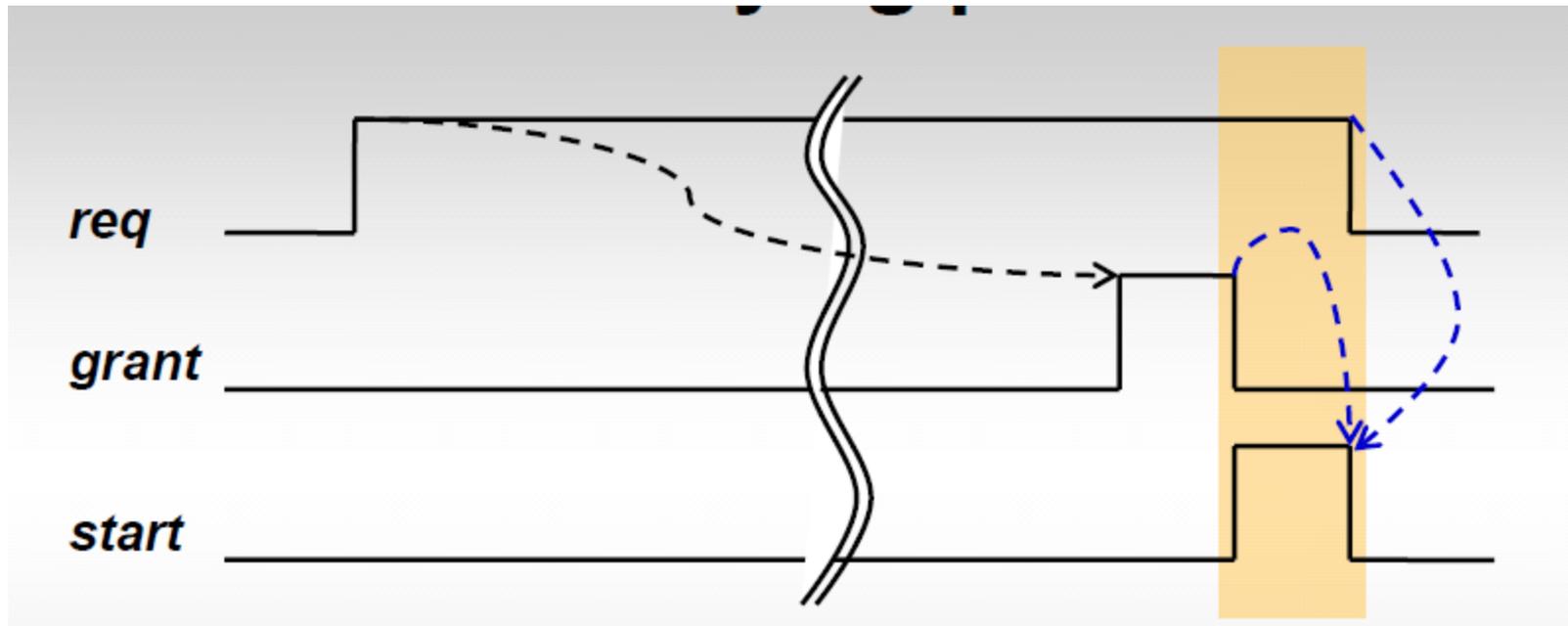
- 3 Complete DMA_ETH Block (51%)
 - 3.1 Functional Interfaces (33%)
 - 3.1.1 Ethernet Ports (6%)
 - 3.1.1.1 Ethernet Frame Format (11%)
 - 3.1.1.2 MII Signaling (4%)
 - 3.1.2 AMBA AHB Bus (59%)
 - 3.1.2.1 AMBA AHB Slave Interface (36%)
 - 3.1.2.2 AMBA AHB Master Interface (99%)
 - 3.1.2.3 AMBA AHB Master2 Interface (0%)
 - 3.2 Core Features (36%)
 - 3.3 Code Coverage (84%)
 - icc_coverage.*.block (87%)

Simulation – Unified Verification Methodology



Assertions based verification

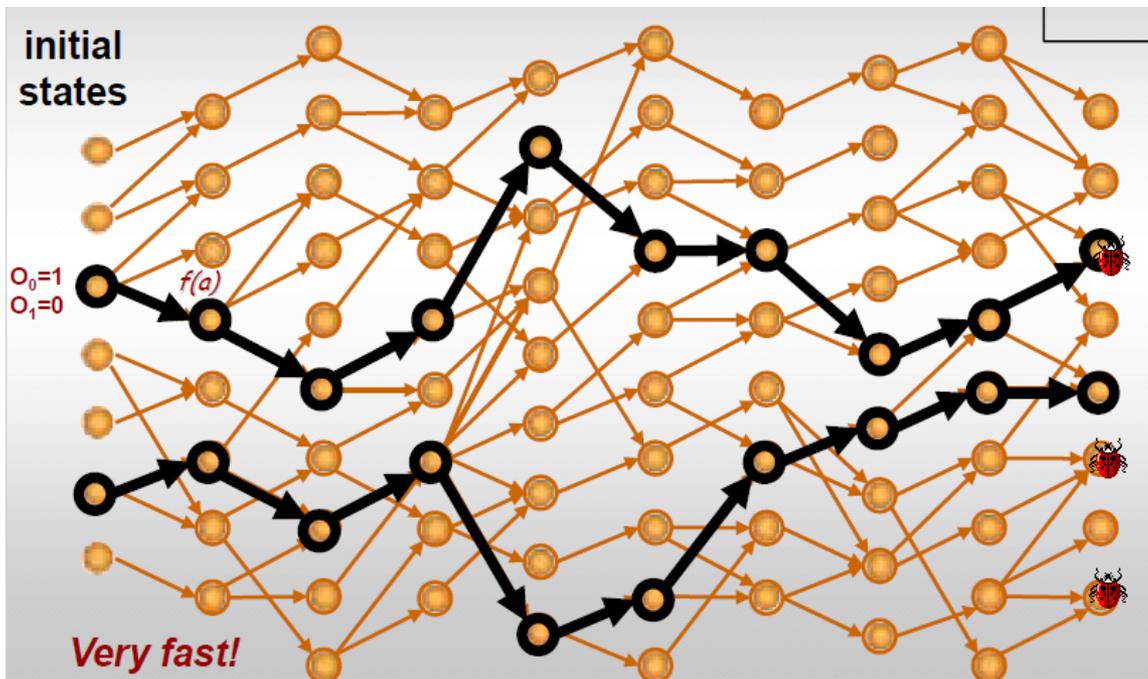
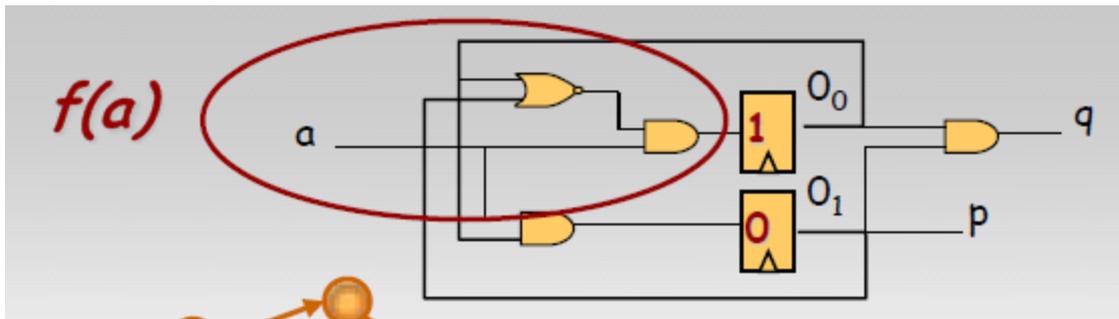
A pattern describes a proven solution to a recurring design problem



// A start can only occur after a grant for an active request
assert

```
property (@(posedge clk) disable iff (~rst_n) req[*1:8] ##0 grant ##1 req | -> start);
```

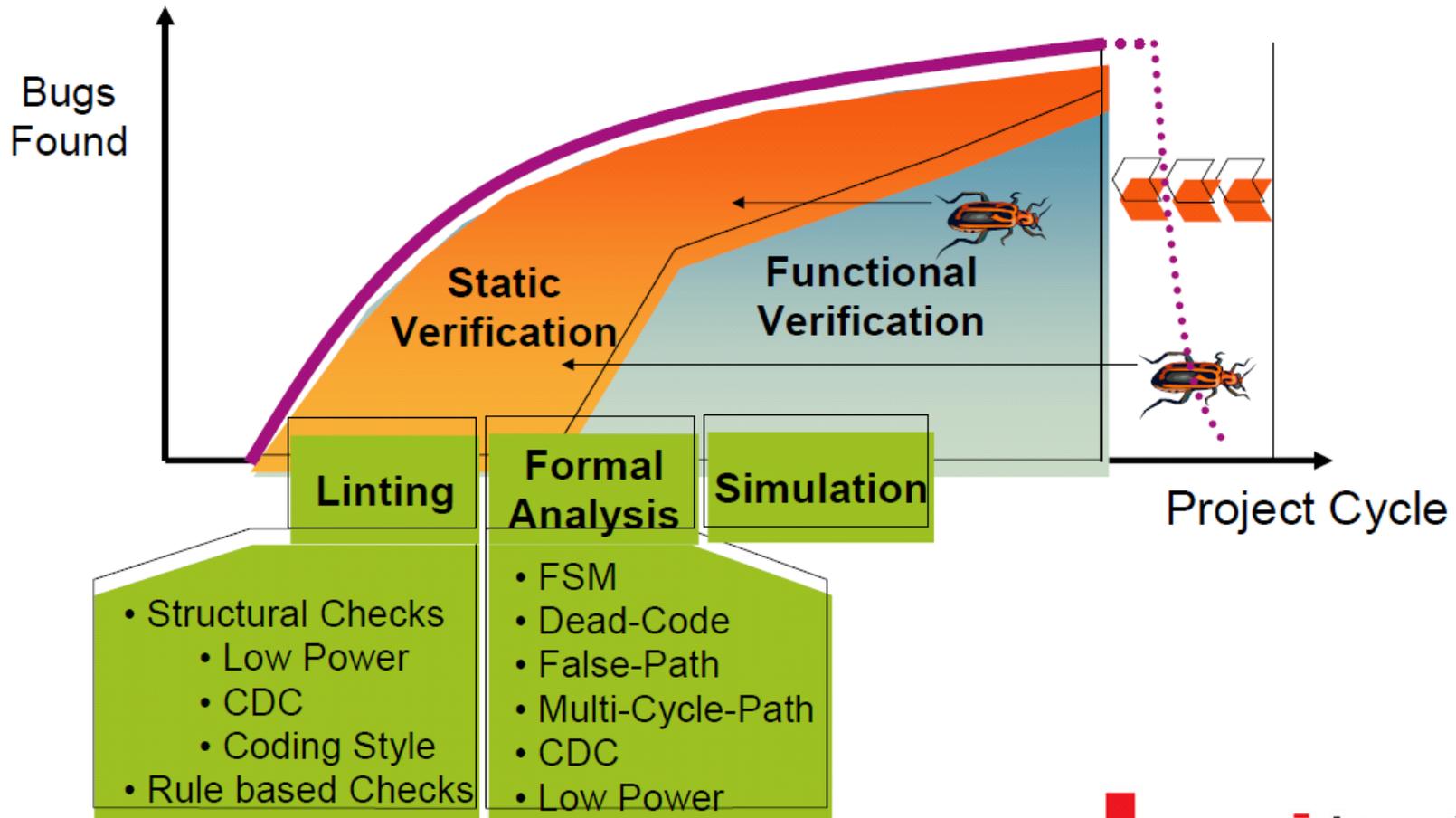
Formal verification



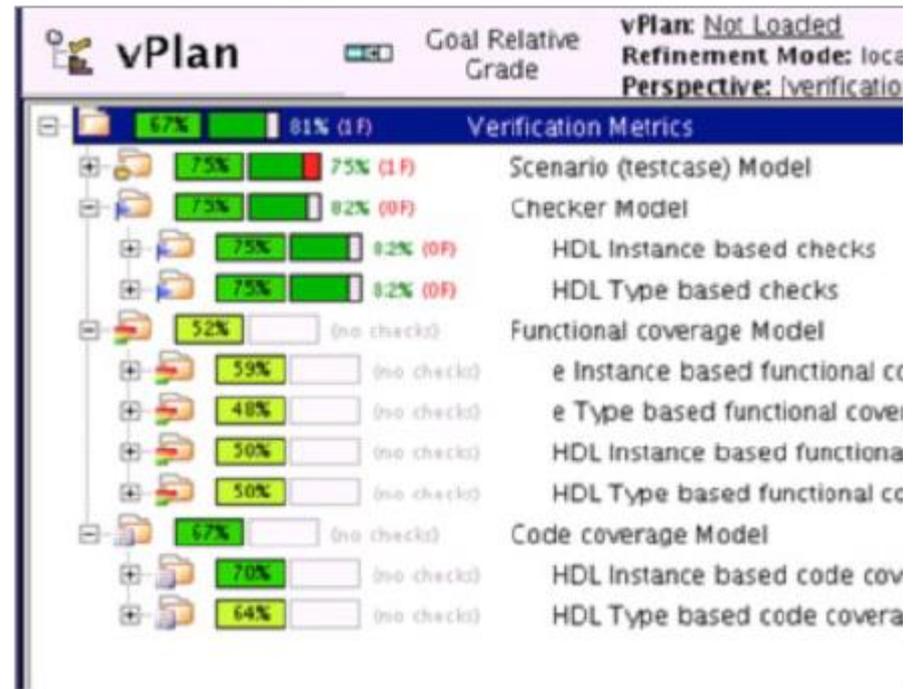
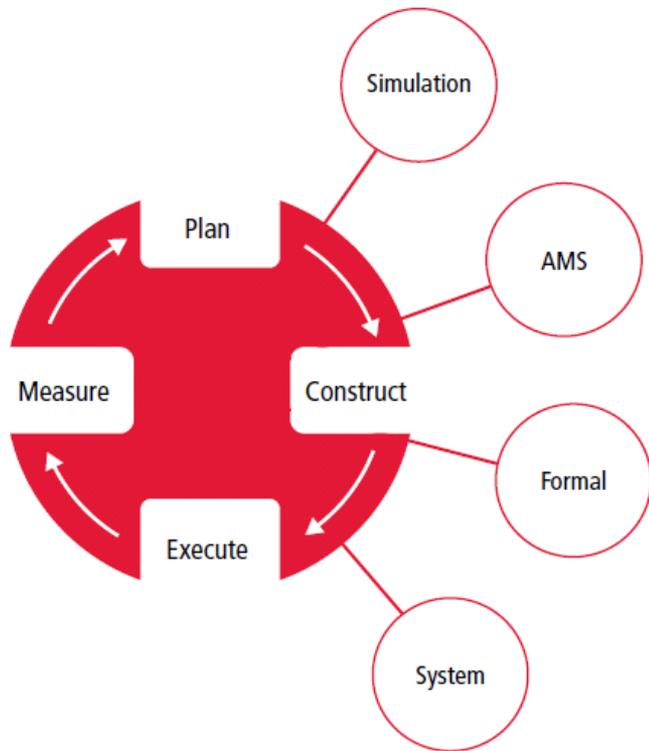
// SystemVerilog Assertion

```
property p_arb;  
  @(posedge clk)  
    req | => ##[0:2] gnt;  
endproperty  
assert property (p_arb);
```

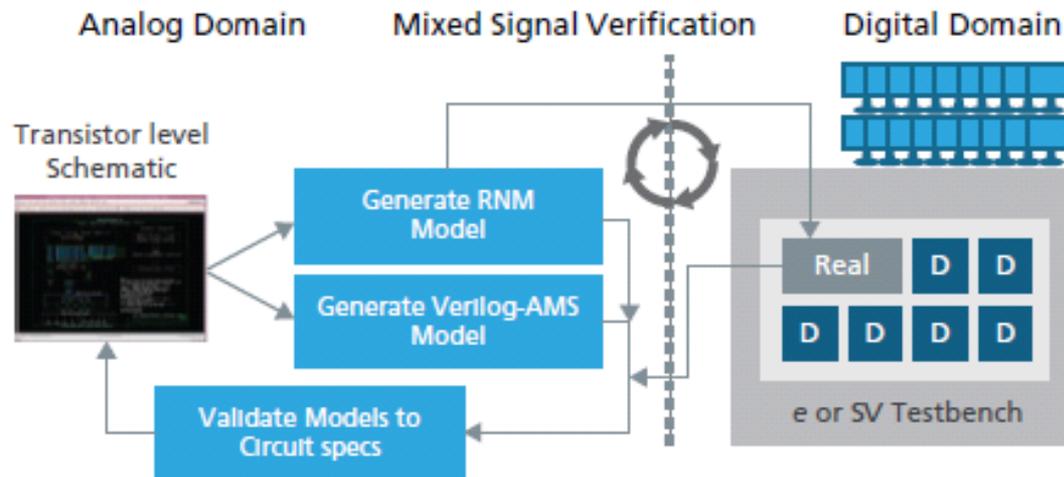
Static verification checking and simulation



Metric Driven Verification

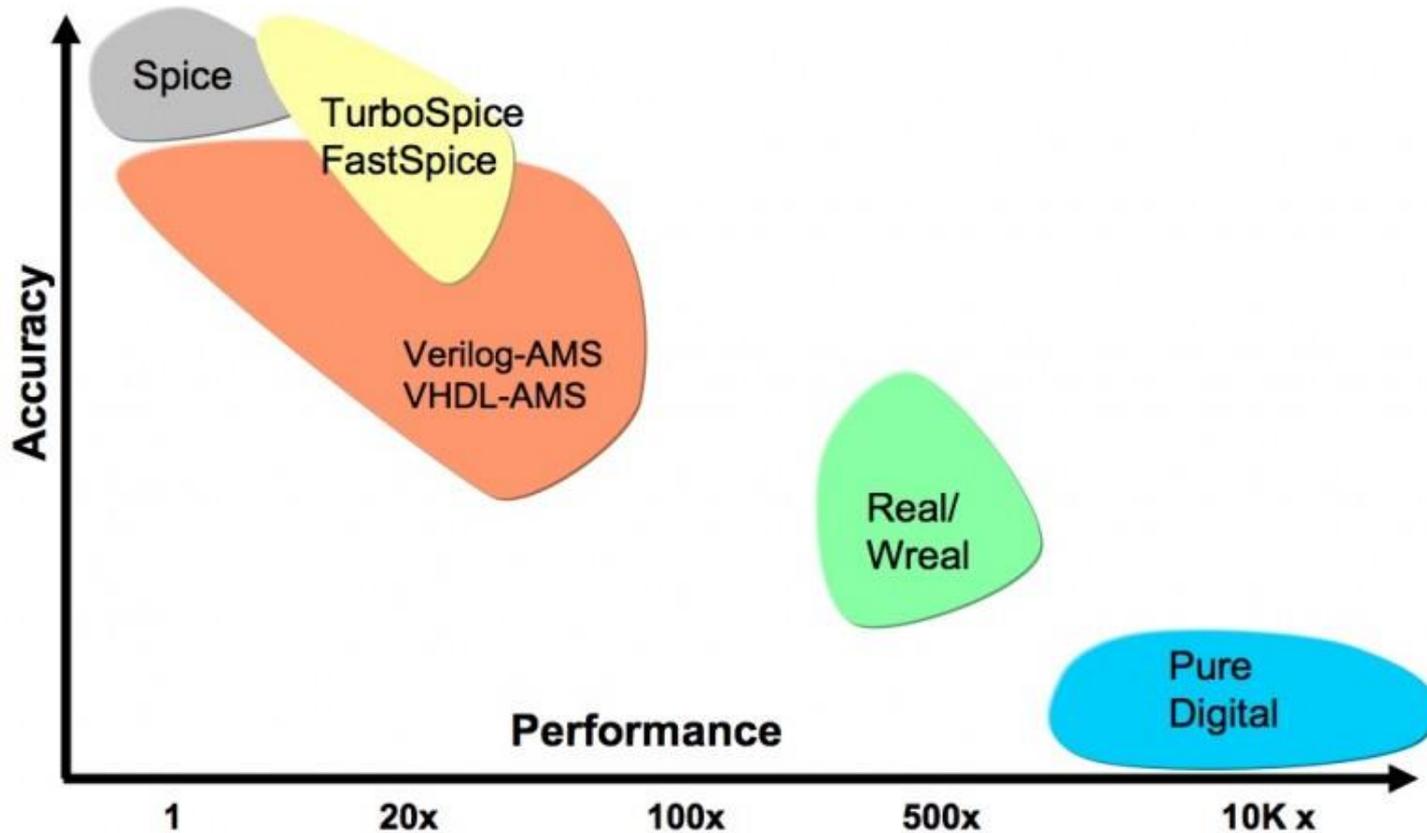


MS Verification



- High performance, real number modeling for mixed signal verification
- Models are easily ported between Virtuoso and Incisive environments
- Run full-chip verification regression suites at digital speeds
- ▶ **Benefits:** Increased Predictability, Productivity and Quality (PPQ)

Accuracy versus performance



Source: Cadence Design Systems

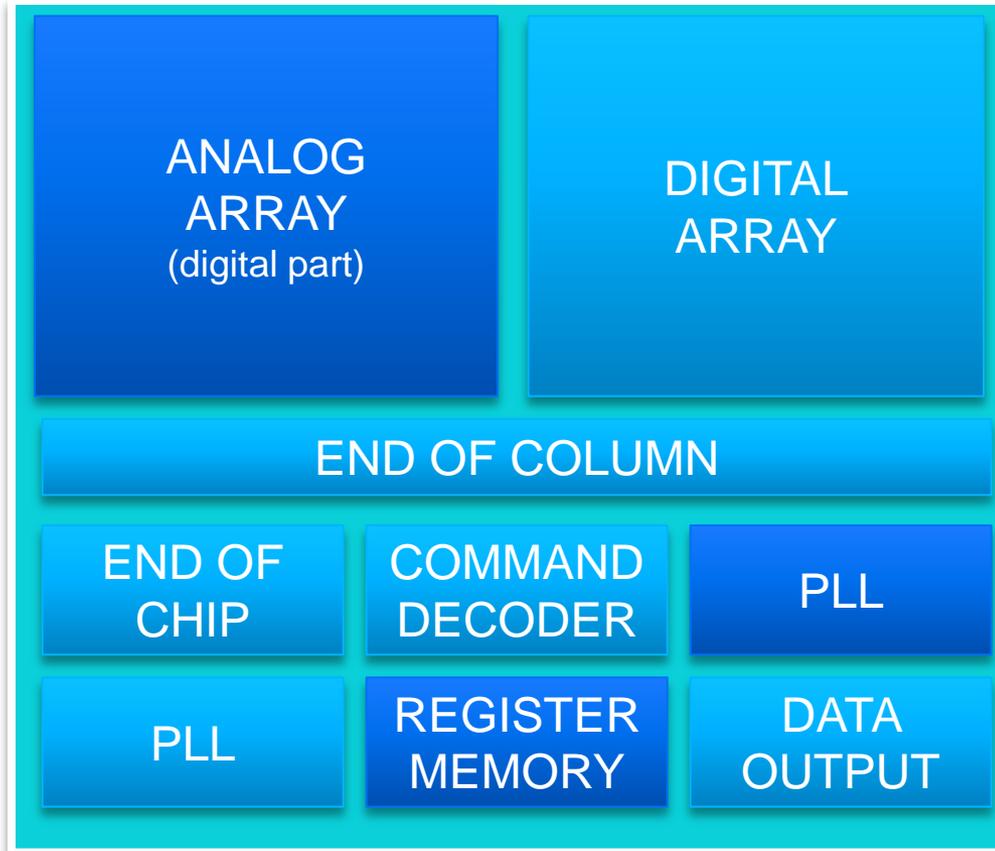
Modeling feature chart

	Feature	Verilog	VHDL	Verilog-AMS (wreal)	SV (2009)	SV (2012)
Modeling	1 Real value variables	✓	✓	✓	✓	✓
	2 Real valued Signals/nets declarations	✗	✓	✓	✗	✓
	3 User Defined Types with reals (multi-field records with reals)	✗	✓	✗	✗	✓
	4 Resolution functions for multiple real signal drivers	✗	User-Defined	6 Built-in functions	✗	User-Defined
Interaction	5 Ability to convert an interconnect to real/logic based on the hierarchical connectivity	✗	✓ Not as flexible as Wreals	Wreal coercion (incl. electrical)	✗	Generic Interconnect
	6 Ability to connect Real-to-Logic and automatic conversion of values	✗	✗	✓	Limited	✓
	7 Interact with electrical signals (Automatic Connect Module)	✗	✗	✓	✗	✗
	8 Testbenches with mixed signal content	✗	✗	✗	✗	✓

✓ Standardized & implemented
 ✓ Cadence solution

✓ On the standardization roadmap; not yet implemented
 ✗ Not in the standards/roadmap; not implemented

FE-I4 Top View

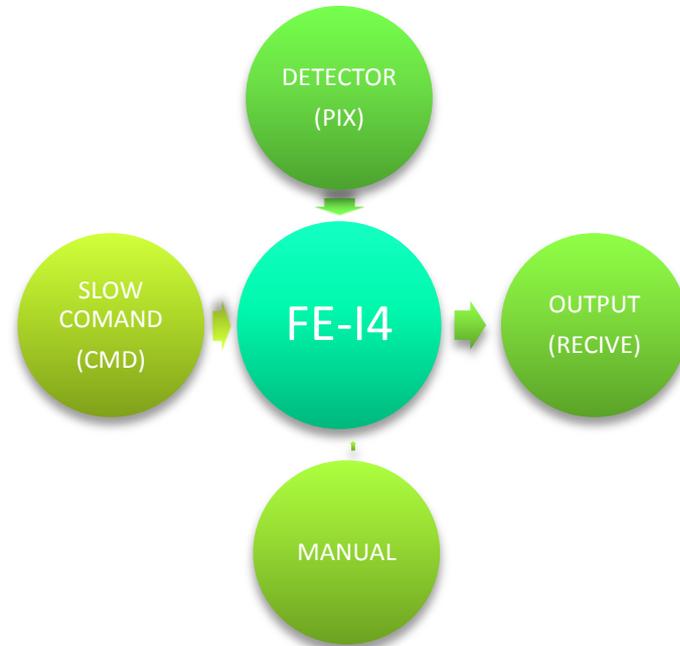
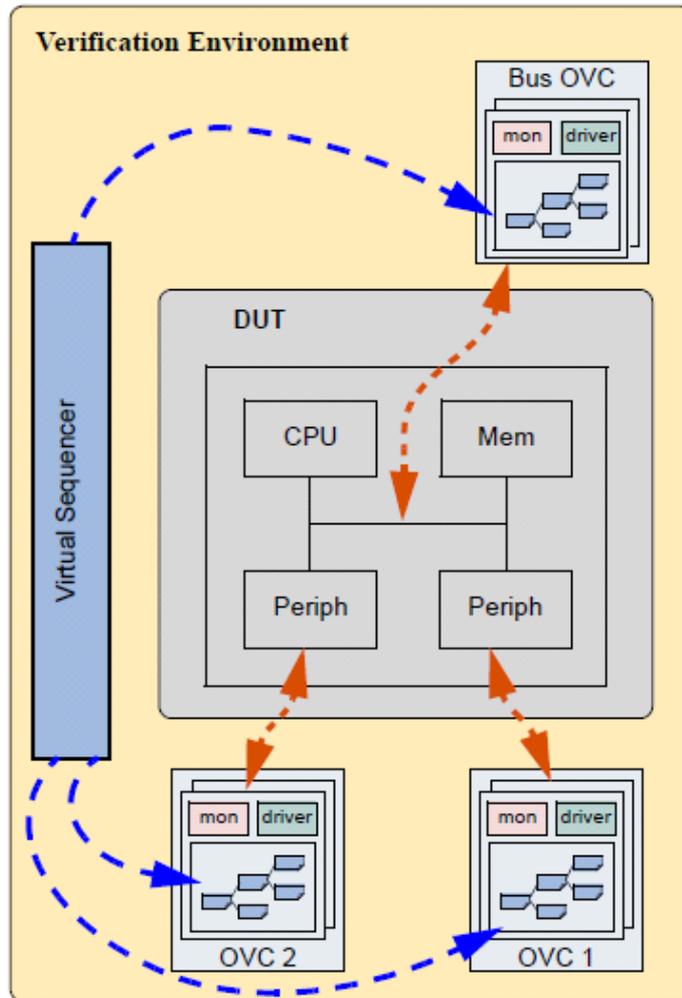


- verilog model



- Implementation (rtl/gate)

FE-I4 Verification environment

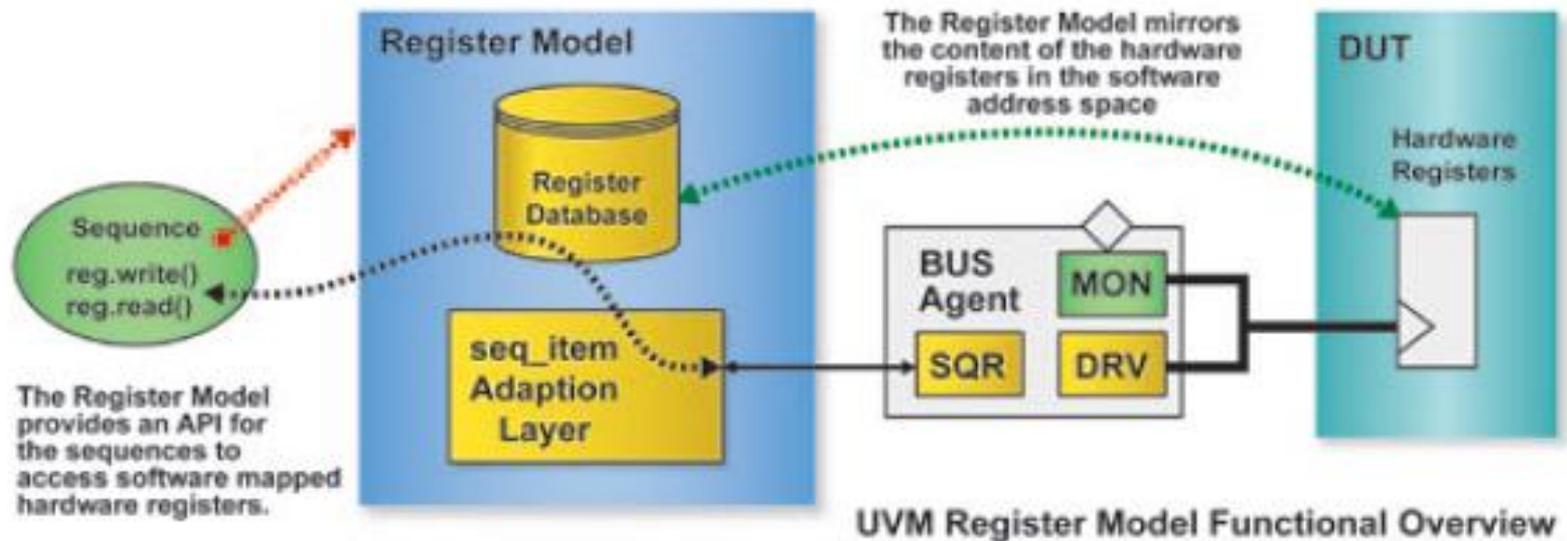


For FE-I4 we have 4 OVC:

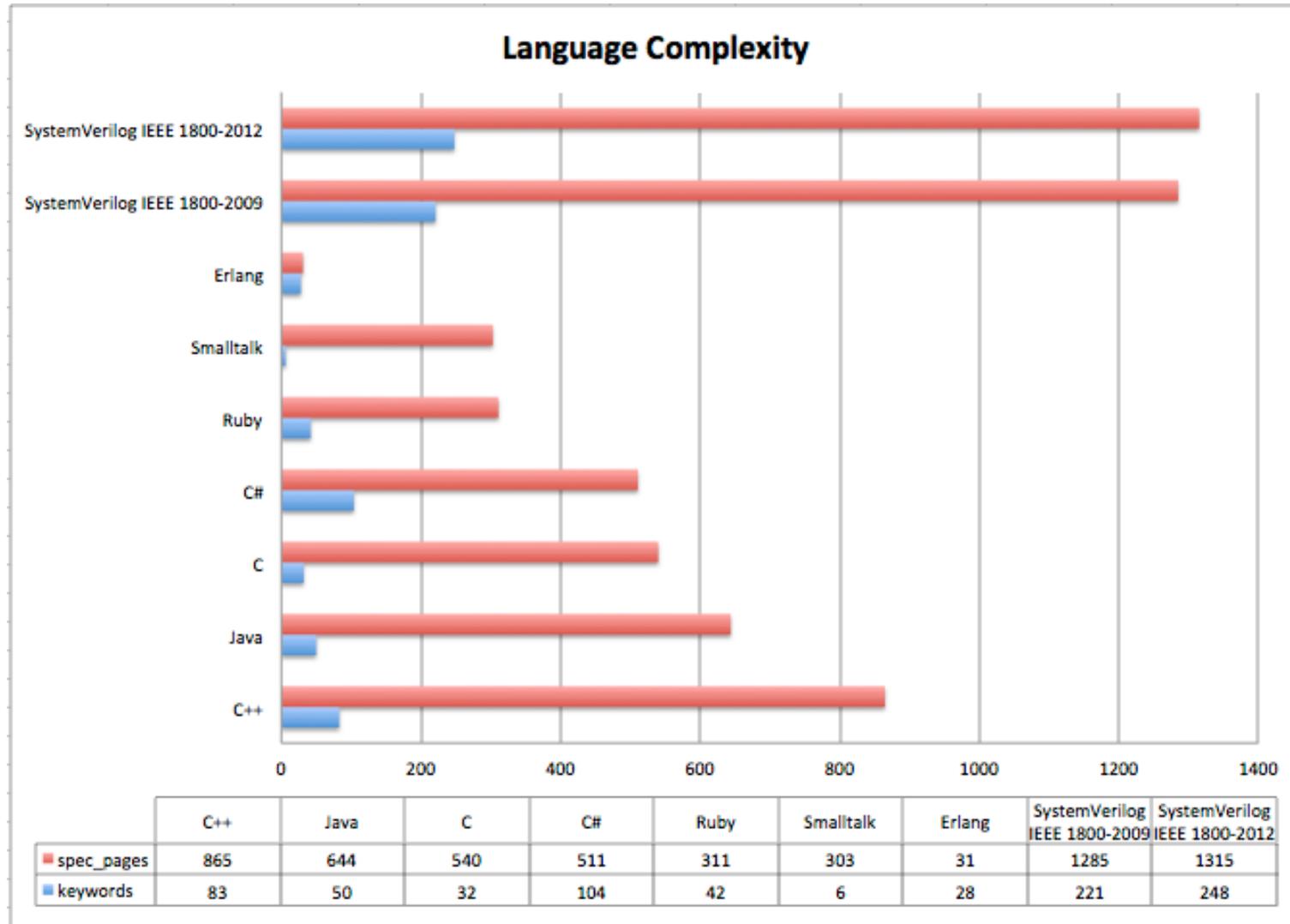
- PIX
- CMD
- REVEIVE
- MANUAL

Questions?

UVM register model



System Verilog



A UVM layer for PyHVL

<http://www.fivecomputers.com/a-uvm-layer-for-pyhvl.html>