SiW ECAL plans for 2 years

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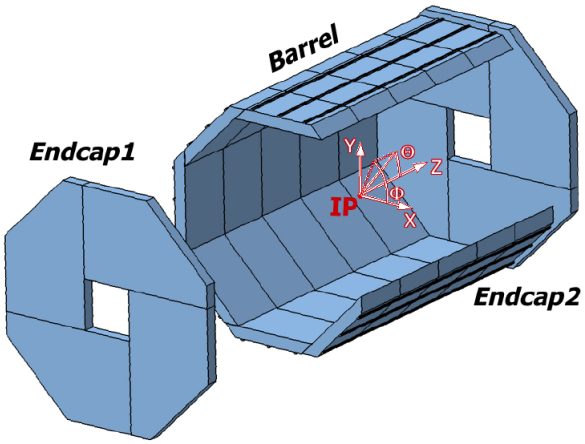
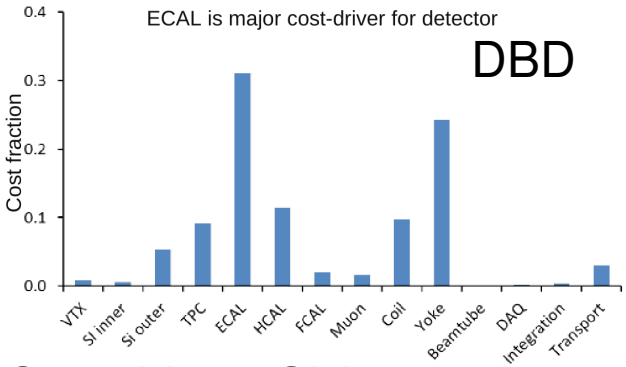
Optimization studies



Hamamatsu HPK offer in spring'2013: 2.5 EUR/cm^2 silicon sensors (if they make all sensors), as in DBD cost estimation.

ECAL inner radius = 1.843 m - can possibly be reduced to 1.4-1.5 m (see talk of H.Tran). Big impact on full ILD cost.

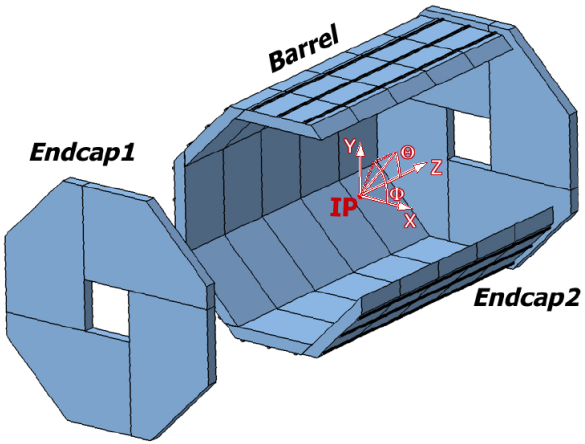
30 layers may be reduced to 25 or 20

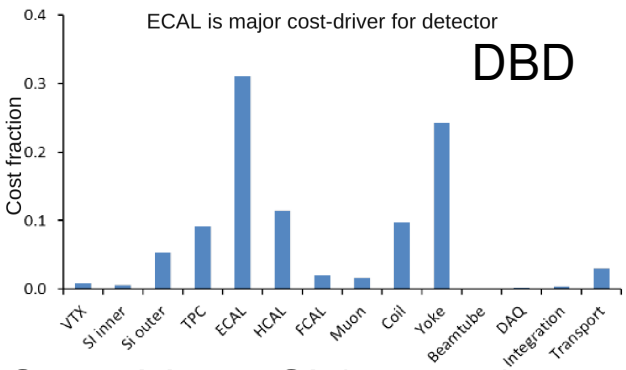


Cost driver: Si ($\sim$ 50%)

- Define new ECAL model with reduced R_{ECAL}, N layers.
- New ECAL model should include realistic ECAL parameters: fraction of dead pixels/chips, realistic PCB and silicon thickness, noise level. Study how ECAL performance depends on parameter variations around "working point". Compare silicon and scintillator options.

Optimization studies (cont.)





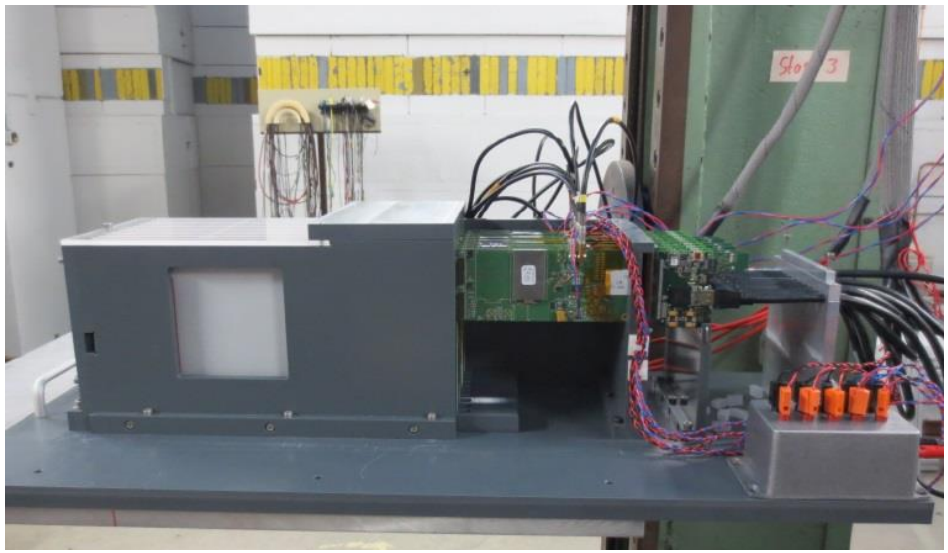
Cost driver: Si ($\sim$ 50%)

- Develop and study a new mechanical model with reduced R_{ECAL}, N layers. Best is to fit ECAL dimensions to integer number of sensor lengths, but not forgetting about constraints from other subdetectors.
- Endcaps need to be modified: too high W load on 1 mm thick carbon walls
- Endcaps will also contain endcap "rings" close to beam pipe. No detailed design yet, high e^+e^- backgrounds from beam-strahlung ($\lesssim$ 170 hits/chip/spill)

Prototyping: current status

Technologically oriented prototyping after physical prototype in 2006-2011.

DAQ: SKIROC2 self-triggering front-end chip with 64 channels, 4 chips on PCB (FEV8) with one glued Si 18x18 sensor. Read out with DIF board $\rightarrow$ HDMI cable $\rightarrow$ GDCC (substituted LDA in May 2013). BX clock and spill signals are distributed by CCC board.
Mechanical support for maximum 10 slabs with 2.1, 4.2 or 6.3 mm W plates, relaxed layer pitch 15 mm.
New "distributed" DAQ software: many GDCC's and many PCs (to be tested).

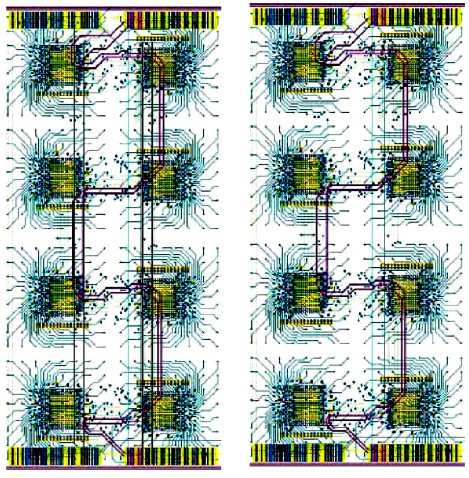


New PCB, FEV8 → FEV9

First FEV9 is produced and received 2 weeks ago, perfect flatness! Improvements:

- correct SKIROC “grounding”: to stabilized 3.3 V
- swap of digital and analog power supply (bug) is fixed
- power line decoupling capacitors to reduce noises
- 2-3 times shorter signal traces (less input C and pick up noises)
- signal transmission over long distances ($\sim$ 2m, esp. for clock, two FEV9 options: with straight and snake lines)
- 16 SKIROCs instead of 4
- new SKIROC BGA packaging (400 balls), 124 chips received this week

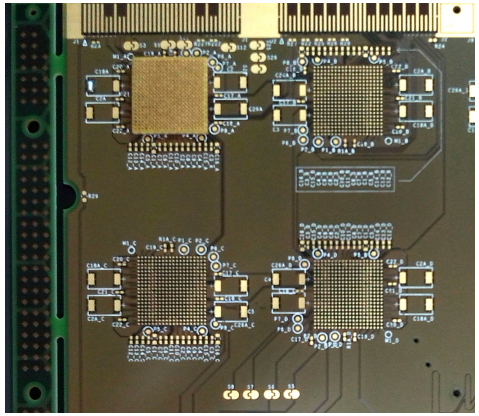
Mechanical model, no chips



Straight and snake lines

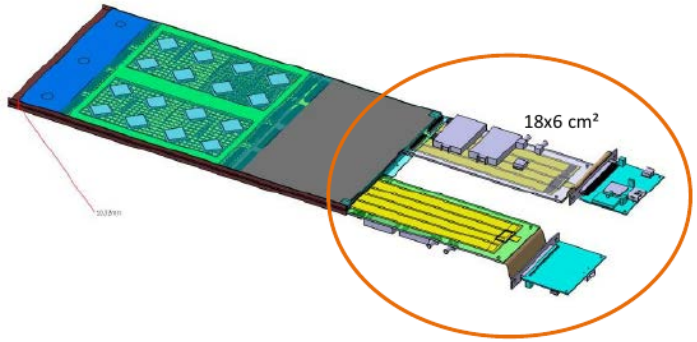
Next steps

First, test new packaging using FEV9 with BGA socket (ordered and received), SKIROC may be remounted. If Ok, permanently solder 4, 8 and finally all 16 chips (for 4 wafers). Qualification of FEV9: Dec'13.



1/4 of FEV9 with BGA slot (top left)

SMB4 design (between many ASUs and DIF) has just started (with power for many ASUs and special line drivers for long line transmission). First SMB4 in Feb'14, tests in Mar'14.



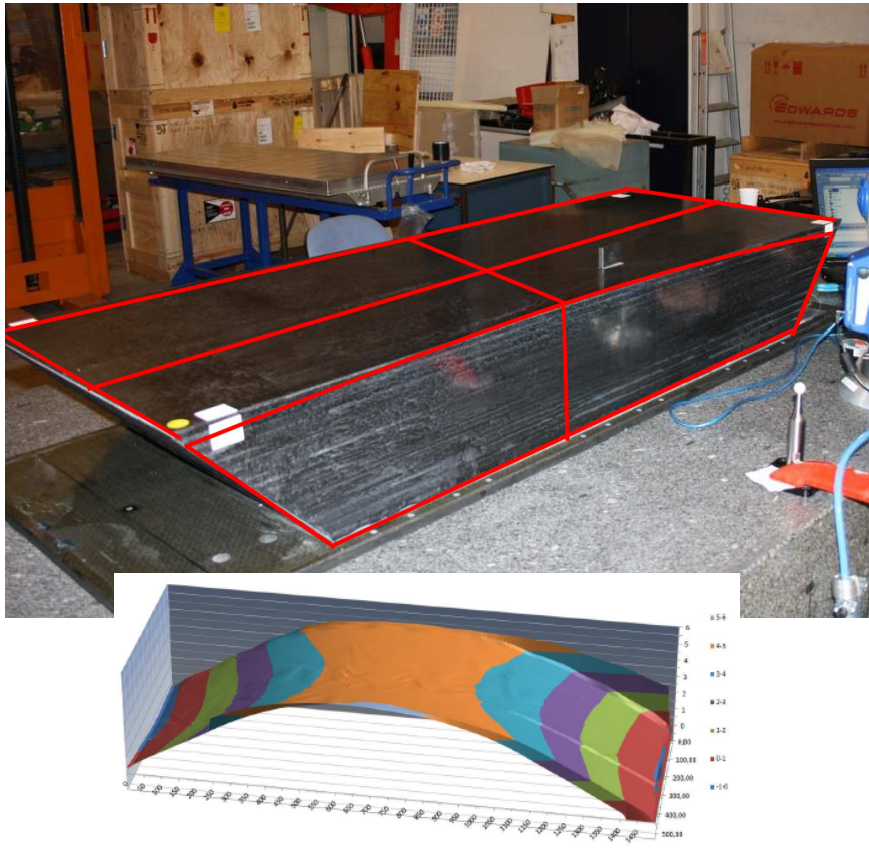
Decision on long line (straight or snake), qualification of next version FEV10 in Apr-May'14.
U-type short slab production, May-Jun'14
Physics tests (cosmics, laser, PHIL accelerator at LAL) June-Dec'14
Long slab production, Oct'14

In parallel, look at boards integration in ILD.

Test of full scale tower

Plan: produce ≥ 1 long and short slabs to fill alveolar tower. Reuse existing 1/4 ASU short slabs. With GEANT4 simultion, find their affordable fraction in the tower.

Test at CERN in 2015.



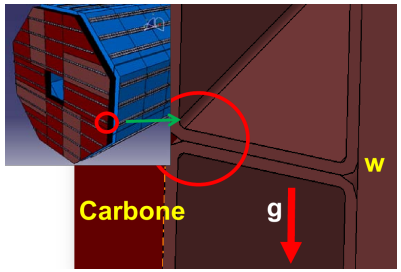
Lab view

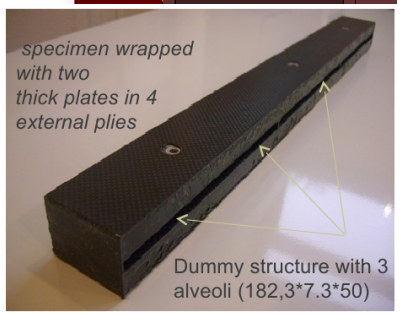
LPSC

- Mechanical design of alveolar endcaps

  Molding of first 2.5 m one layer module with 3 alveoli. Special handling tool for endcap and barrel modules using their rails.

First crack sound from alveolar skin of 1.82 m dummy structure in real test at 6.6 MPa (35 MPa in simulation). ≈ 3 safety factor, not enough (seismic conditions).





LPSC (cont.)

- Cooling system (end-caps + barrel)

  Cooling station design, global pipe integration, sensors, controls; priliminary tests of full scale leakless loop
- Contribution to prototypes: internal and external plates of the EUDET module, heat exchanger
- ECAL support rails (endcaps + barrel)

LPNHE

Si sensor gluing robot

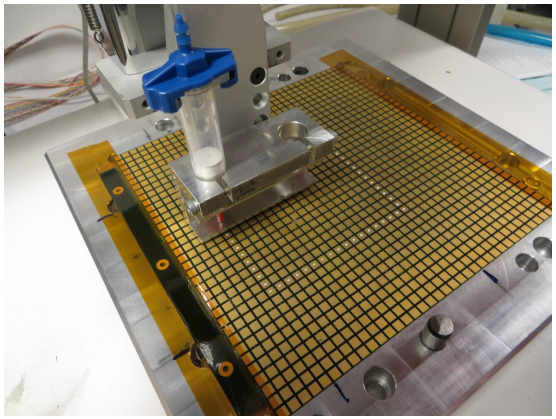
- Short-term : gluing of one sensor per PCB (9 sensors glued in total)

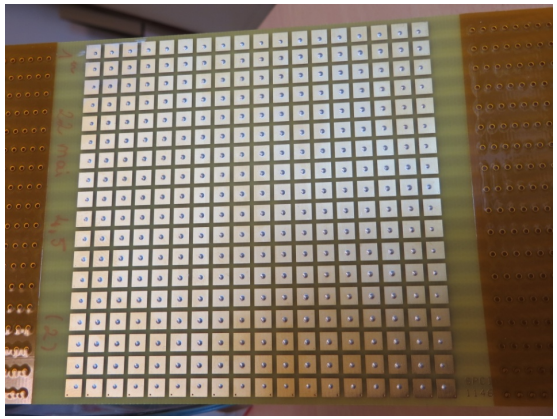
  Constraints on PCB are defined:

  - Flatness
  - Parallelism of the edges
  - Uniform height of ASIC soldered on board

  Improvements:

  - use of specific pumps for dry and clean vacuum
  - careful PCB cleaning
  - outer glue dots slightly shifted to center to avoid short cuts





LPNHE (cont.)

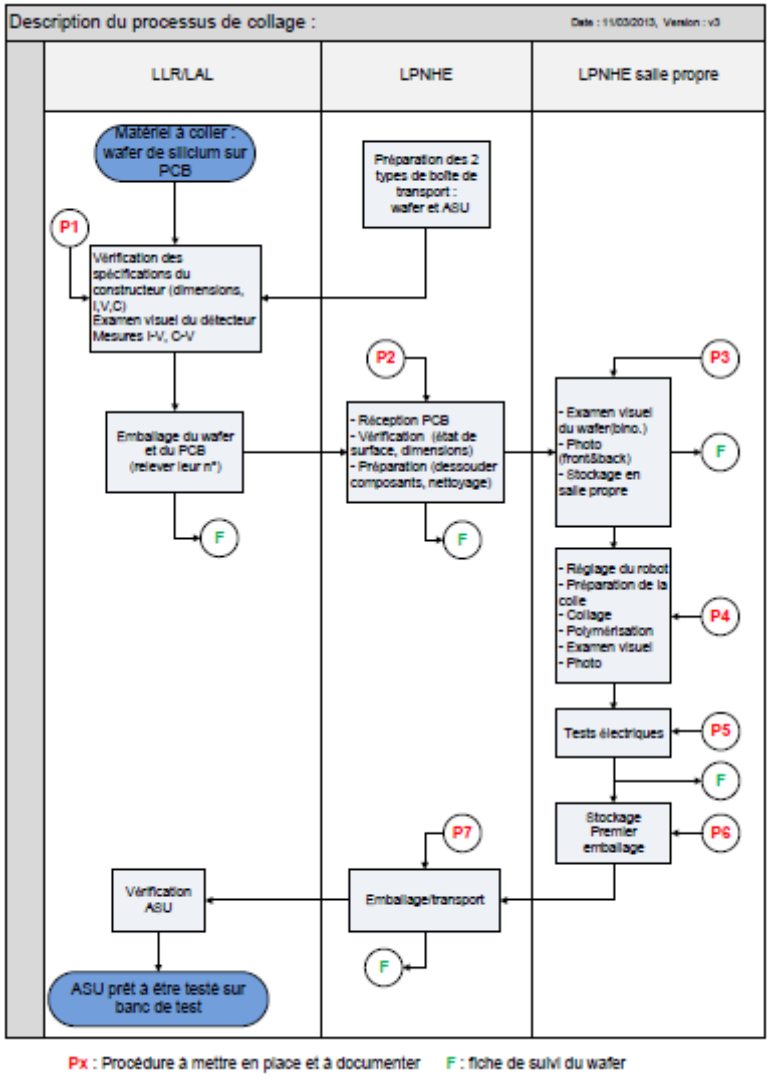
first task flow between LPNHE/LAL/LLR, reception and gluing procedures at LPNHE are written

- mid-term (in progress): fully automated process.

Positioning and aligning with the second robot. Glue 4 sensors on a PCB. Clean room for both robots.

- long-term: mass production

In parallel: Si sensor production at Lfoundry. Sensor specifications have been sent.



PHIL accelerator at LAL

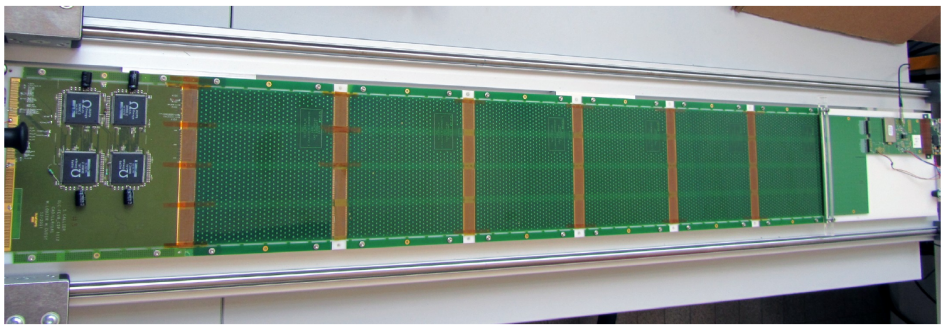
1-3 MeV e^-, minimal measurable bunch intensity 10^8, very short duration. All electrons arrive at the same time: can mimic high energy showers at CERN.

$\sim 100 \times 100\ \mu m^2$ collimators (eg. 5-10 mm of steel) can reduce intensity from 10^8 to $\sim$ 2000 MIPs measurable by ECAL DAQ. Point-like source, suitable for scans. 3 MeV e^- can pass 2 or 3 layers with sensors and PCBs, can be put in coincidence. Most interesting: guard ring cross talk study.

Other tasks: measure cross talks between inner pixels, across SKIROC channels, efficiency scans, power pulsing tests with 5 Hz PHIL bunches. PHIL upgrade next year : bending magnet, variable beam intensity. Wide beam with $\sim 0.1 e^-$ per pixel will allow silicon sensor calibration.
Application for P2IO postdoc has been sent.

LAL

- Slab assembly: HV Kapton, ASU interconnections, plan to semi-automate
- Analysis of beam test data
- Signal transmission tests for long slab with interconnections and simplified straight PCB lines
- COB design

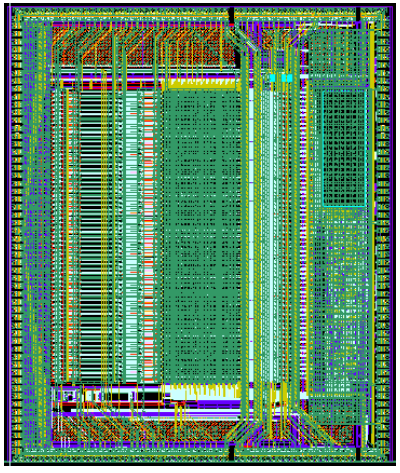


Omega group

- Production of SKIROC 2B and SPIROC 2D : $\sim$ end 2014, <50 kEUR, large production

SKIROC 2B: improve performance and fix bugs, pin compatible with SKIROC2.

SKIROC2



- SKIROC3 development

  HARDROC3 received in Jun'13 (AIDA milestone): zero suppression, more complicated digital part, SCA depth 16 $\rightarrow$ 8, new slow control using I2C link. Not backward compatible with HARDROC2.

  Similar changes in SKIROC3, to be discussed after 2B.

LLR

- ECAL ILD general design and optimization
- Si sensors (ordering, characterization, optimization)
- DAQ electronics (SKIROC packaging with Ω, FEV, SMB, DIF, GDCC)
- long slab design (w LAL)
- mechanical prototypes (w LPSC)
- slab assembly (w LPNHE, LAL)
- DAQ software
- beam tests, data analysis (w LAL); cosmic and laser tests

Optimistic dates

- New PCB FEV9, BGA packaging. First, with BGA sockets. Dec'13
- New adaptor board SMB4 for many ASUs (Mar'14)
- FEV10 design, production (Apr-May'14)
- U short slabs May-Jun'14
- Long slab Oct'14
- Physics tests (cosmics, laser, PHIL accelerator) Jun-Dec'14
- CERN beam test with one tower in big mechanial structure in 2015
- SKIROC 2B in the end of 2014 (Omega), then SKIROC3
- Guard ring studies at PHIL (2014) and with laser