# ILC ORIENTED R&D IN ITALY

## A bright future behind us


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- acceleration related activities within the GDE:
  - design of the Damping Rings [Susanna Guiducci at LNF-Frascati]
  - design of the Main Linac [Paolo Pierini at LASA-Milano]

mission accomplished with the TDR fulfillment ; since then, the ILC related activity dropped to a minimal level, limited to a participation to the FP7 project EUCARD-2 (Enhanced European Coordination for Accelerator Research & Development) on Low Emittance Rings.

- detector related R&D:

  - early activities by Paolo Checchia et al. on a hybrid (Silicon + Scintillator) e.m. calorimeter (http://www.pd.infn.it/~checchia/lcit/Welcome.html) (LCCal collaboration) (1999-2005) + Technology development on hybrid pixels with capacitive coupling (MCa)

  - P-ILC, supported by INFN-CSN1 on vertexing (EUDET included), SiPM +Scintillator tile hadron calorimetry & simulation for the IV concept (2006-2009)+independent DREAM activities

  - MCS, supported by INFN-CSN5, possibly the indication of a soft re-start [2014, Stefano Veneziano, Simonetta Gentile (Roma1) and MCa]

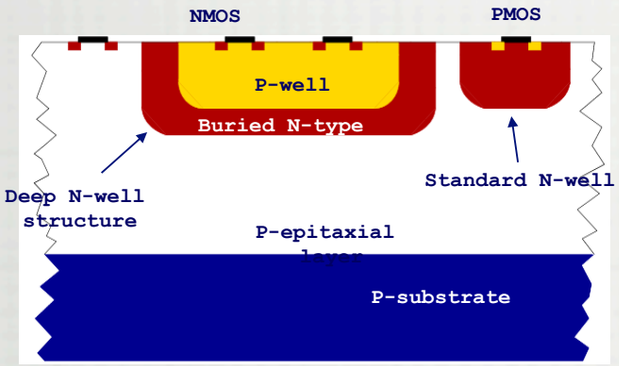
# A bit more about P-ILC:

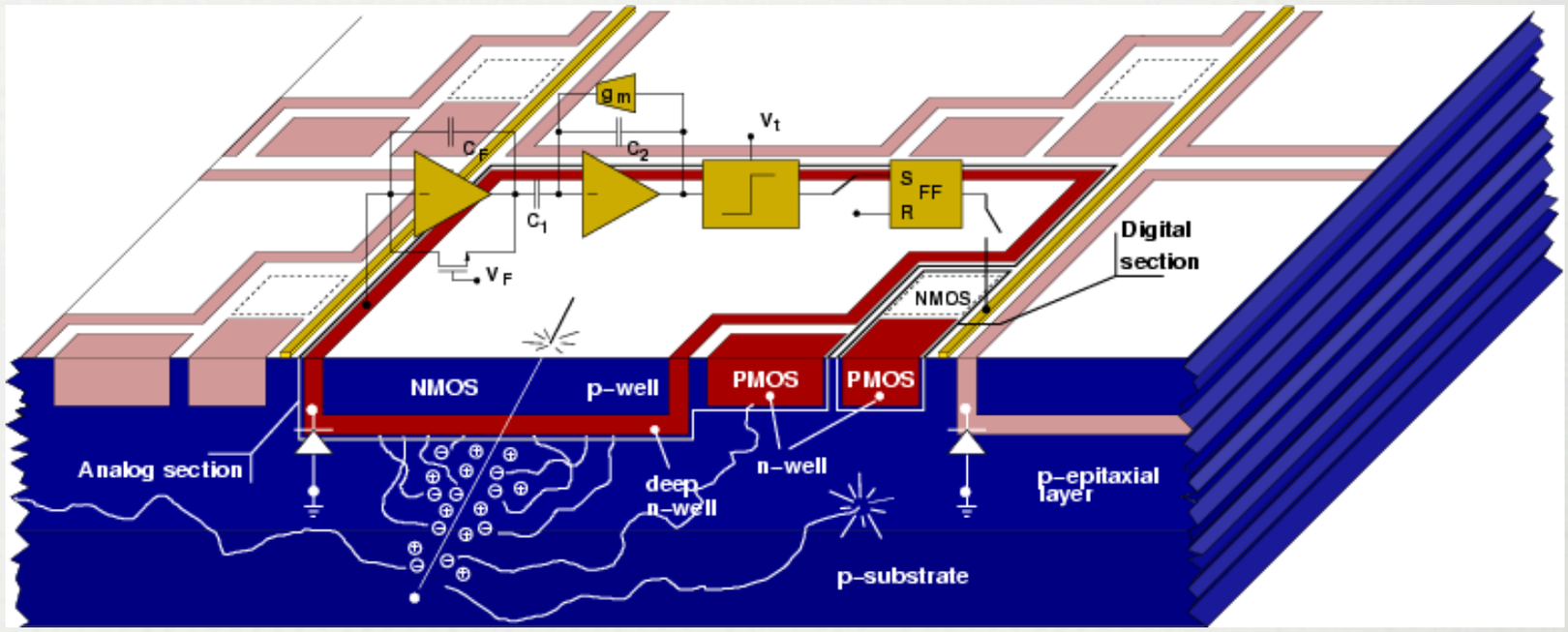
| | FTE 2006 | FTE 2007 | FTE 2008 | FTE 2009 |
|---|---|---|---|---|
| **Milano** | 3.1 | 3.4 | 3.3 | **3.5** |
| **Roma 3** | 1.0 | 2.2 | 0.7 | **0.2** |
| **Ferrara** | 1.0 | 2.0 | 1.7 | **0.8** |
| **Pavia** | 3.0 | 4.5 | 5.5 | **2.5** |
| **Lecce** | - | 2.5 | 2.5 | **2.3** |
| **LNF** | - | 2.1 | 2.0 | **1.7** |
| **Roma 1** | - | 2 (3.9) | 2 | **1.0** |
| **Tot. FTE** | 8.1 | 18.7 | 17.7 | **12.0** |

with investment of ~ 120 kEUR/year [Additional cost, manpower excluded]

# About VTXing (Pavia/Bergamo/Roma III): the focus has been on the STm 130 nm triple-well technology

In triple-well CMOS processes a deep N-well (DNW) is used to isolate N-channel MOSFETs from substrate noise




- A DNW is used to collect the charge released in the epitaxial layer
- NMOS devices of the analog section are built in the deep N-well
- a standard Charge Sensitive amplifier and a 1-bit memory cell for on-pixel sparsification can be implemented

# The ILC oriented demonstrator (25 micron pitch) [2006-2008]:

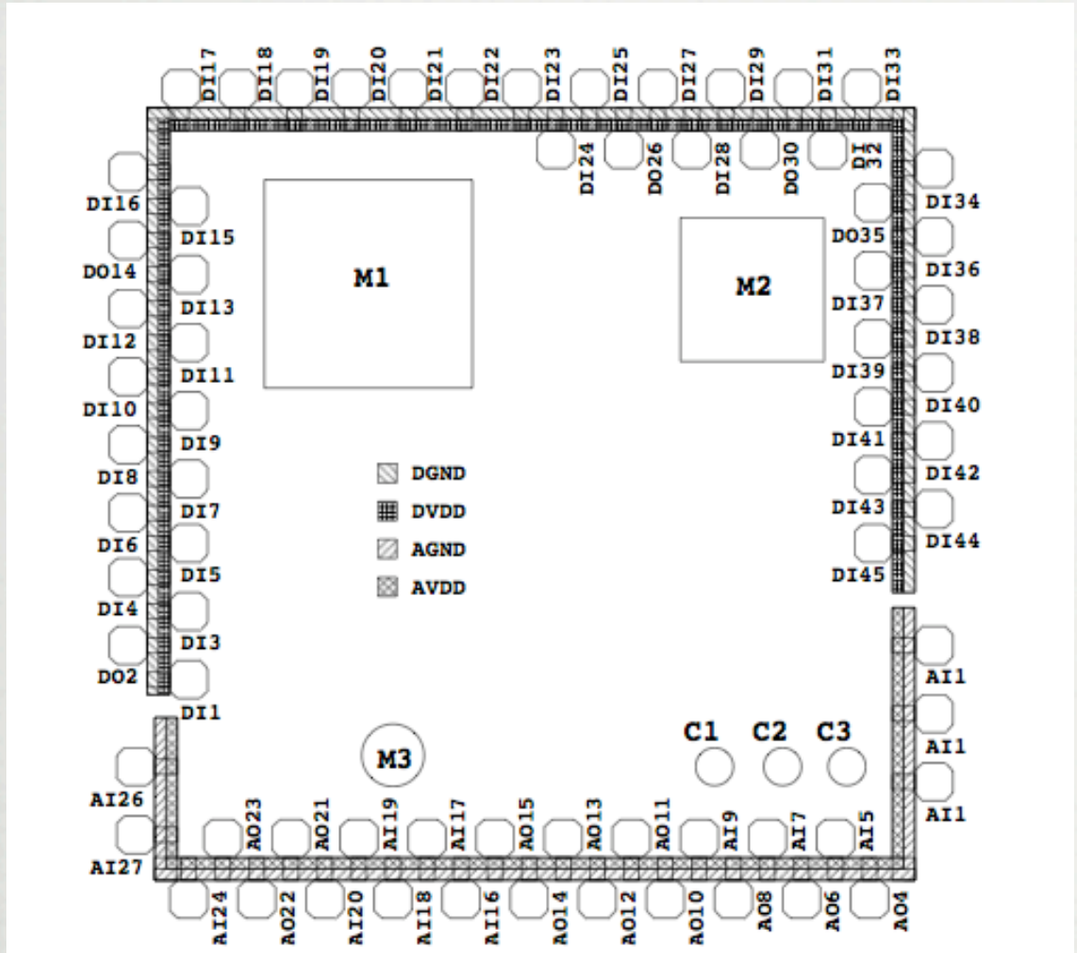
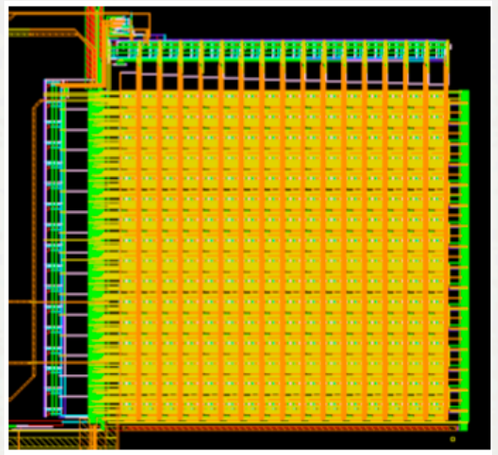
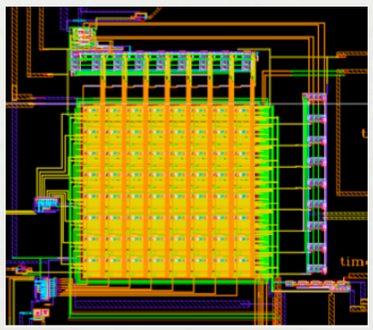


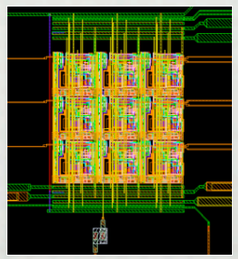

Figure 18: schematic representation of the SDR0 chip layout and pad diagram.



M1
16 x 16 pixels
Full digital machine
Binary output

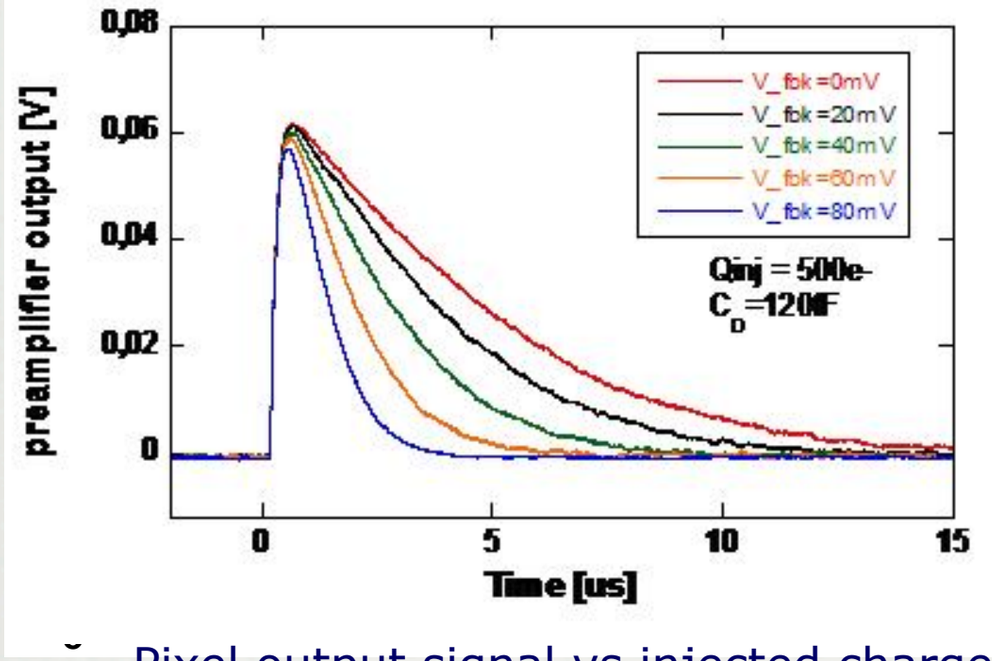


M2
8 x 8 pixels
Full digital machine
Analog output of a selected pixel



M3
3 x 3 pixels
NO digital machine
Analog output of all of the pixels

# A snapshot of the basic features:

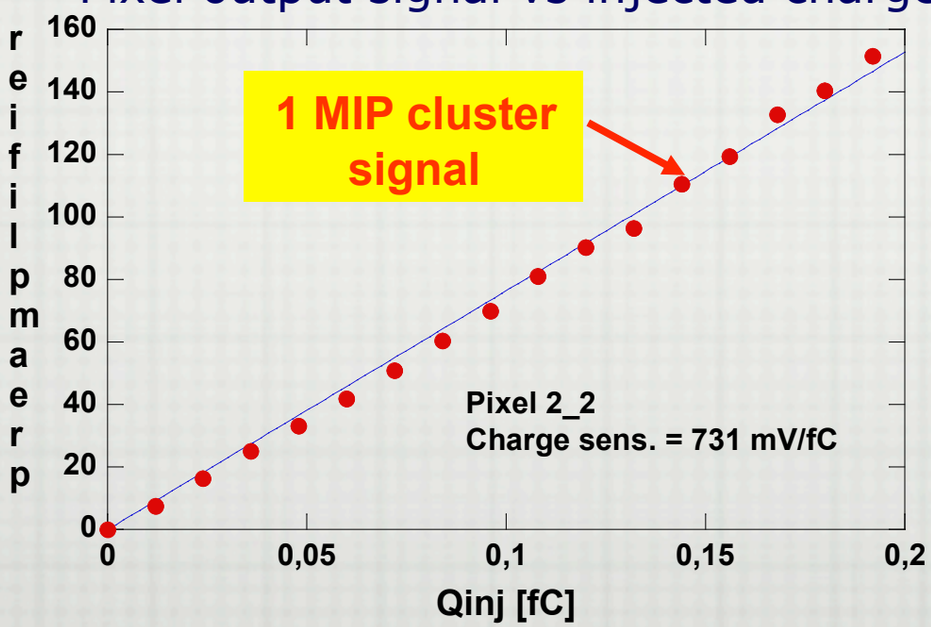



- Average **charge sensitivity ≅ 0.7 V/fC**
- ENC = **40 e rms @ $C_D$=120 fF**

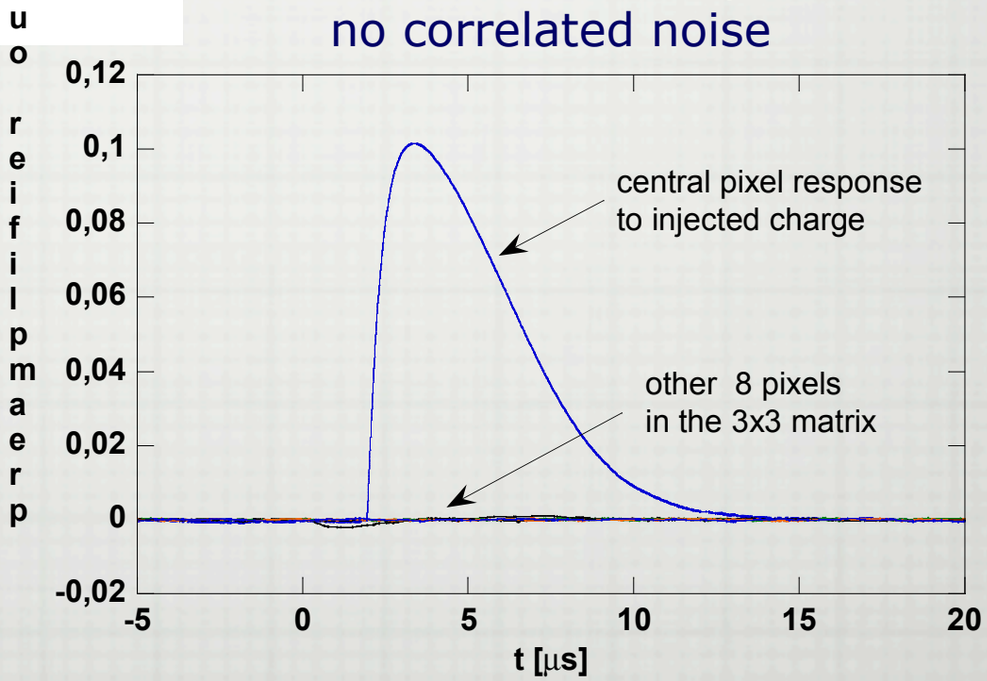
  (preamplifier input device: $I_D$ = 1 mA, W/L = 22/0.25)
- **Threshold dispersion ≅ 60 e**

  (in 16x16 matrix and 8x8 matrix)

Pixel output signal vs injected charge




No crosstalk between pixels, no correlated noise



# A key questions: what are these artists doing by now?

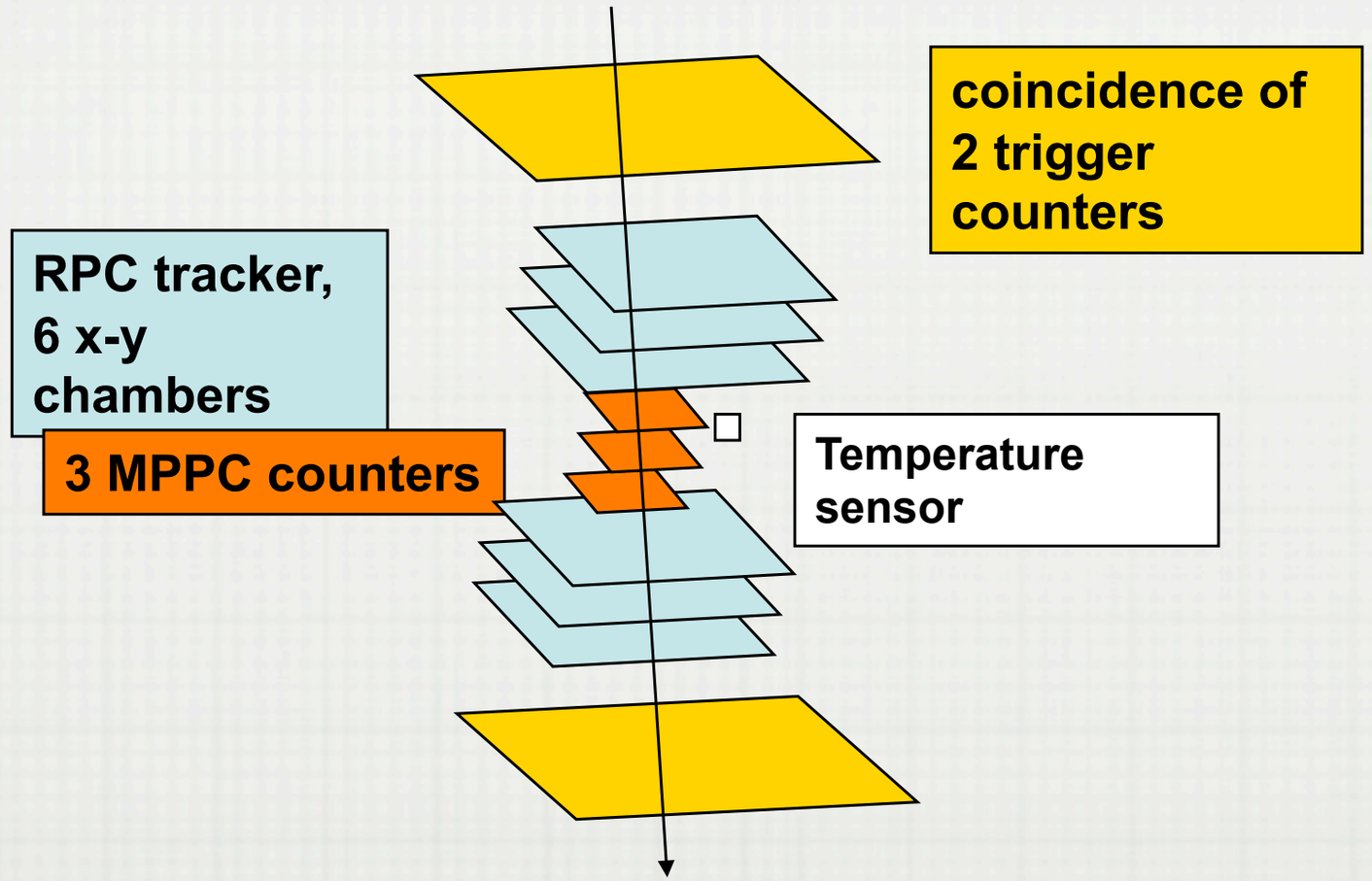
- Eleuterio Spiriti moved from Roma III to LNF and he's involved in the ALICE upgrade

- Valerio Re, Ludovico Ratti & co-workers joined the VLSI 65 nm project, with a focus on the CMS upgrade [after a period invested in the SuperB project & on 3D technologies]

- Antonio Bulgheroni is at JRC-Karlsruhe; gone with the wind..

so: there's certainly a significant "Silicon Community" in Italy, however the GoodOldBoys are fully committed by now and I am optimistic about the involvement of "freshmen", provided the ILC scenario is more clear.

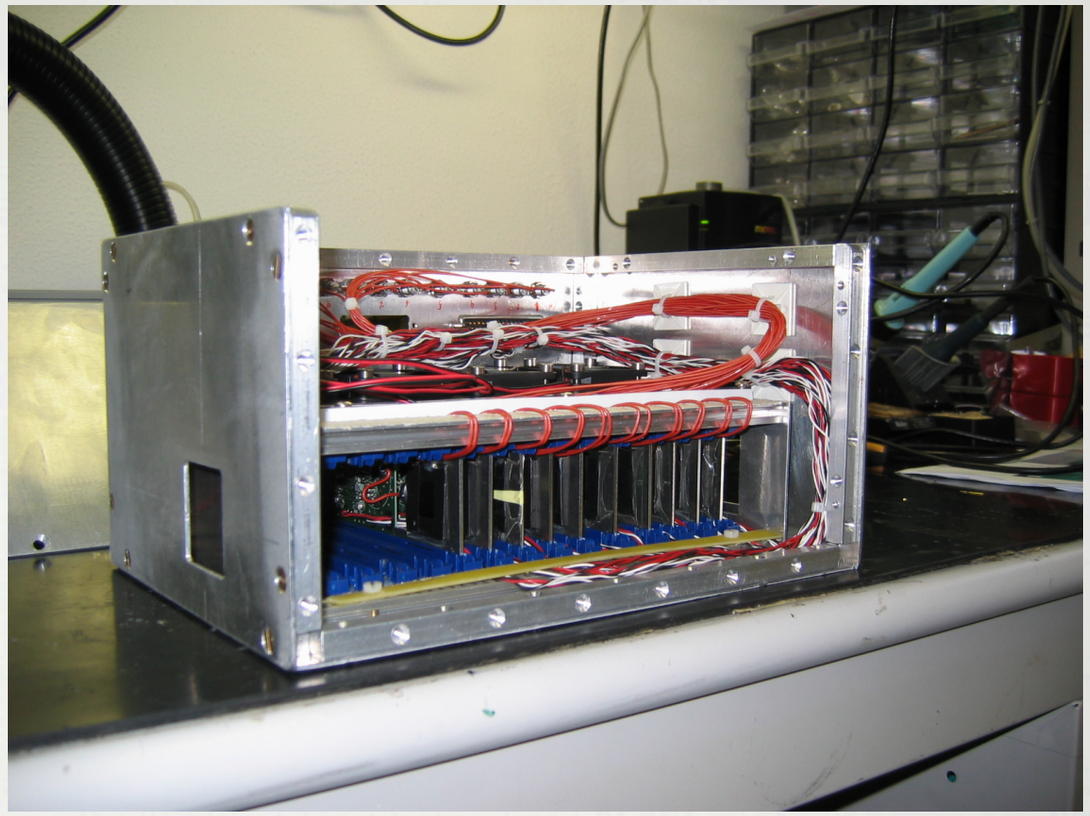
# About CALOrimetry (Roma I/LNF): the focus has been on an analog hadron calorimeter based on scintillating tiles + SiPM




**100-150 evts/day with x-y tracking on the 3x3cm$^2$ tiles**

Test set-up for the characterization (photo-electron/mip, uniformity) of different prototype tile (wrt scintillator, engineering and sensors; 2007). Cosmics + BTF@LNF

# The MagicBox used to test 10 tiles in one run:



## Taxonomy:

- Ch.1 – BC400 5mm, Hamamatsu 400 pixels [SiPM glued on the side face]
- Ch.2 – BC400 5mm, Hamamatsu 1600 pixels
- Ch.3 – "CCCP" scint 5mm, Hamamatsu 400 pixels
- Ch.4 – EJ212(BC400 eq.) 2mm, Hamamatsu 400 pixels
- Ch.5 – EJ212(BC400 eq.) 2mm, Hamamatsu 1600 pixels
- Ch.6 – BC400 5mm, Hamamatsu 3x3mm$^2$ [SiPM glued in the centre]
- Ch.7 – CALICE tile, MePhi (CALICE reference) [WLS fiber]
- Ch.8 – BC400 5mm, IRST SiPM
- Ch.9 – BC400 5mm, SensL 1300 pixels
- Ch.10-EJ212(BC400 eq.) 2mm, SensL 1300 pixels

## Motivations:

- (1 vs 2) + (4 vs 5) measure the effect of the PDE
- (1 vs 4) + (2 vs 5) tile thickness
- 1 vs 3 :scintillator producer
- 1 vs 6: sensor area
- (1,2) vs (8,9): different SiPM producers (5mm thick tile)
- (4,5) vs 10: different SiPM producers (5mm thick tile)
- Compare to the CALICE benchmark

The same key questions: what are these artists doing by now?

- Sandro Calcaterra joined BESIII
- Riccardo de Sangro joined BELLE II
- Simonetta Gentile: very active in ATLAS but still very interested

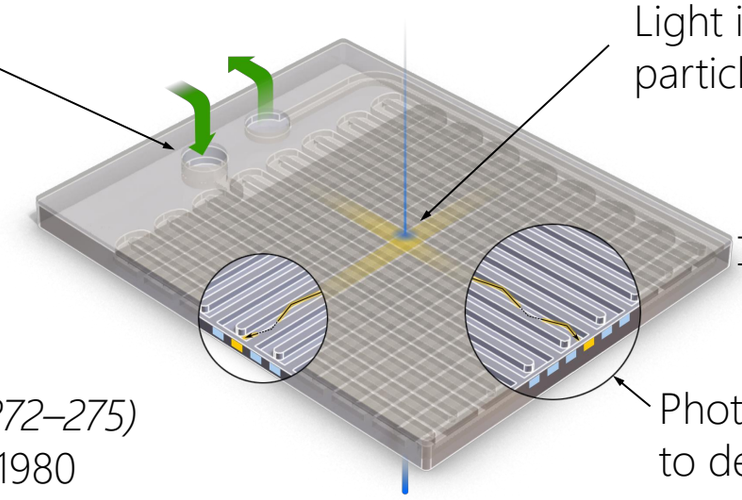
So, the answer is not so different w.r.t. the VTX community...

# A soft step back to the future: the MicroCapillariScintillanti project (INFN, CERN, EPFL), lead by Stefano Veneziano@Roma 1 and joined by Simonetta Gentile & MCa

## The concept of MicroFluidic Scintillation Detectors :

Single microfluidic serpentine filled with liquid scintillator

Light is generated upon interaction with a particle and guided along microchannels



Microtechnologies allow to manufacture very thin devices

Photodetector arrays on the sides allow to determine the interaction position

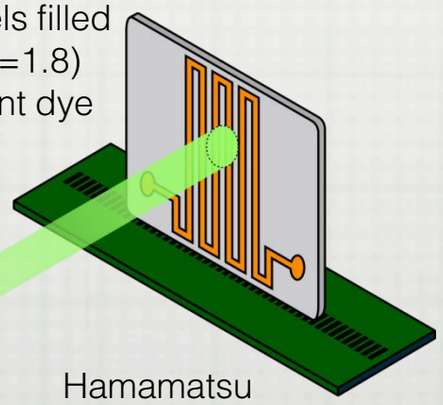
Ref: Mapelli et al., *Sens. Act. A 162 (2010) 272–275)*
**Patent filed** 8th May 2012, PCT/EP2012/001980

## First results:

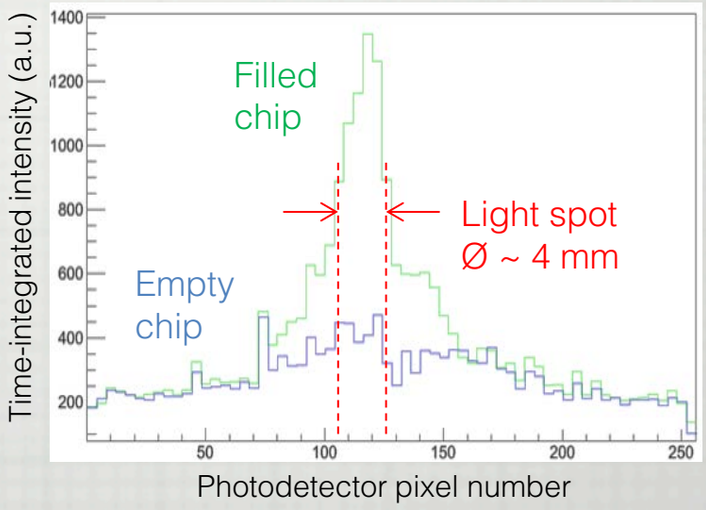

500 μm pitch between the channels

SU-8 (n=1.6) microchannels filled with methylene diiodide (n=1.8) + rhodamine 6G fluorescent dye

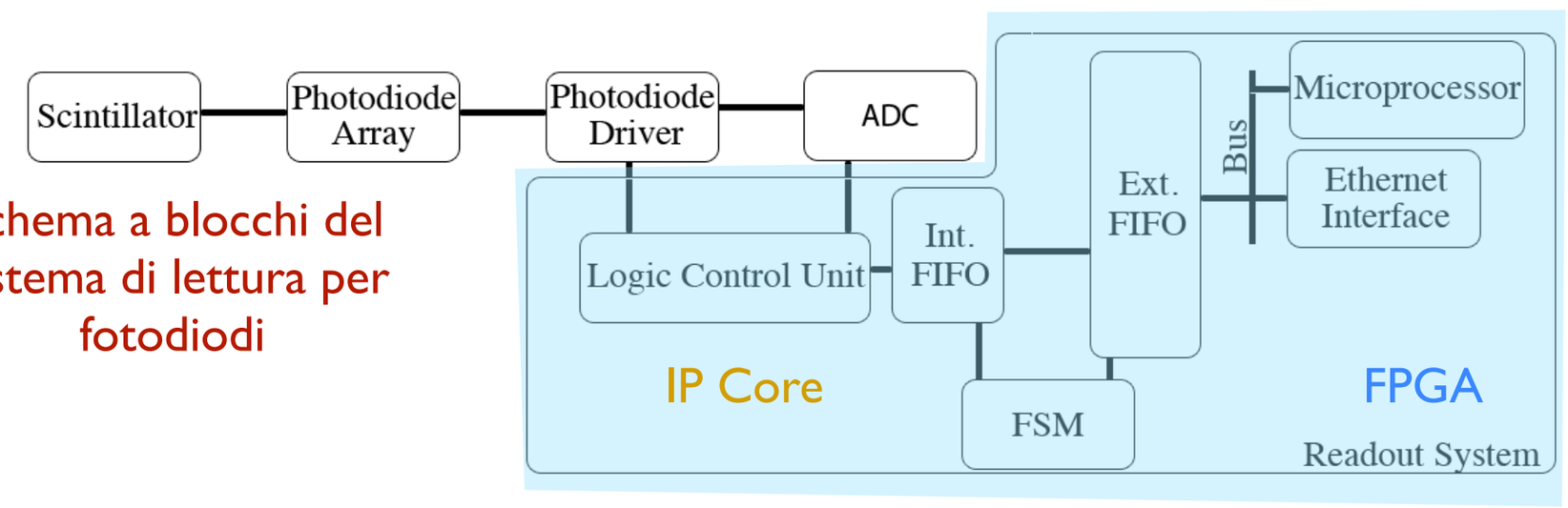
Green light (spot Ø ~ 4mm)



Hamamatsu photodiode array (PCB)



The know-how in the read-out of the detector can be interesting for the ILC, since SiPM are the photosensors of choice for MCS:




Schema a blocchi del sistema di lettura per fotodiodi

FPGA with embedded processor, essentially the same platform used by the University of Mainz for re-designing the Clock&ControlCard and the "DataAggregator" for the Analog HCAL [see the talk by Aliakbar Ebrahimi at LCWS2013]

A first step was taken during LCWS2013 and we joined Tohru Takeshita and Katsushige Kotera in the optimization of the "small tile design" for an Ecal based on scintillating "strips" (45x5x1mm$^3$)

No fireworks, nothing but a small activity hopefully marking a comeback...

# Final remarks

- at LCWS it was clear that a *phase transition* is ongoing for ILD and SiD moving towards optimization, integration and questions at system level, so it would really the right time to re-start..

- No doubts the INFN potential is quite high; however, till when the scenario will be more clear it will be hard to have a commitment beyond the bare survival level [the push by the LHC community and the budget constraints simply do not allow it]

- in such a phase, waiting for the sun to rise, IMHO 3 issues might be relevant to trigger a stronger commitment:

  - actions involving Italian companies (e.g. in Silicon pad production [FBK and STm] and optimized pcb for the Ecal, as discussed with JCBrient)

  - having a fair degree of co-funding by external resources (possibly the main issue in the afternoon discussions)

  - focusing on R&D providing a technology platform common to other HEP experiments [e.g. MAPS for STAR and ALICE, SiEcal for the CMS upgrade]