ATLAS DCS Upgrade

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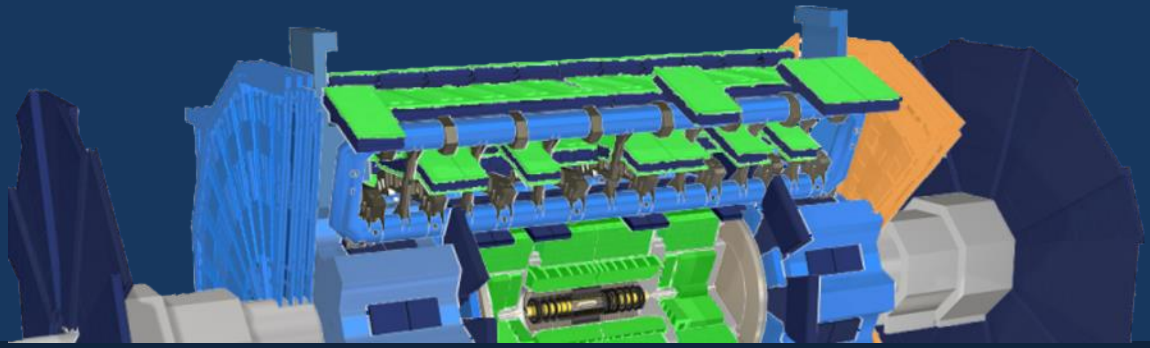
http://atlas.ch

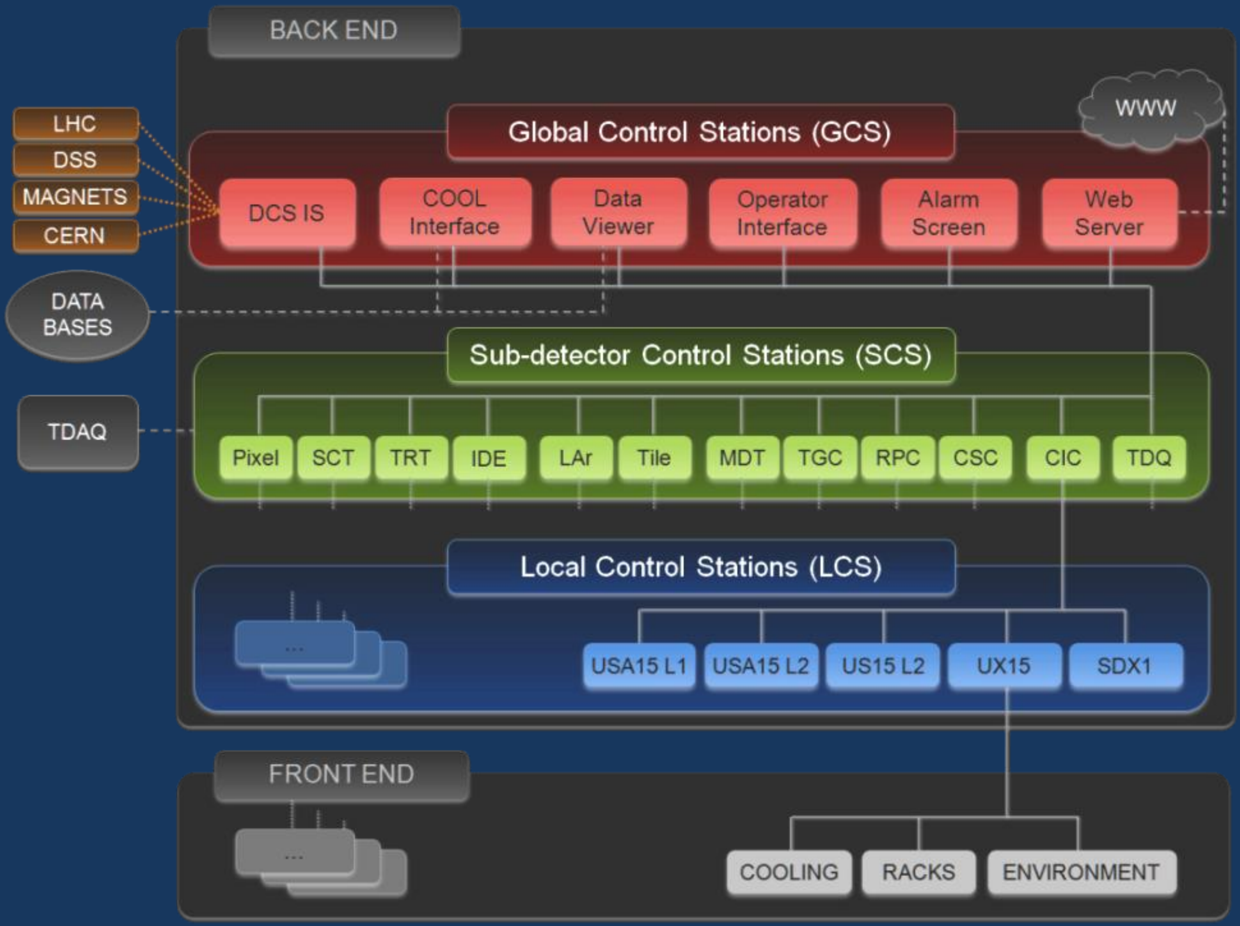


DCS Architecture

- Facilitate management of implementation, operation and maintenance by using standard building blocks
  ➲ **J**oint**CO**ntrols**P**roject

- Controls hierarchy:
  1. Front-End (FE):
     detector interface
  2. Local Back-End (BE):
     FE connection, readout, processing
  3. Sub-detector BE:
     grouping different technologies, standalone operation
  4. Global BE: interfaces to operators, storage and external facilities

Detector Control System



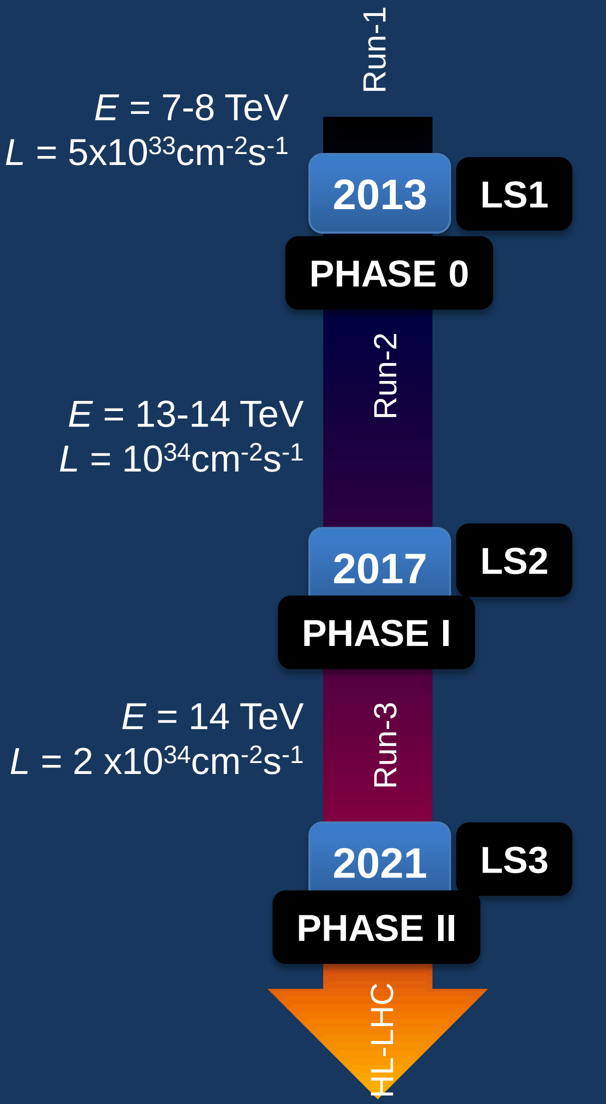
Layer architecture + FSM pays off during upgrade phases!

Future Upgrades

Upgrade Constraints

- ▶ Higher luminosity ➲ need to increase radiation tolerance for cavern equipment by factor ~10
- ➲ ELMB successor: ELMB++, still in designing stage
  - ➲ Radiation hardness!
  - ➲ Backwards compatibility
  - ➲ Fix bugs, support new connectivity (Ethernet)
- ▶ Phase 0 (installed):
  - ▶ new Pixel Inner B-Layer (see Lukasz Z. talk on DCS cooling)
- ▶ Phase I (approved):
  - ▶ Fast Track Trigger (electronics)
  - ▶ LAr (trigger electronics)
  - ▶ TDAQ
  - ▶ **NSW (New Small Wheel)**
- ▶ Phase II (planning): Replace complete inner detector

LHC Upgrade Schedule



Run-1

E = 7-8 TeV
L = 5x10^{33}cm^{-2}s^{-1}

2013 **LS1**

PHASE 0

Run-2

E = 13-14 TeV
L = 10^{34}cm^{-2}s^{-1}

2017 **LS2**

PHASE I

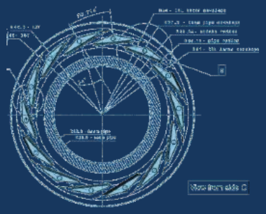
Run-3

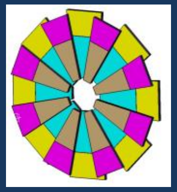
E = 14 TeV
L = 2 x10^{34}cm^{-2}s^{-1}

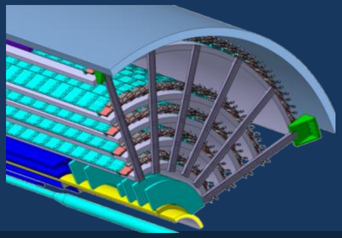
2021 **LS3**

PHASE II

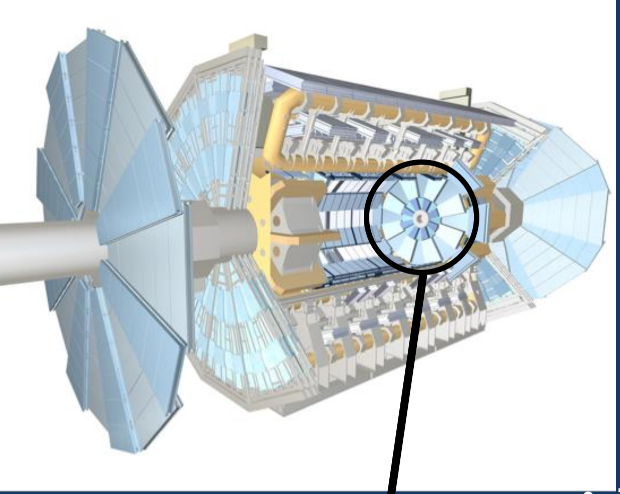
HL-LHC







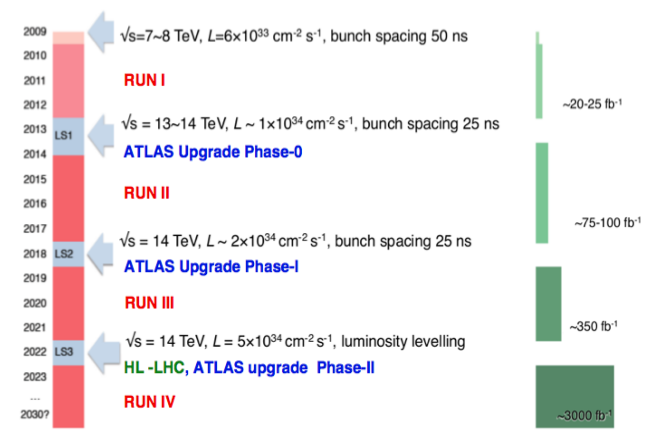
Motivation ATLAS Small Wheel Upgrade 2017-18 (Phase I)



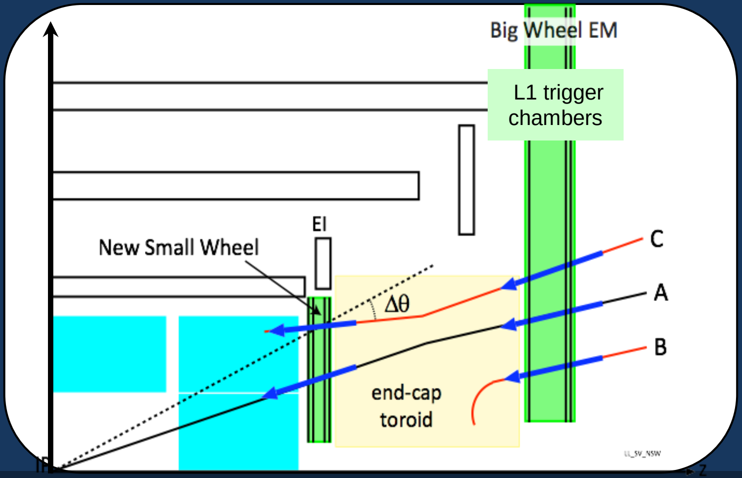
The innermost station of the muon endcap

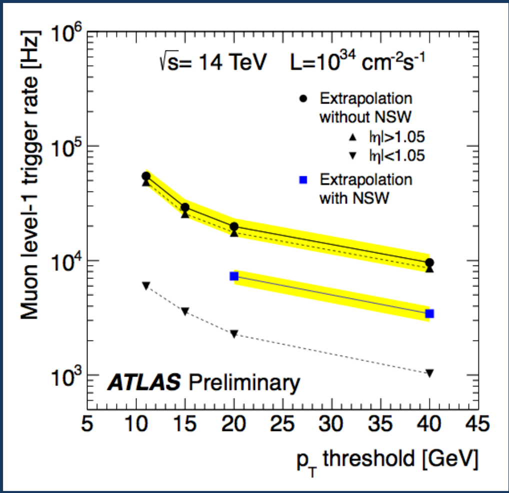
Located between endcap calo and toroid

Pseudorapidity coverage:
$1.3 < |\eta| < 2.7$

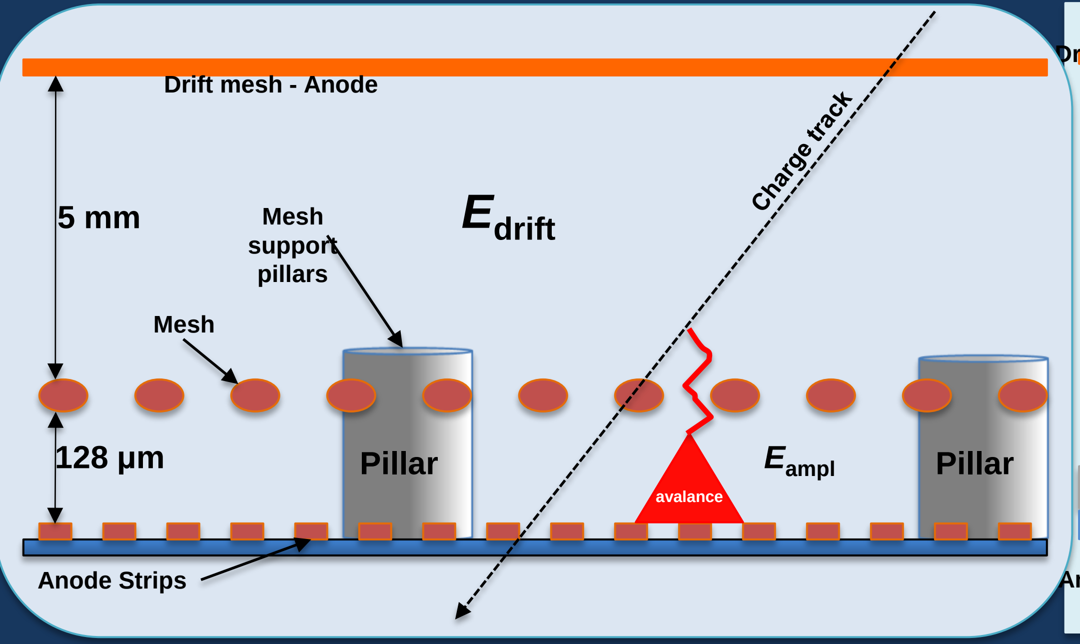


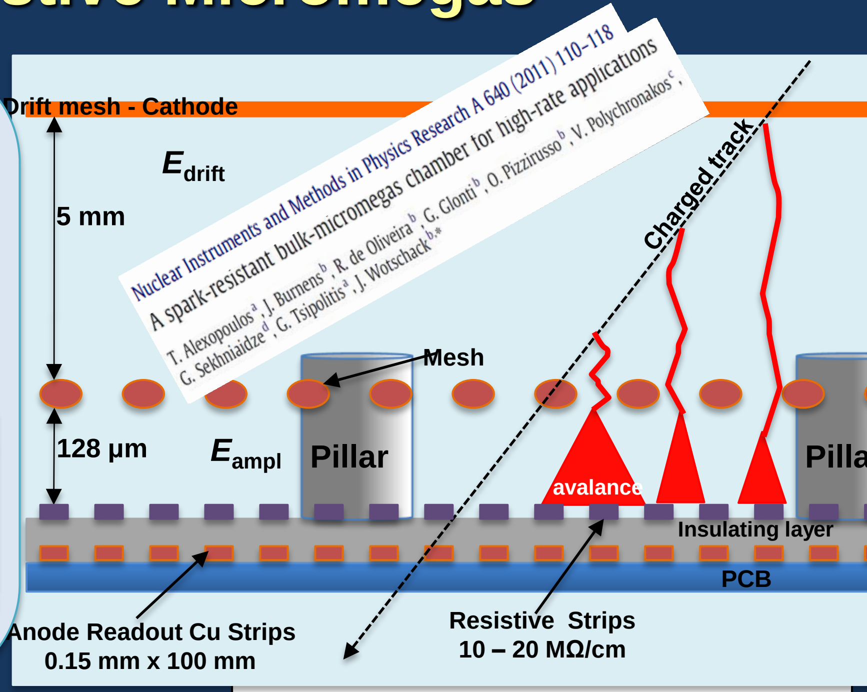
- **The ATLAS upgrade is motivated primarily by the pile-up rate (<*n*>=55 interactions per 25 ns bunch crossing) that are expected at $L=2\times10^{34}$ cm^{-2}s^{-1}. This will lead to an increased particle flux (rate) which the present detectors (MDT + CSC) cannot handle efficiently. Also, added trigger capability.**
- **Replacing the Small Wheels with a detector that can provide precise tracking and trigger segments will eliminate fake triggers without loss on physics acceptance. (sTGC + Micromegas)**





Micromegas technology - Resistive Micromegas

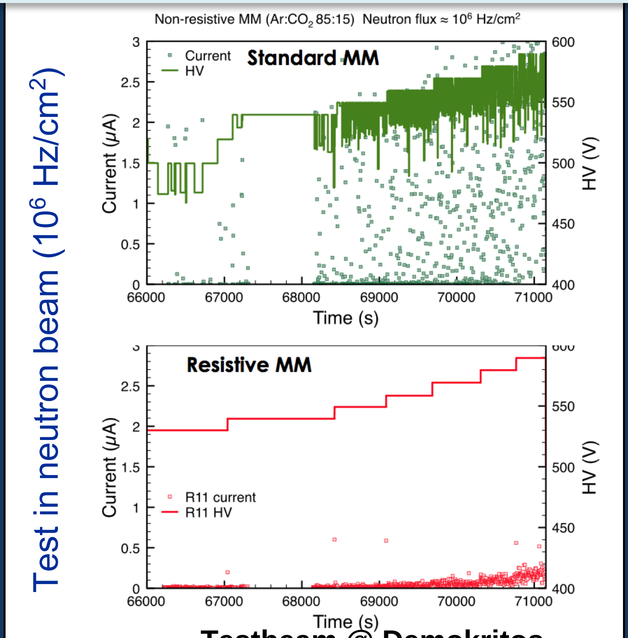



Nuclear Instruments and Methods in Physics Research A 640 (2011) 110–118

A spark-resistant bulk-micromegas chamber for high-rate applications

T. Alexopoulos[a], J. Burnens[b], R. de Oliveira[b], G. Glonti[b], O. Pizzirusso[b], V. Polychronakos[c], G. Sekhniaidze[d], G. Tsipolitis[a], J. Wotschack[b,*]

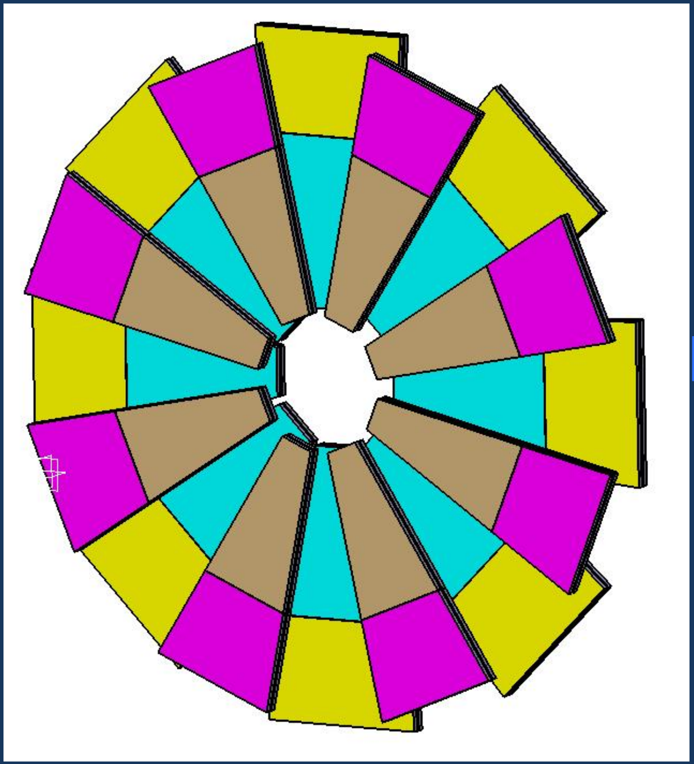
- **Micromegas** *(I. Giomataris et al., NIM A 376 (1996) 29)* **are parallel-plate chambers where the amplification takes place in a thin gap, separated from the conversion region by a fine metallic mesh**
- **The thin amplification gap (short drift times and fast absorption of the positive ions) makes it particularly suited for high-rate applications**

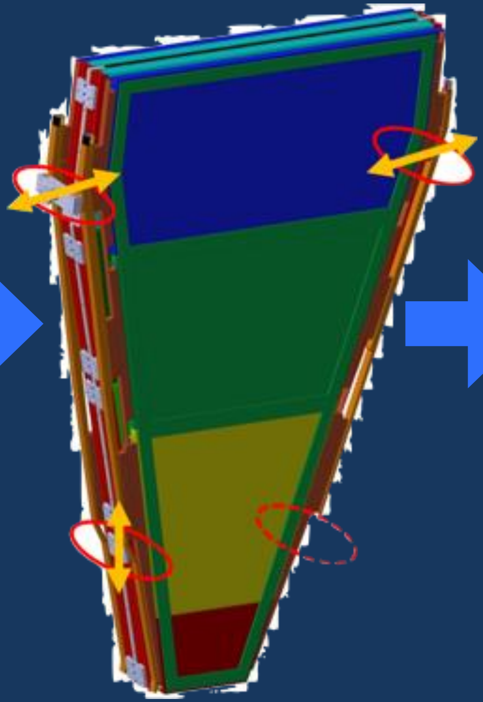


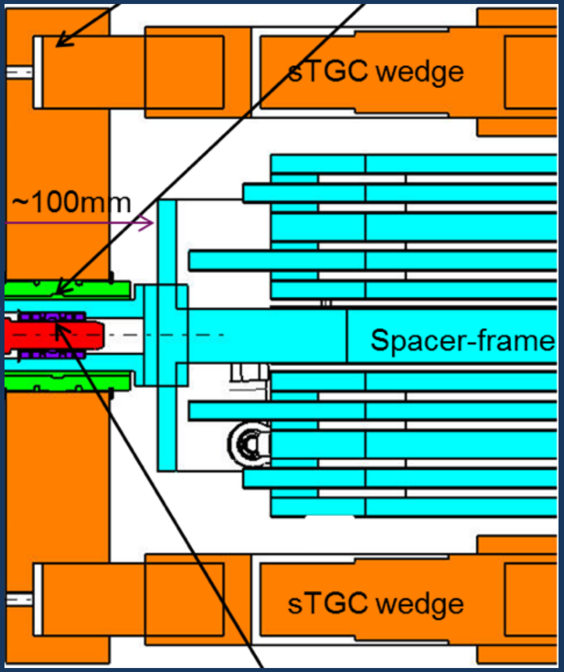
Testbeam @ Demokritos

New Small Wheel (NSW) Layout

- Two technologies: Both Micromegas & sTGC detectors will provide tracking and trigger data
- 16 Sectors per Wheel (8 large, 8 small)
- 2 Multilayers per Sector
- 8 Micromegas Layers & 8 sTGC Layers per Multilayer





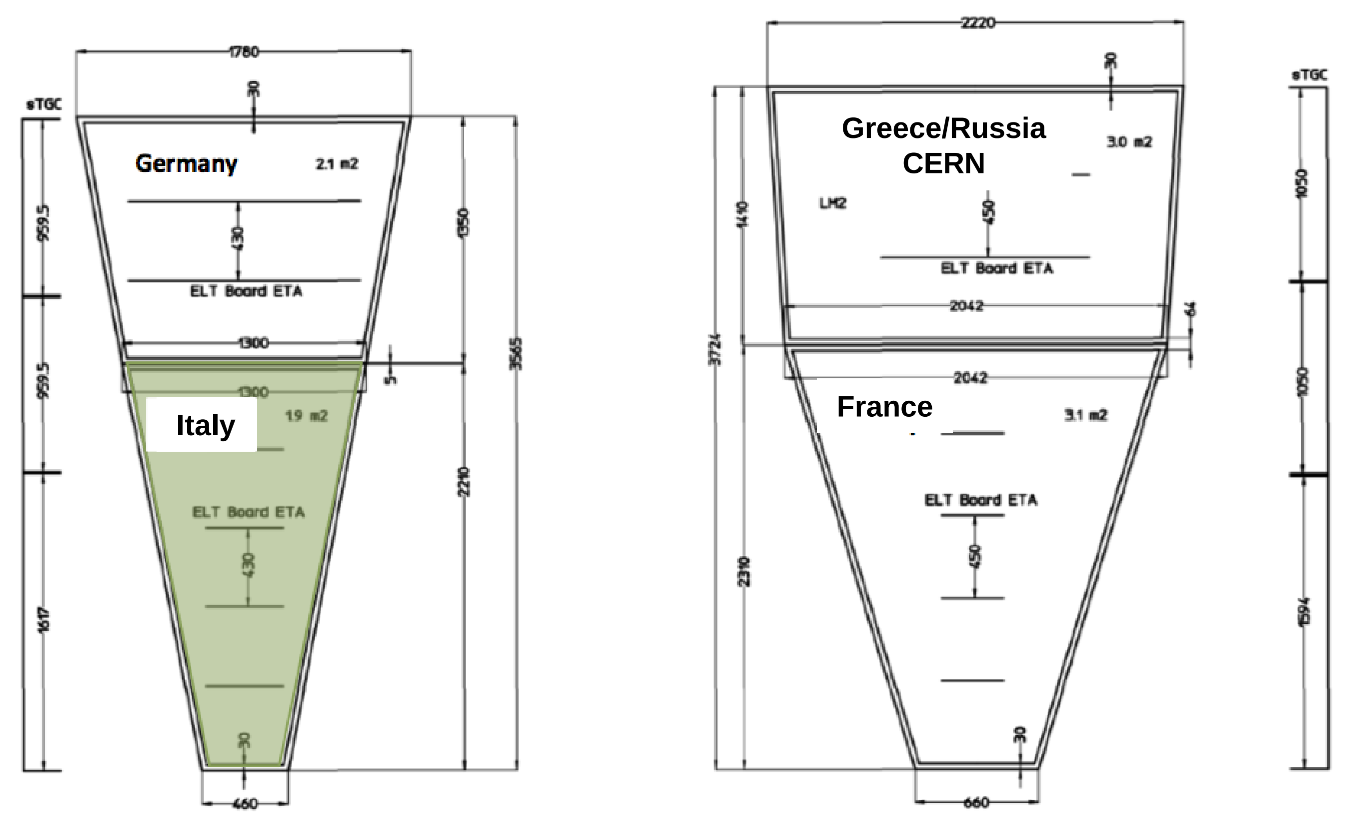


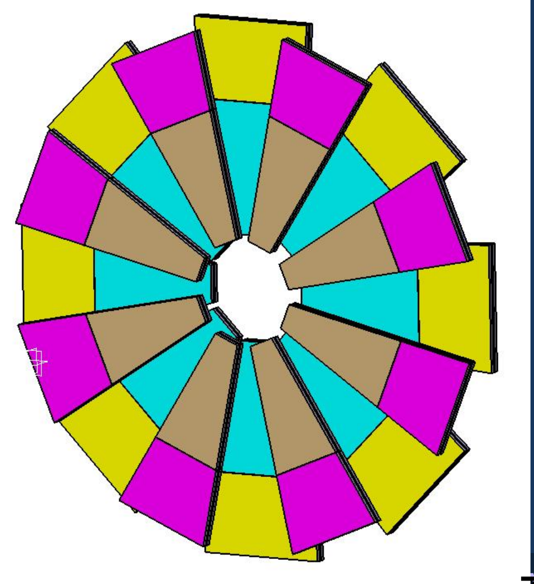
Micromegas Construction

- **<u>Mechanics & Electronics</u> is a multi-national operation; Mechanics: institutes from 6 countries, Electronics: Institutes from 10 countries (USA, Italy, Romania, Netherlands, Italy, Israel, Greece, France, Chile, Taiwan) -- Total: 30 Institutions are involved**

- **8 layers of Micromegas detectors will equip each large & small NSW sectors; for half of the layers, the strips will be under a stereo angle to measure the second coordinate.**

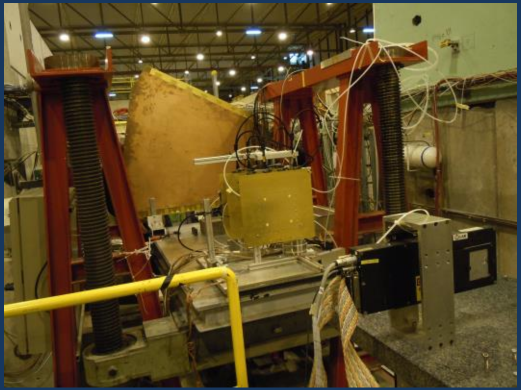
Total Surface	1200 m^2
Total number of MM Channels	2.1 M
Micromegas Strip Pitch	0.445 mm
Gas	Ar:CO_2 93:7 atm pressure
Drift Gap	5 mm
Amplification Gap	128 μm
HV on Resistive Strips	550 V
Drift Field	600 V/cm
Resistive Strips	10-20 MΩhm/cm
Stereo Strips on 4/8 Layers	1.5^o



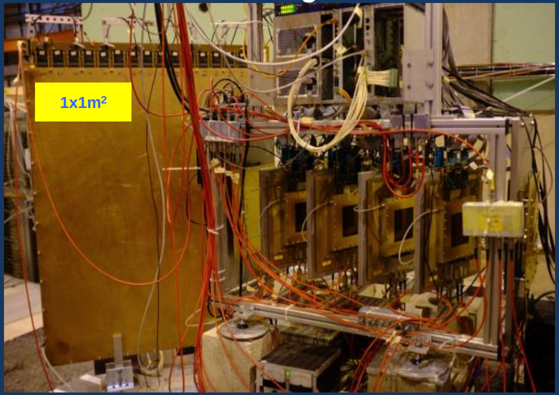


Full Micromegas Development Time-Plan

non-resistive MM, SPS/CERN, Demokritos-GR



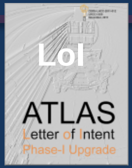
resistive MM, SPS/CERN, Demokritos-GR, Garching-GE



resistive MM, DESY II/DESY, LNF-IT, CEA-FR

2008 2009 2010 2011 2012 2013

developed new MM technology



LoI

ATLAS

Letter of Intent

Phase-I Upgrade

approved by ATLAS

TDR

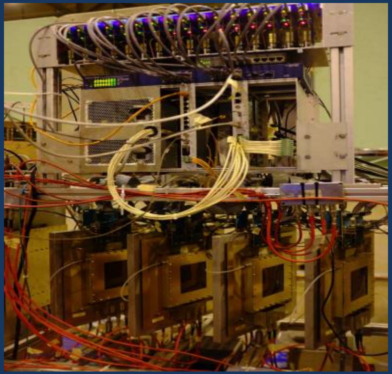
ATLAS

New Small Wheel

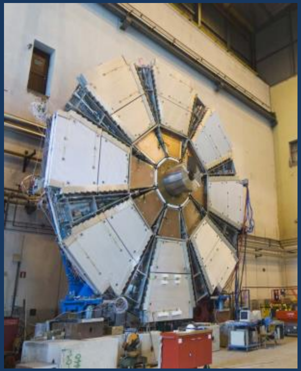
Technical Design Report

module-0 production & qualification

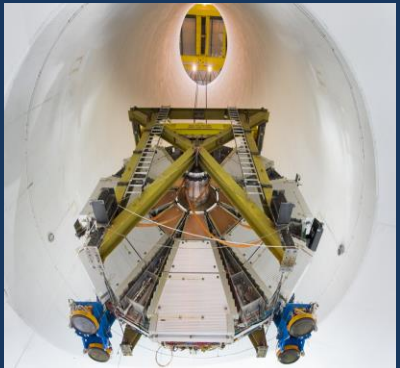
Full-production of chambers and electronics



Full commissioning on surface



Full installation in cavern

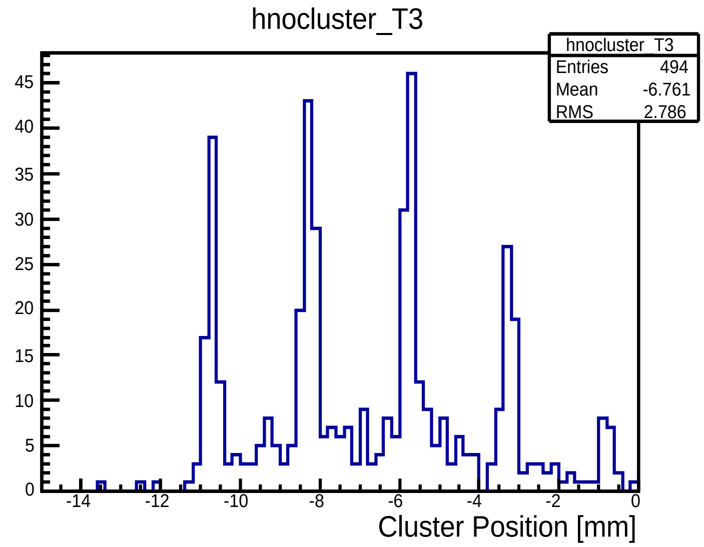


Running...

2014 2015 2016 2017 2018 2019

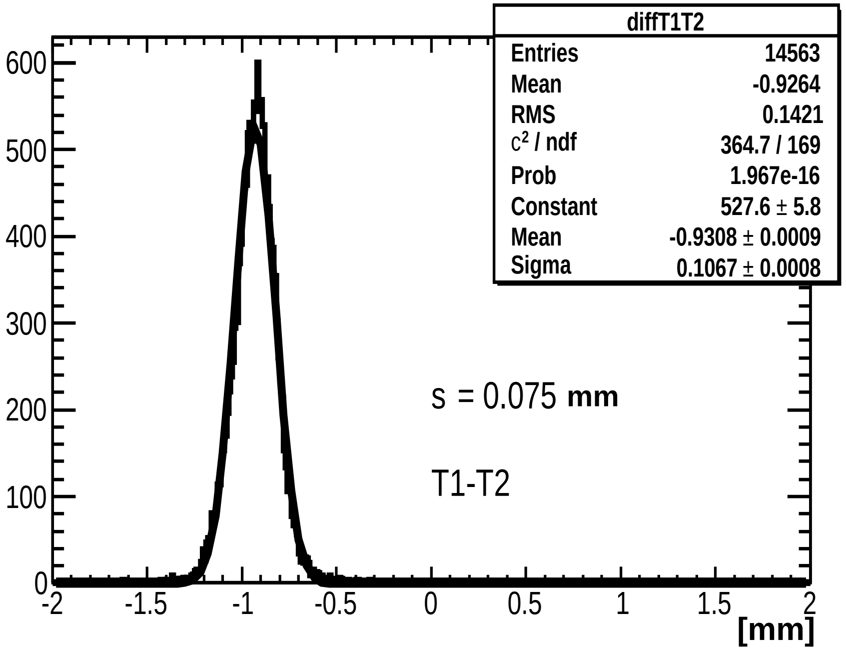
Efficiency & Spatial Resolution for Normal Tracks

Distribution of local inefficiencies as measured from the missing hits on one chamber corresponding to a reconstructed track from the other chambers.



Global inefficiencies of 2% consistent with the partially dead area due to the presence of 300**µ**m diameter pillars separated by 2.5 mm.

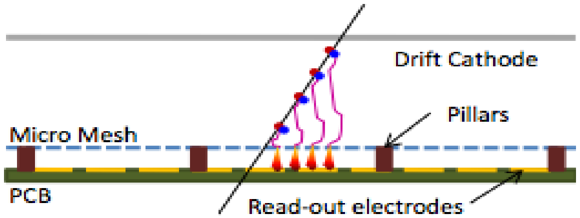
Spatial resolution for perpendicular tracks estimated by difference of cluster charge centroid measurements of pairs of MM chambers.



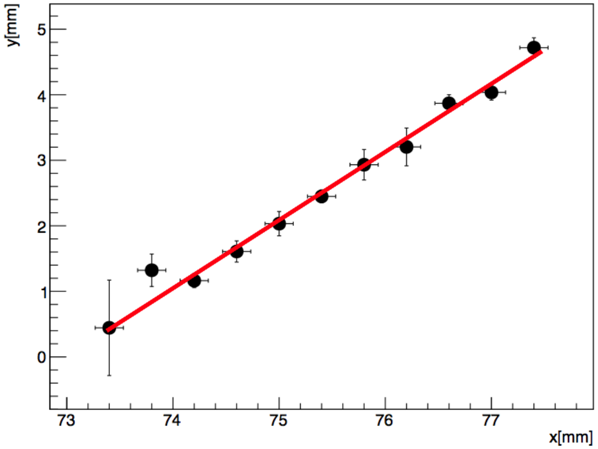
About **75 µm** with an average cluster size of 3.2 strips (400µm pitch).
Similar results obtained with a full track reconstruction method

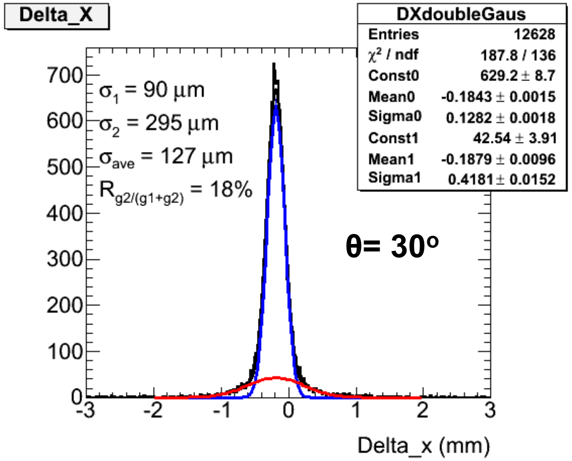
micro-TPC Mode for Incline Tracks

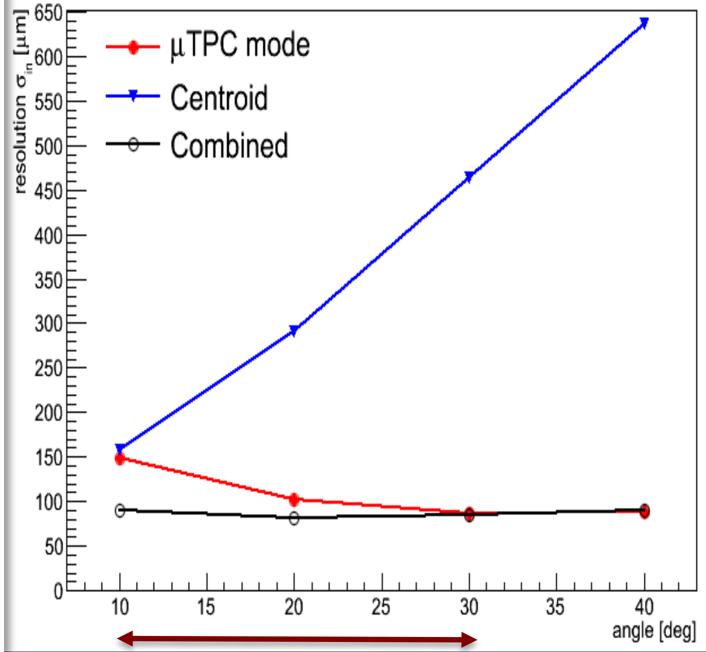
- **S**ub 100 **μ**m spatial resolution easy to achieve for perpendicular tracks
- For inclined tracks need to exploit time information to operate in micro-TPC mode



Single Segment Reconstruction in a Micromegas



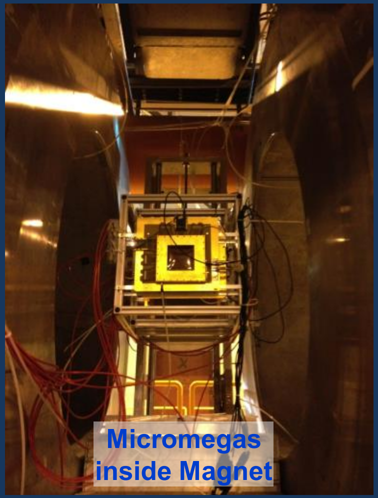


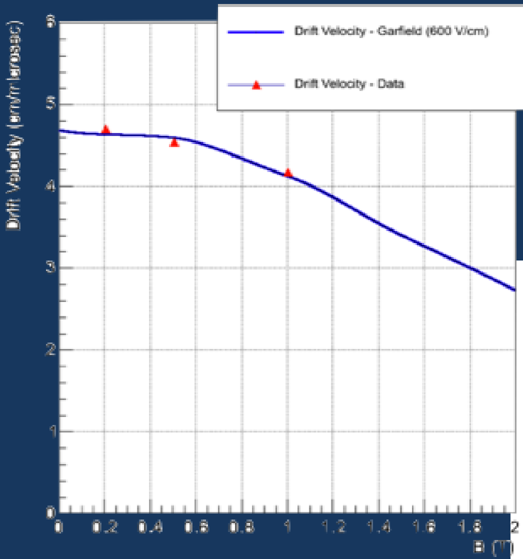


Muon angular range in NSW

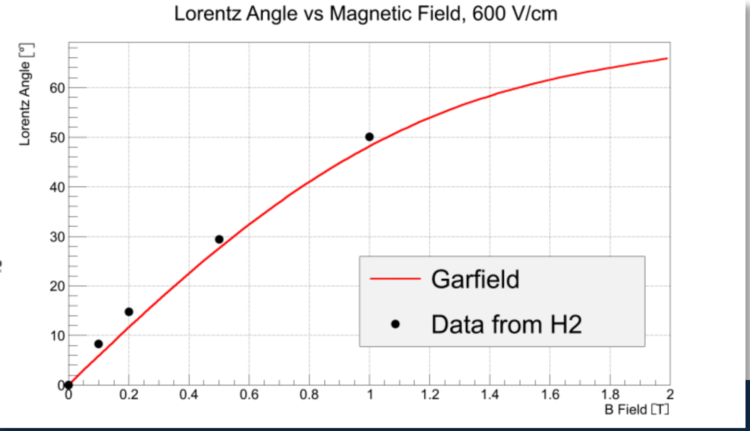
Micromegas Performance in *B*

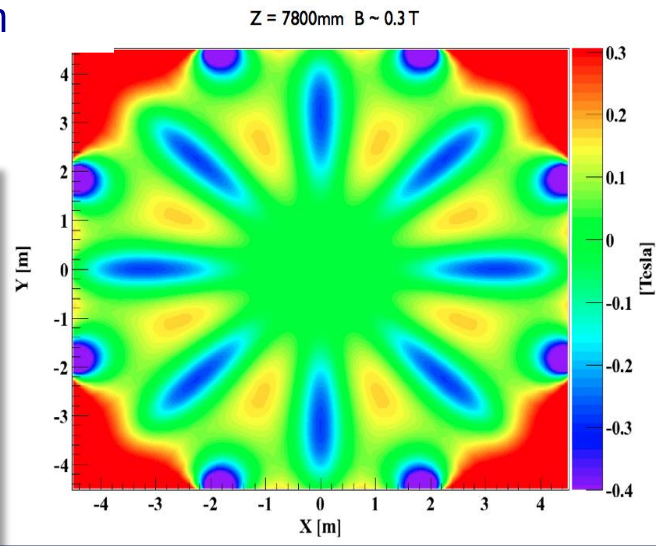
- **ATLAS New Small Wheels will be operated in a mixed directional *B* field up to 0.4 T.**
- **Micromegas chambers tested successfully in a magnetic field up to 1 T showing no performance degradation.**
- **Lorentz angle & drift velocity measurements are in agreement with simulation.**


Micromegas inside Magnet



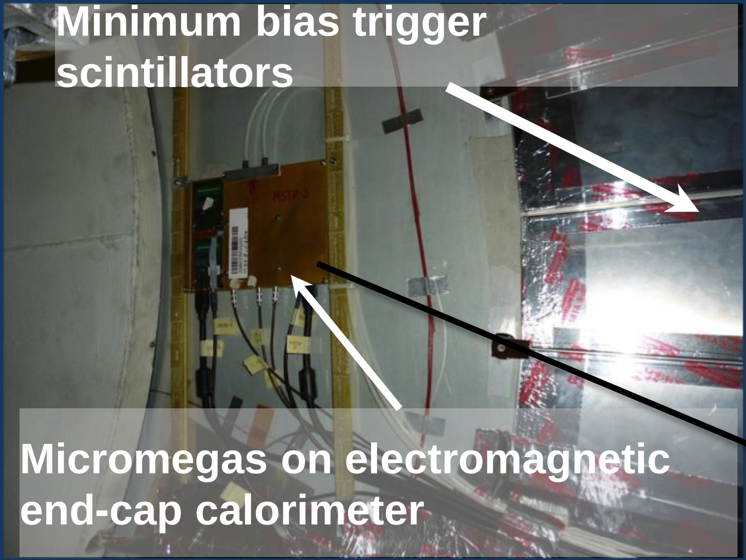
Lorentz angle from perpendicular tracks; E_{drift} = 600V/cm





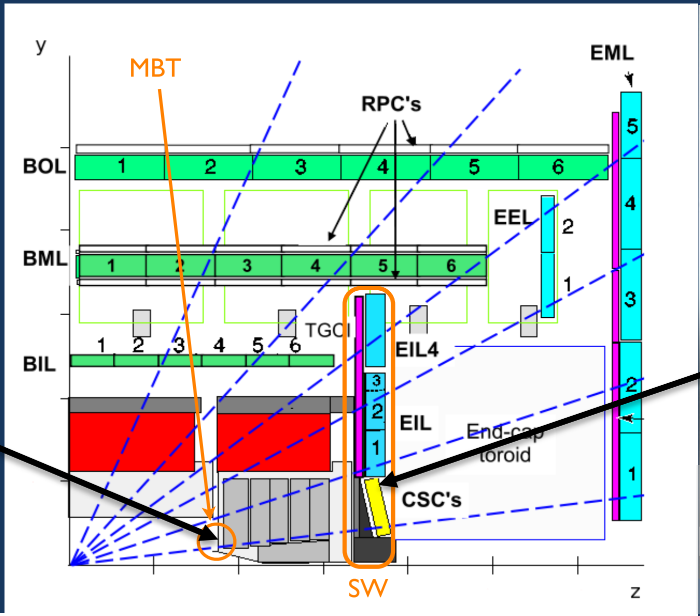
ATLAS End-Cap Toroid field

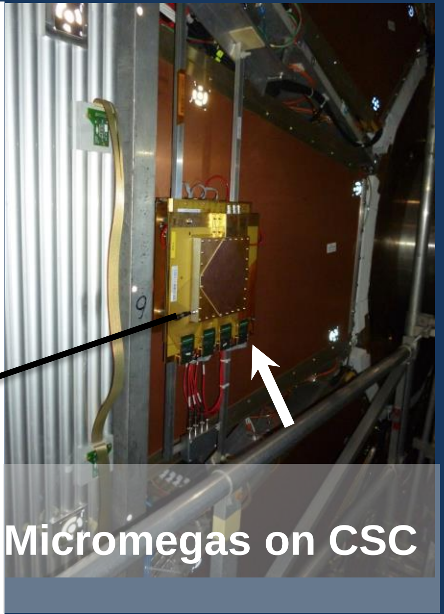
Micromegas Performance in ATLAS



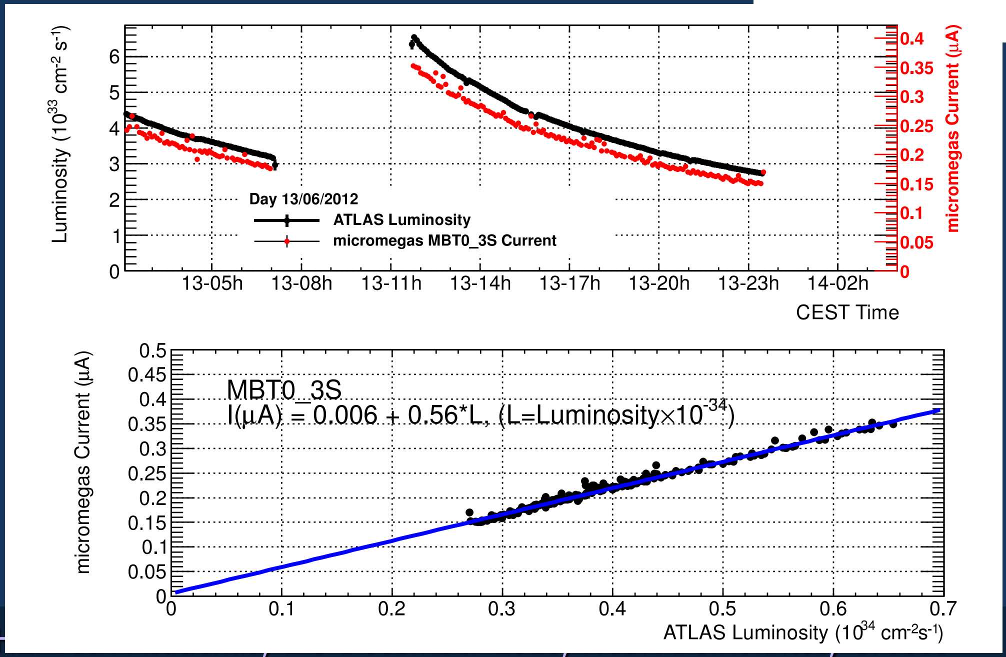
Minimum bias trigger scintillators

Micromegas on electromagnetic end-cap calorimeter

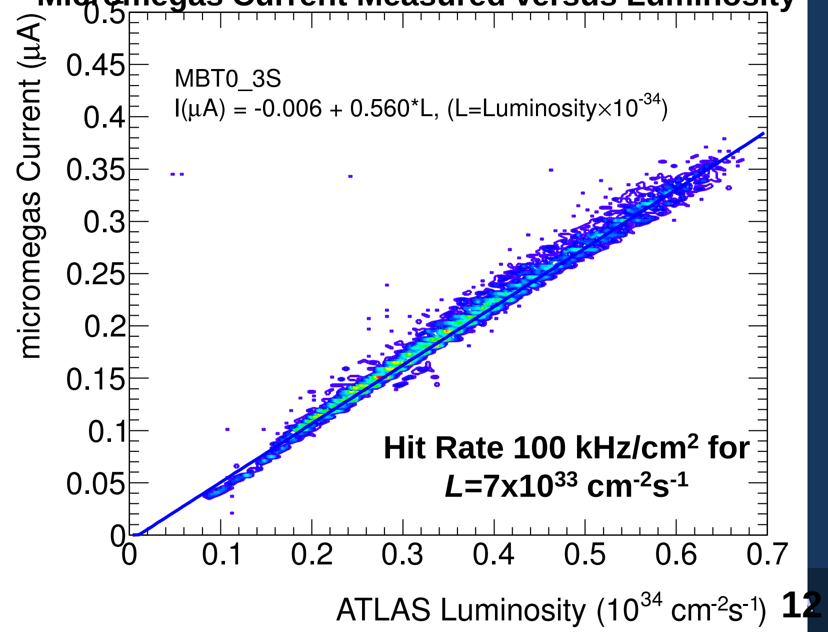




Micromegas on CSC



Micromegas Current Measured versus Luminosity

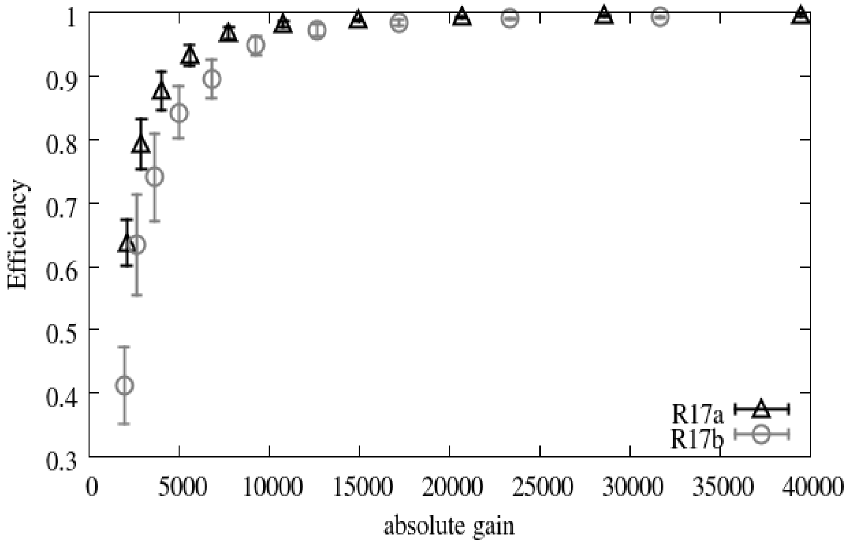


Hit Rate 100 kHz/cm^2 for $L=7\times10^{33}$ cm^{-2}s^{-1}

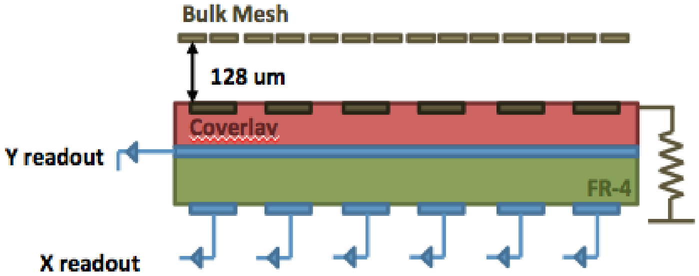
Ageing Performance Studies

Extensive program of irradiations on small prototype (10x10 cm^2) **performed** at C.E.A. Saclay, Orphee reactor,

Irradiation with	Charge Deposit (mC/cm^2)	HL-LHC Equivalent	Results
X-Ray	225	5 HL-LHC years equivalent	No evidence of ageing
Neutron	0.5	10 years HL-LHC years equivalent	No evidence of ageing
Gamma	14.84	10 years HL-LHC years equivalent	No evidence of ageing
Alpha	2.4	5 x 10^8 sparks equivalent	No evidence of ageing



Both detectors reach efficiencies of about 99.5% for the highest values of the gain, proving that there is no visible degradation effect in these measurements



R17a detector is exposed to different radiation sources

R17b detector is kept unexposed.

- Gain control measurements are performed before and after each exposure.
- After the ageing both detectors are taken to the SPS/CERN.
- The goal to accumulate an integrated operation charge equivalent to the one would be obtained at the HL-LHC for 10 years for each type of radiation.

Performance evaluated in terms of **efficiency** and **spatial resolution**

Components of NSW DCS

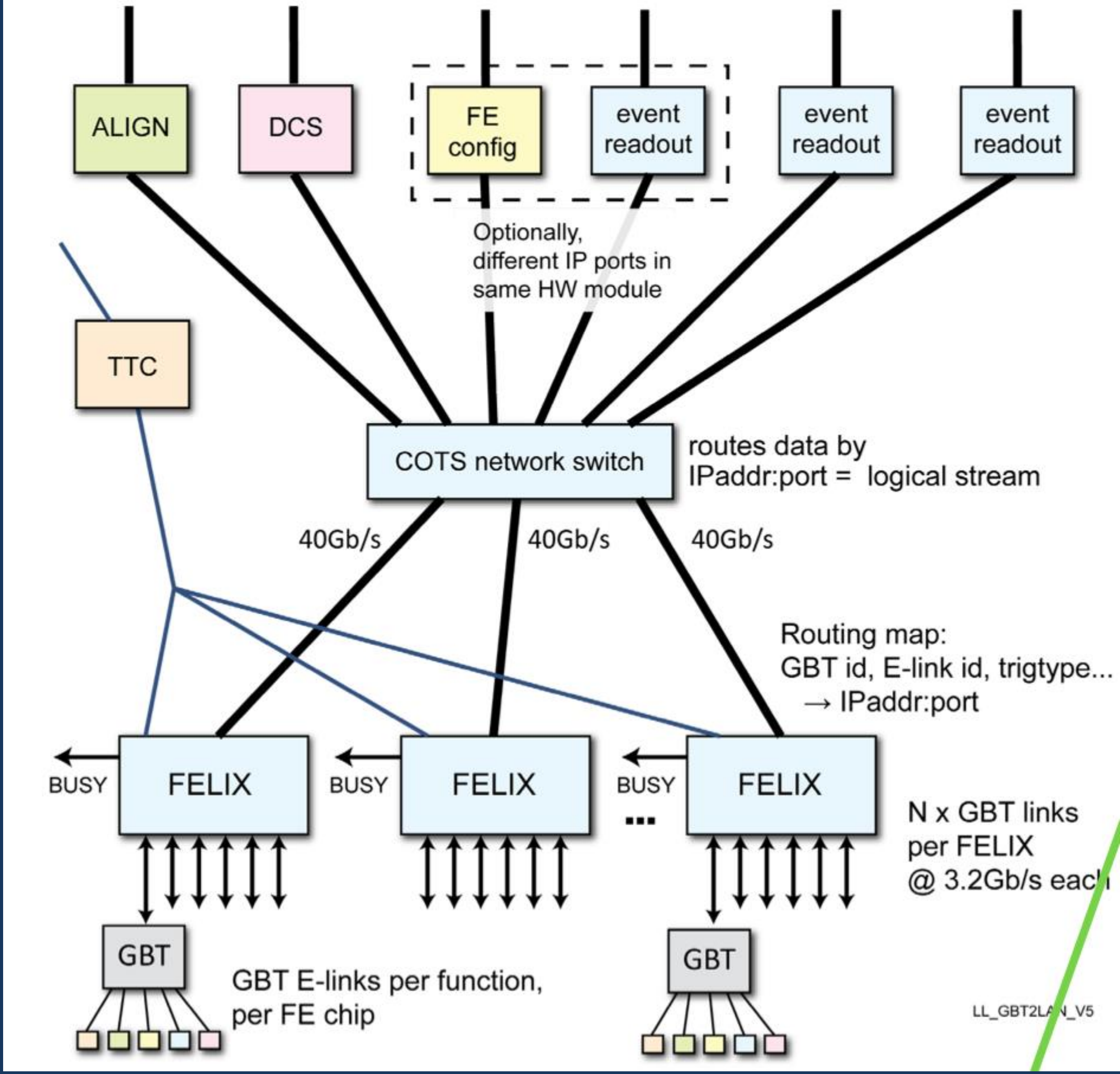
- *T, B, HV/LV,* **gas, alignment,**

- **ELMB++**

- **Monitor DC-DC converters**
- **Monitor Front End ASICs VMMx, V_{ref}, …**
- **Monitor/Configuration companion ASIC on FrontEnd Boards**
- **Configuration/Status of VMMx**
- **Calibration VMMx**

- **propose to use the GBT-SCA ASIC**

New Small Wheel Proposed Readout



DCS: Detector Control System

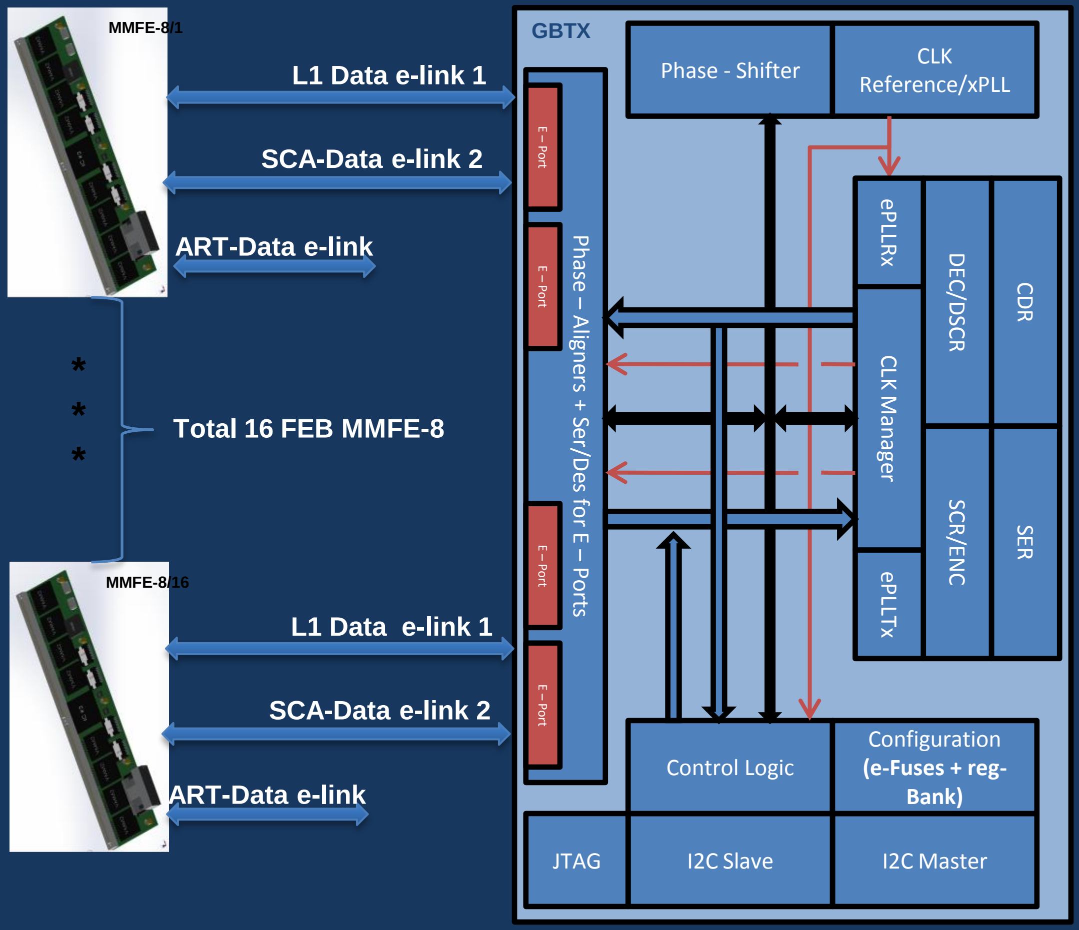
TTC: Timing, Trigger and Control

FELIX: Front End Link eXchange

GBT: Gigabit Transfer ASIC

New Small Wheel DCS

Front End Boards



MMFE-8/1

L1 Data e-link 1

SCA-Data e-link 2

ART-Data e-link

*
*
*

Total 16 FEB MMFE-8

MMFE-8/16

L1 Data e-link 1

SCA-Data e-link 2

ART-Data e-link

GBTX

Phase - Shifter

CLK Reference/xPLL

E – Port

E – Port

E – Port

E – Port

Phase – Aligners + Ser/Des for E – Ports

ePLLRx

DEC/DSCR

CDR

CLK Manager

ePLLTx

SCR/ENC

SER

Control Logic

Configuration **(e-Fuses + reg-Bank)**

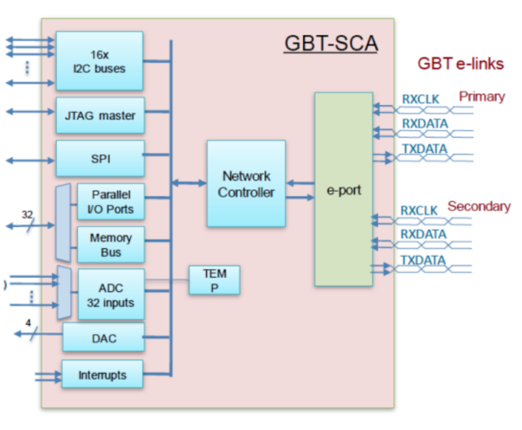
JTAG

I2C Slave

I2C Master

GBT-Slow Control Adapter (SCA) ASIC

- Slow Control Adapter (GBT–SCA) ASIC suitable for the control and monitoring applications of the embedded front-end electronics
- Interfaces with the GBTX using a dedicated E-link port (Standard e-Ports in the 80 Mb/s can be used as well)
- Is intended for the slow control and monitoring of the embedded front end electronics and implements a point-to-multi point connection between one GBT optical link ASIC and several front end ASICs
- More than one GBT-SCA ASIC can be connected to a GBT ASIC thus increasing the control and monitoring capabilities in the system
- There are 16 I2C buses, 1 JTAG controller port, 4 8-bit wide parallel-ports, a memory bus controller and an ADC to monitor external analog signals
- Implements environment monitoring functions: Temp sensing



Specs:

- **16 I^2C master controllers, @100kbits/s to 1 Mbits/s.**
- **1 JTAG & 1 SPI master controller**
- **32 multiplexed ADC channels, 12-bit dual slope, 1-occupied by the temp sensor**
- **4 DAC channels**
- **32 Digital I/O lines individually programmable**

Link Architecture

Radiation tolerant chipset:

- GBTIA: Transimpedance optical receiver
- GBLD: Laser driver
- GBTX: Data and Timing Transceiver
- GBT-SCA: Slow control ASIC

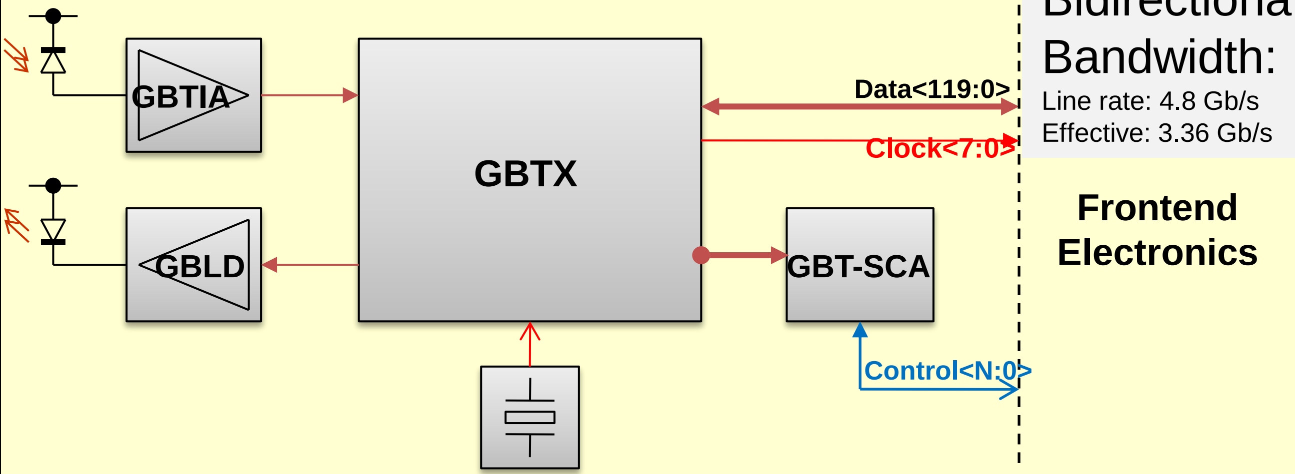
Supports:

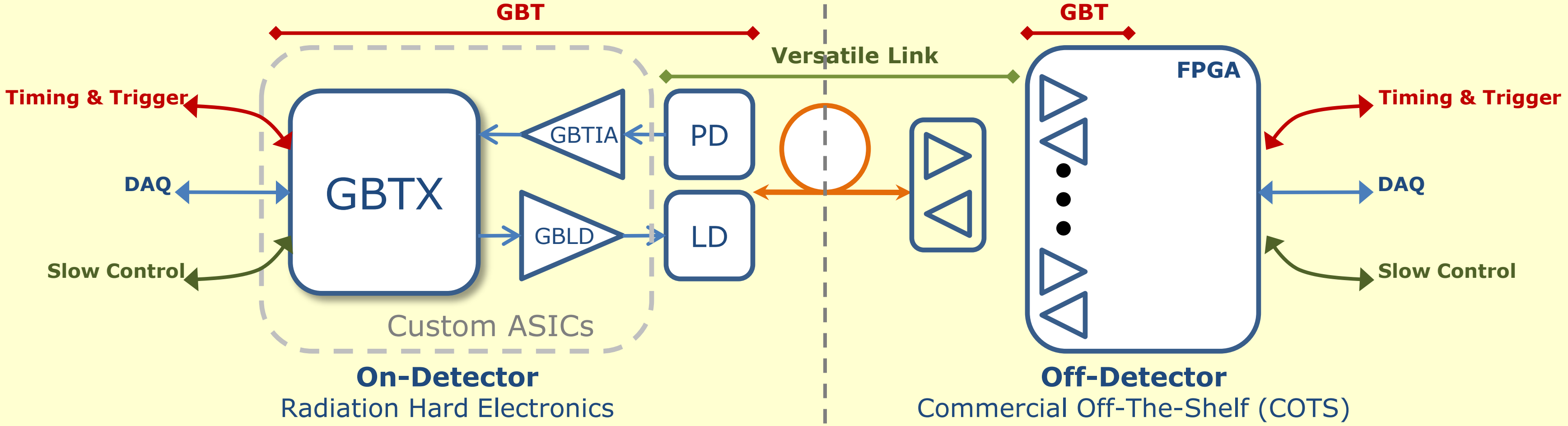
Bidirectional data transmission

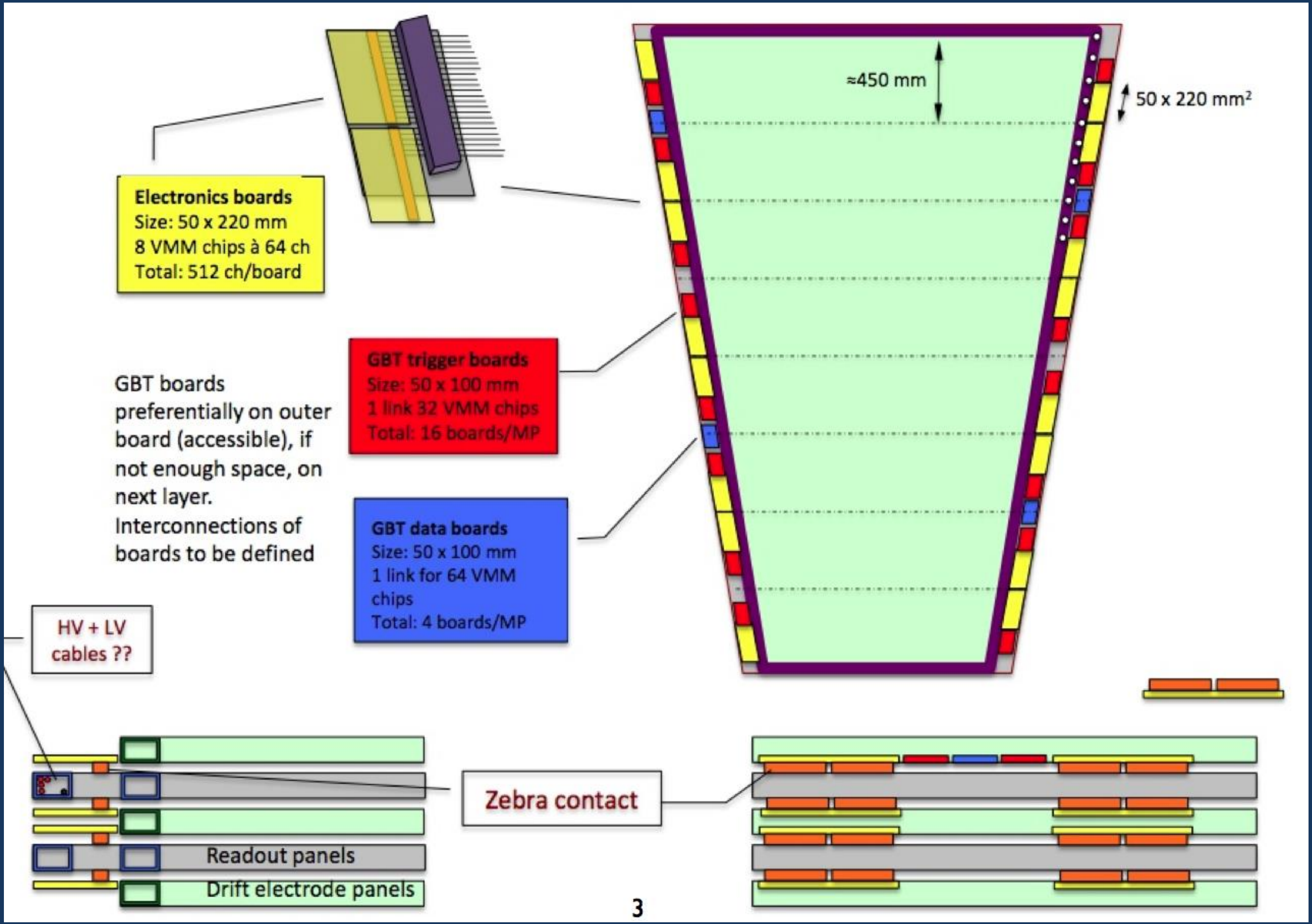
Bandwidth:

Line rate: 4.8 Gb/s

Effective: 3.36 Gb/s







Electronics boards
Size: 50 x 220 mm
8 VMM chips à 64 ch
Total: 512 ch/board

GBT trigger boards
Size: 50 x 100 mm
1 link 32 VMM chips
Total: 16 boards/MP

GBT data boards
Size: 50 x 100 mm
1 link for 64 VMM chips
Total: 4 boards/MP

GBT boards preferentially on outer board (accessible), if not enough space, on next layer.
Interconnections of boards to be defined

1GBT/plane serves 16 FEB/plane
4GBT/MP x 2MP/sector x 32 sectors/MM = 256 GBT/MM Readout boards & 384 GBT/sTGC and 1024 GBT trigger boards

Summary

- Will continue using the highly distributed control system based on SCADA software WinCC OA
- A heavy & intense NSW upgrade program ahead of us!
- We are evaluating the optimal solution for NSW DCS