AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Development of front-end electronics for future LC at AGH-UST

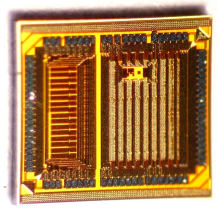
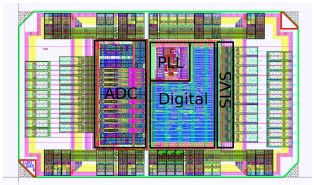
M. Firlej, T. Fiutowski, M. Idzik, **Sz. Kulis**, J. Moroń, D. Przyborowski, K. Świentek

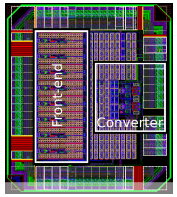
Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

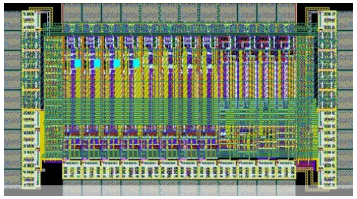
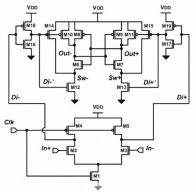
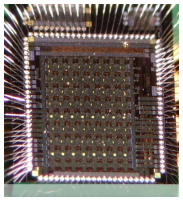
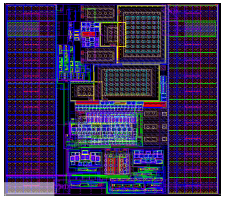
CLIC Workshop 2014
04/02/2014 CERN

Outline

- Introduction and motivation
  - Readout architecture (examples: Linear Colliders, LHCb upgrade)
- ASICs R&D
  - Front-end (LumiCal, SALT, CLIC)
  - ADC (fast sampling SAR ADCs)
  - Multichannel system aspects (MUX, PLL, etc...)
- Summary

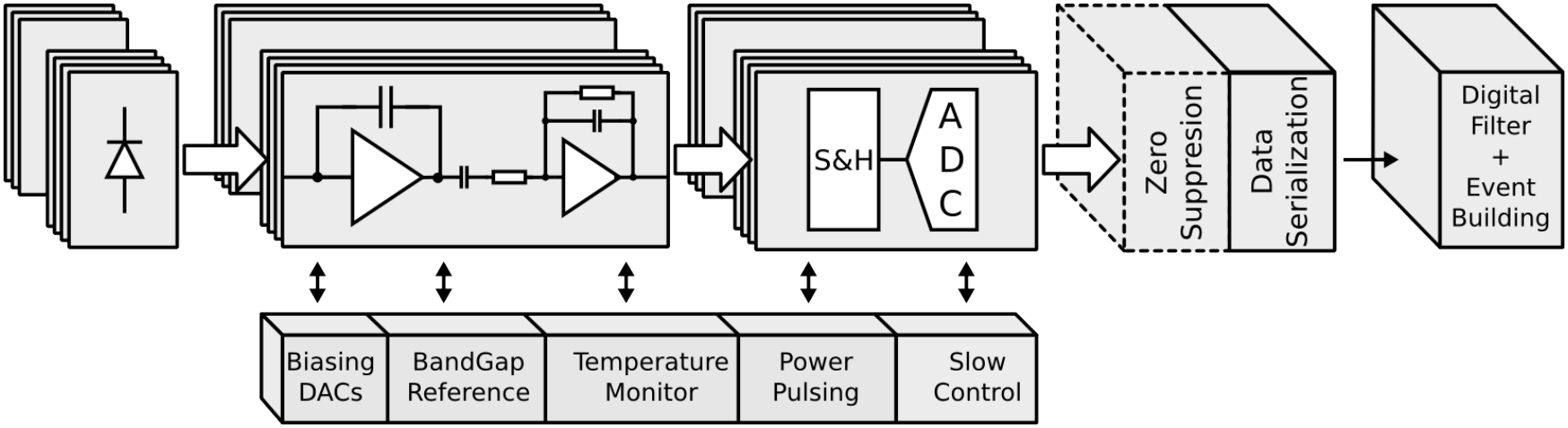





Disclaimer: this talk will focus mainly on (micro)electronics

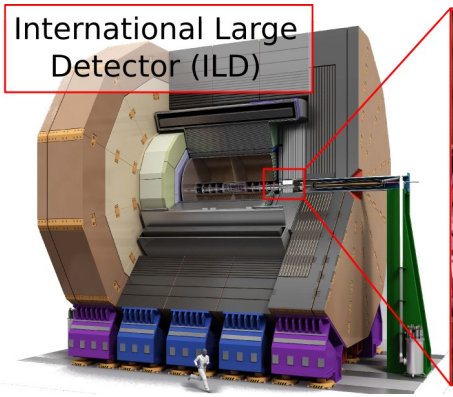
Introduction
Readout architecture

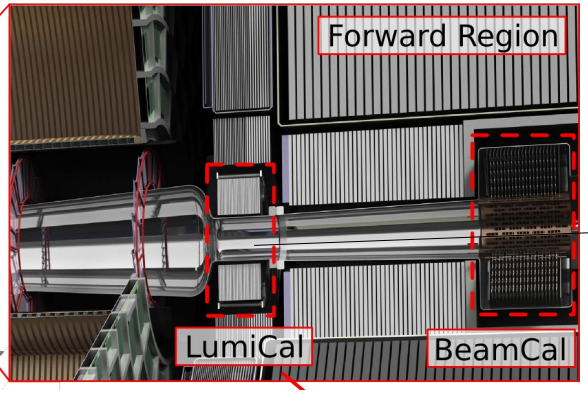


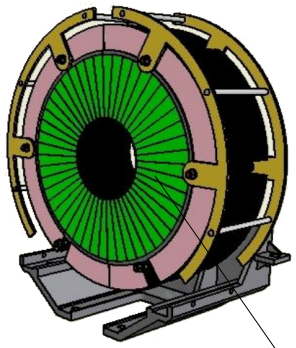
- This architecture is well suited for high rate systems requiring **time and amplitude measurement** *(forward regions of CLIC detector, LHC upgrade)*
- Why this type or architecture was not feasible in the past ?
  → in older technologies, power consumption of fast ADC was too high to place ADC in each readout channel

Introduction
Readout electronics of Luminosity calorimeter for future Linear Collider

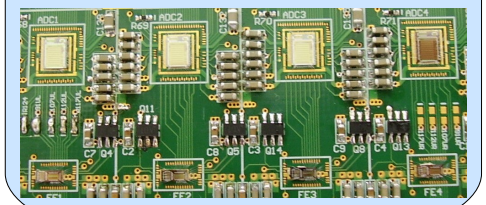
LumiCal detector will contain 30/40 layers of sandwich Si-W calorimeter (more than 200k channels)

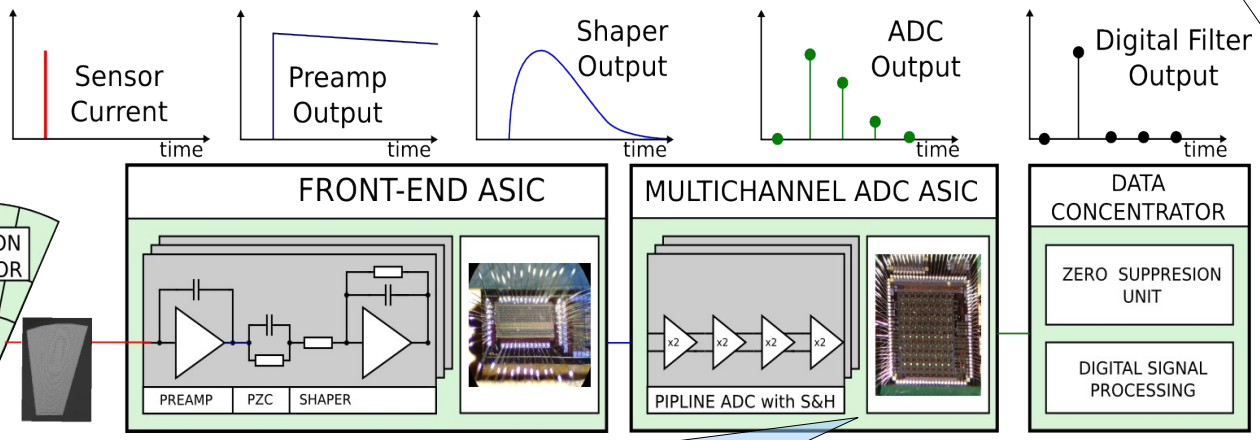






4 pairs of Front-end + ADC

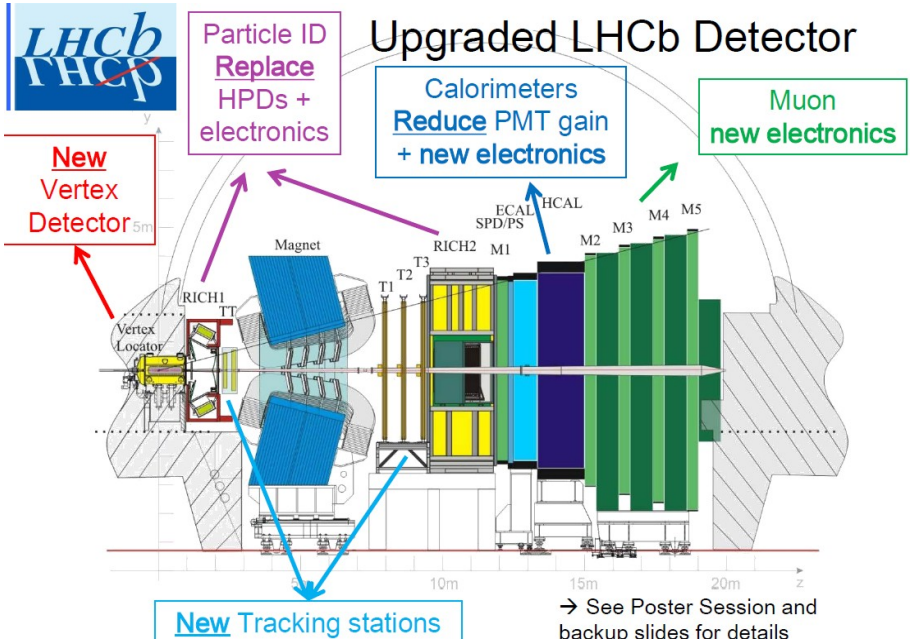




1st Prototypes of 8-channel front-end and ADC ASICs were designed and produced in AMS 0.35µm CMOS.

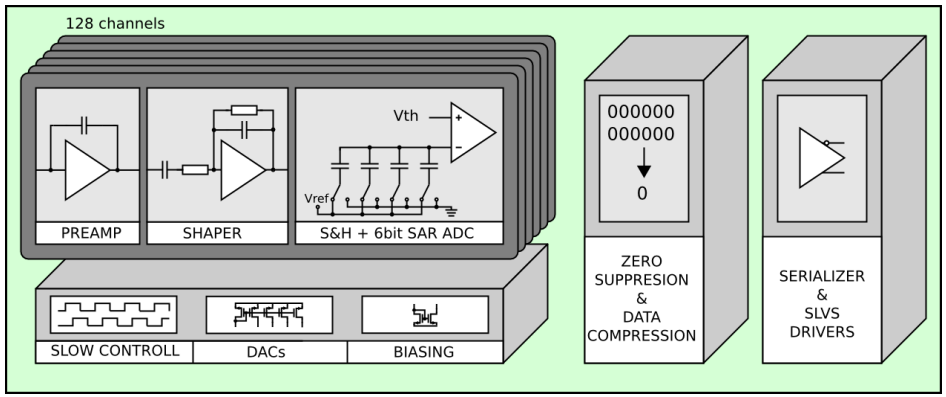
Testbeam validated!

Introduction
LHCb Tracker System Upgrade



Motivation: Increase trigger rate from 1 MHz to 40 MHz
→ **new readout electronics** needed in LHCb Upstream Tracker System (present TT - Trigger Tracker)

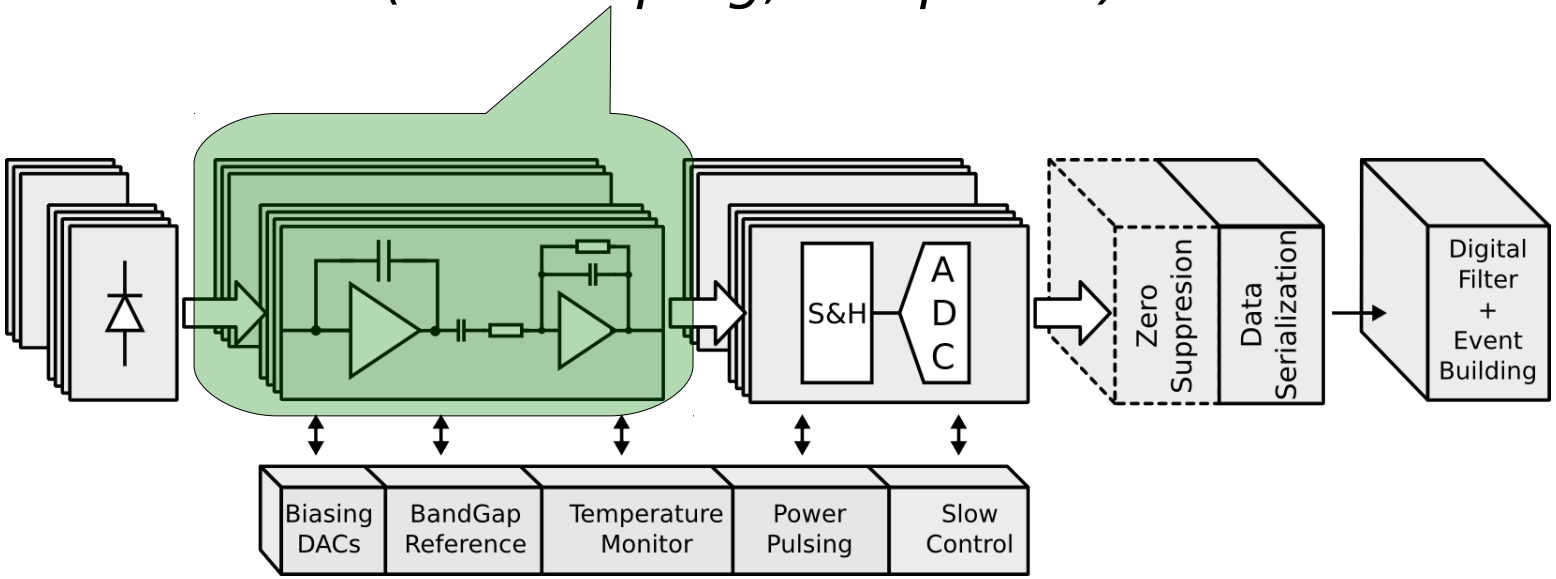
Complex System on Chip (SoC) ASIC



- 128 channels
- Preamplifier-shaper, 6-bit ADC, zero supp., serialization, fast data transmission
- CMOS 130 nm CMOS technology

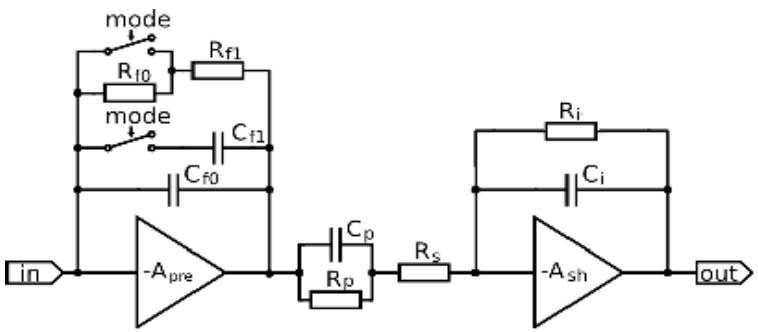
Front-end ASICs

(fast shaping, low power)

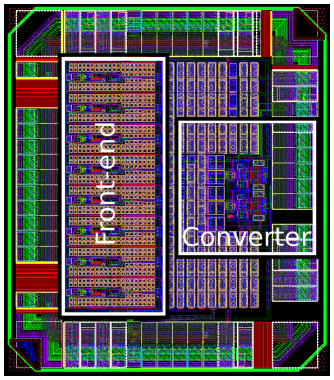


Front-end
LumiCal front-end in CMOS 130 nm

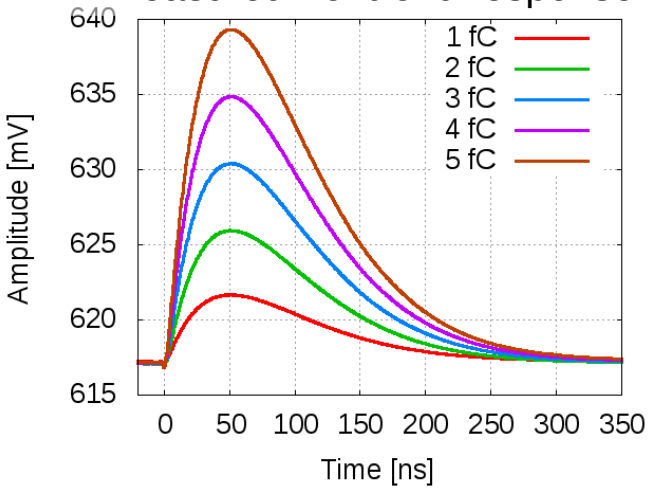
Channel schematic diagram



Layout



Measured front-end response



Design specs:

- 8 channels
- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain:
  - calibration mode - MIP sensitivity
  - physics mode - input charge up to ~5 pC
- Power pulsing implemented
- Power consumption ~1.5 mW/channel

Very Preliminary Measurements:

- Fully functional
- Tpeak ≈ 51 ns
- Calibration mode @10pF:
  - gain 4.1 mV/fC
  - linear range ~60 fC
  - ENC 930 e-
- Physics mode @10pF
  - gain 105 mV/pC
  - Linear range ~2.7 pC (saturates >5pC)

Front-end
Shaper design for lowest pileup (LHCb driven)

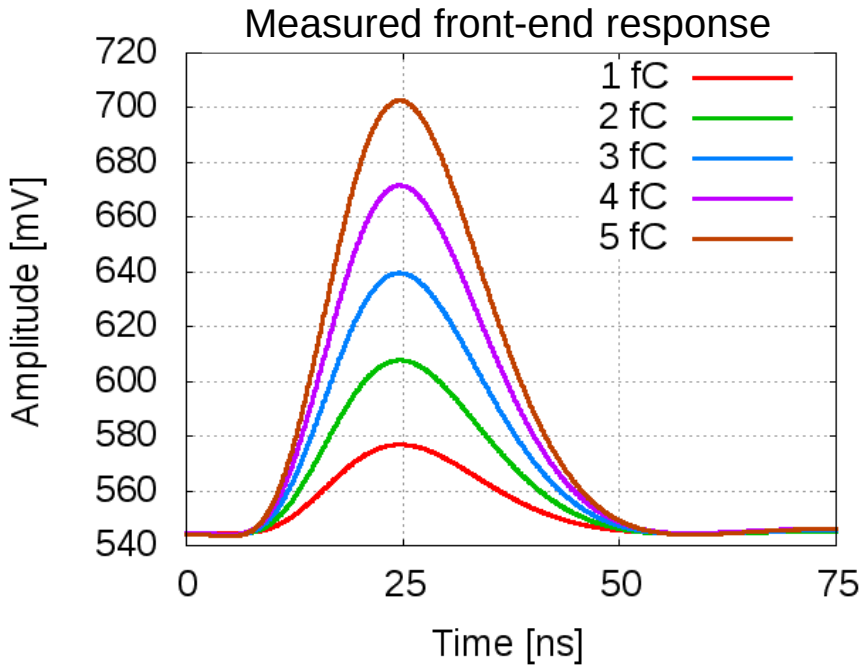
Is it possible, with realistic shaper complexity and power consumption, to shorten a pulse tail to less than 5% of pulse amplitude after 2*T_{peak} ?

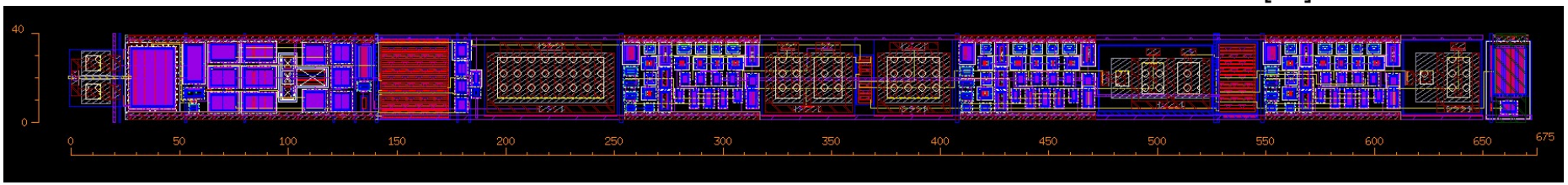
... it seems possible

Main front-end features of the prototype:

- Architecture: Preamplifier, PZC, 3-stage shaper
- Preamplifier: NMOS input cascode with boosting amplifiers
- Shaper: with **complex poles and zeros**
- T_{peak} : **~ 25ns**
- C_{det} : **5-35 pF**
- Power cons.: **< 1.9 mW**

May be **interesting for high occupancy** (more than one hit per channel per bunch train) **CLIC detector regions**

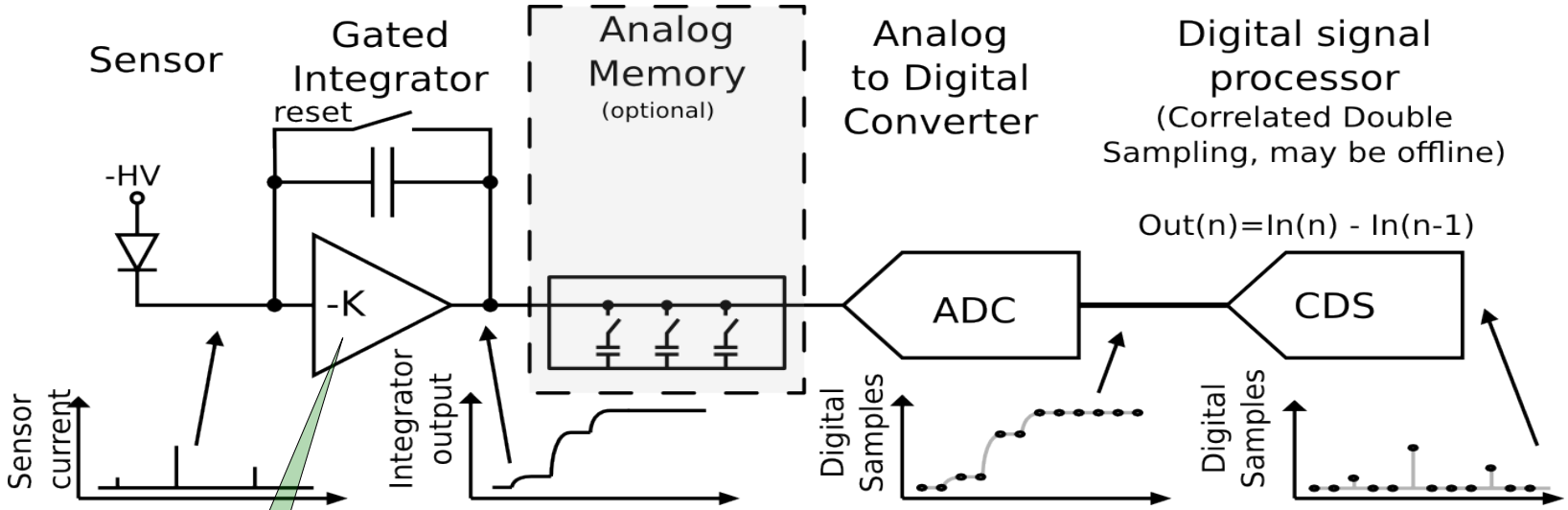


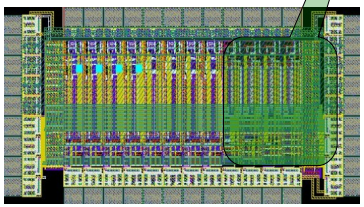


Front-end

Gated integrator – good candidate for CLIC high occupancy regions ?

- Simplest possible shape (step) will allow amplitude information reconstruction even in case of high occupancy
- Time resolution of single event tagging limited by
  rise time of preamplifier and ADC sampling frequency

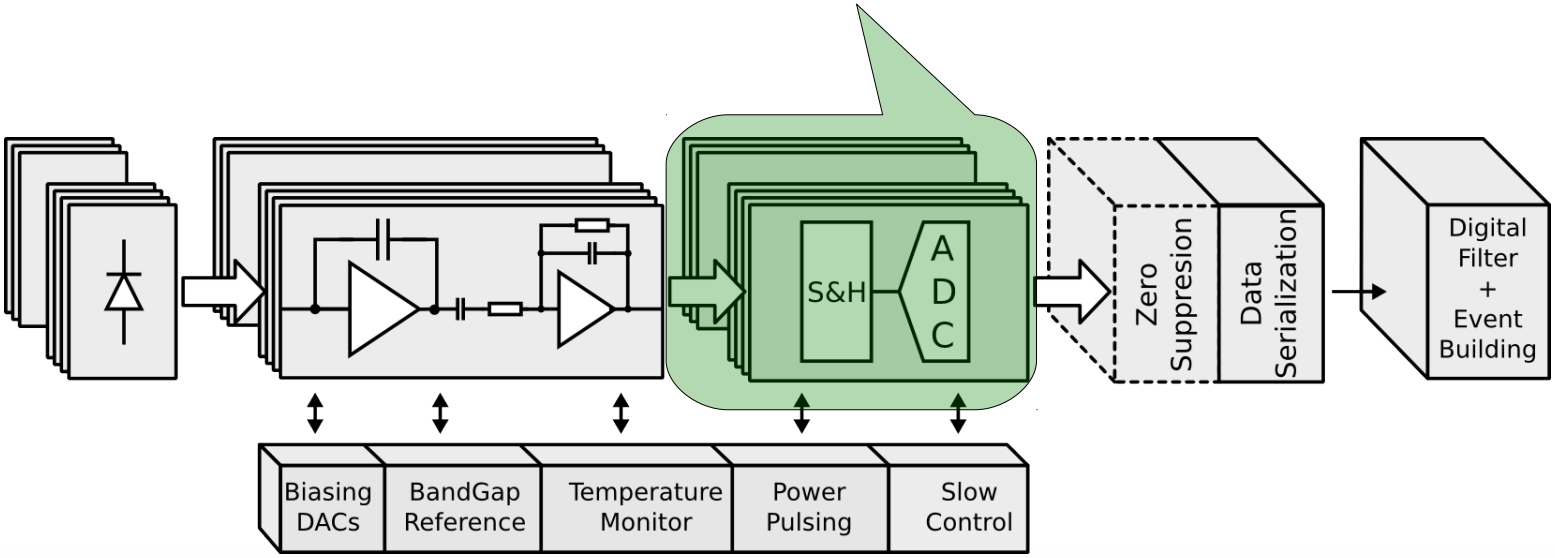




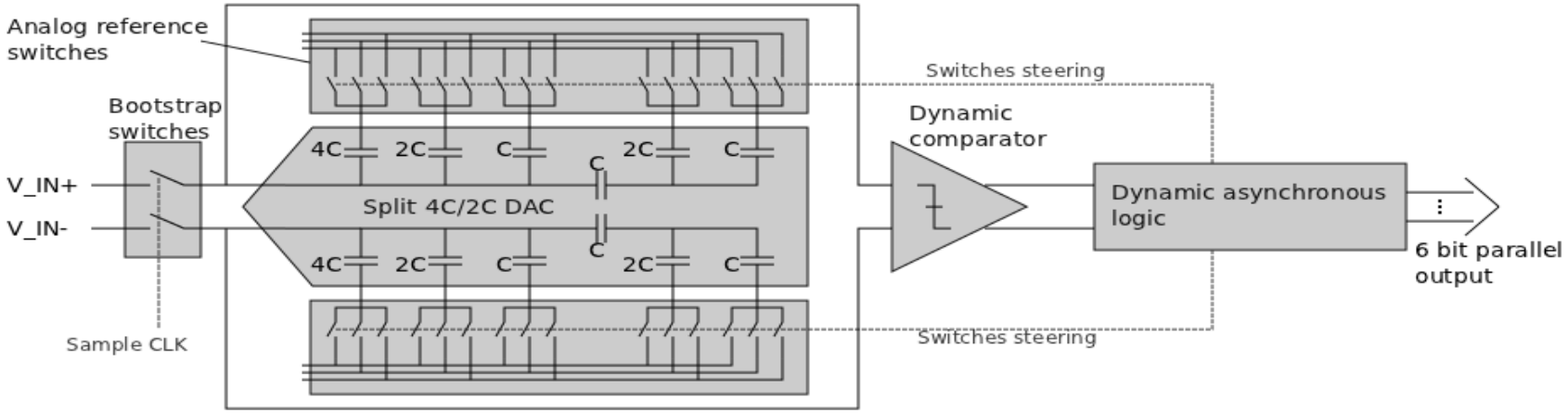
We have a simple prototype with can be used to verify this concept

Analog-to-Digital converters

(low power, high sampling frequency)



SAR ADC
Architecture&Design considerations

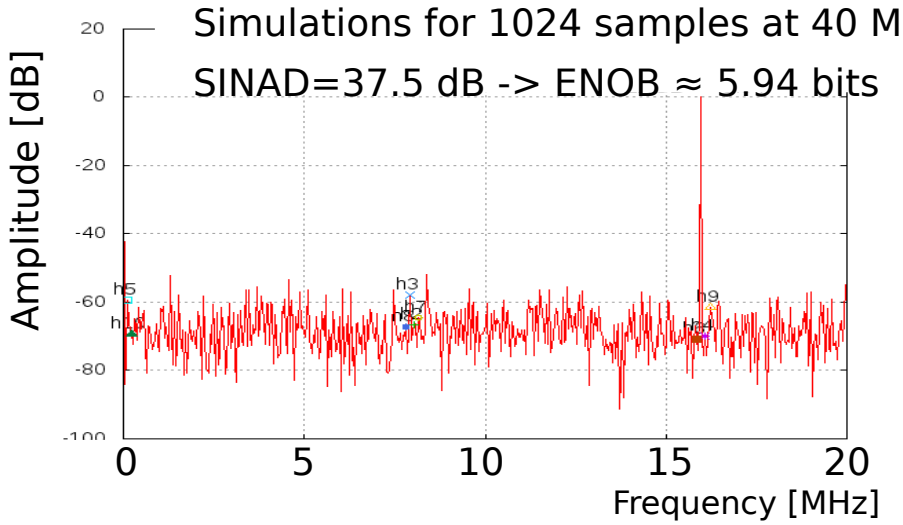


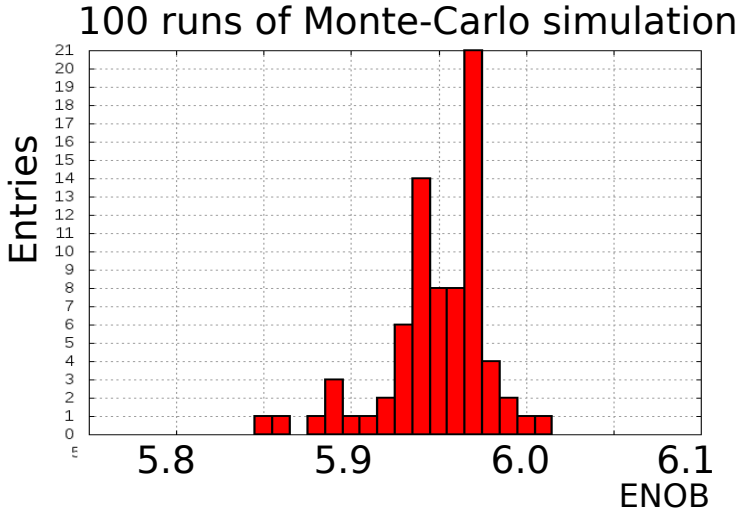
Architecture of ADC:

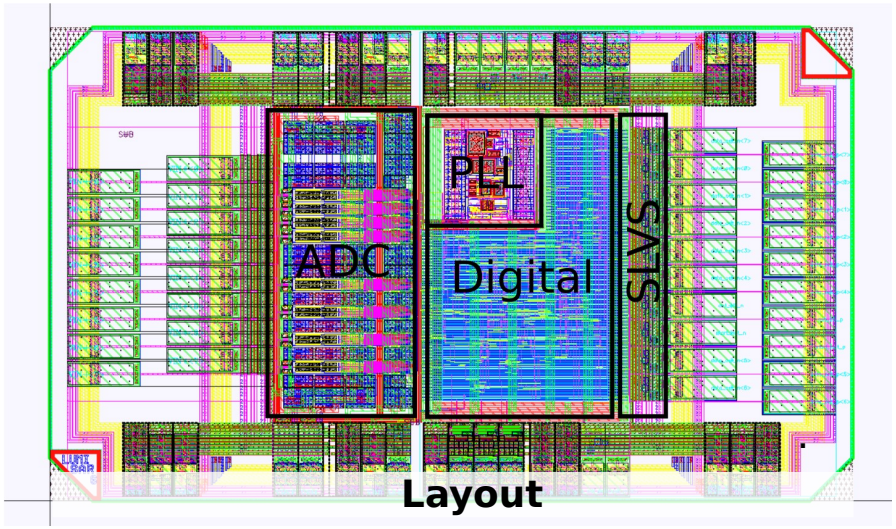
- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***

Design considerations:	**LHCb upgrade**	**LumiCal**
• Resolution	6 bits	10 bits
• Variable sampling frequency	up to ~90 MS/s	up to ~50 MS/s
• Power consumption at 40 MS/s	**~0.35 mW**	**~1 mW**
• pitch, ready for multichannel integration	40 µm	146 µm

6-bit SAR ADC for LHCb uprgade
Importance of post-layout simulations







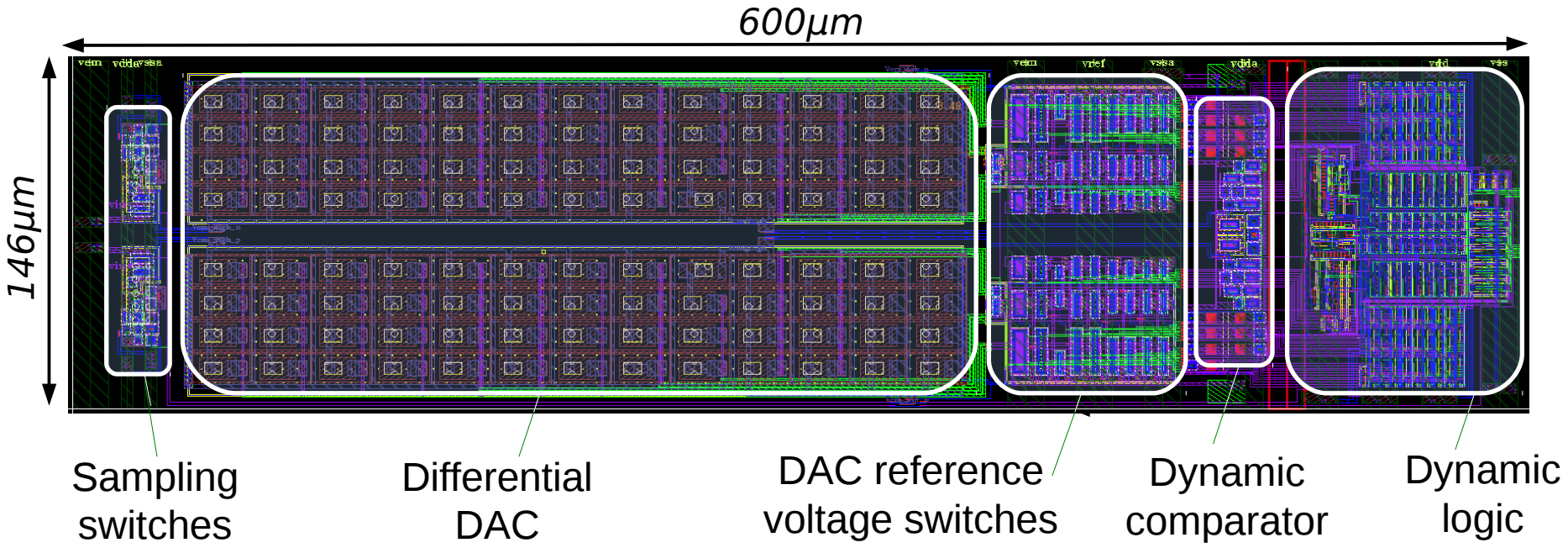
Simulated ADC performance:

- Simulated ENOB **>5.8 bits**
- Maximum sampling rage **~ 90 MS/s**
- Power consumption ~ **0.35 mW @ 40 Ms/s**

ADC prototype contains:

- 8 channels of 6-bit SAR ADC in **40µm pitch**
- Multiplexing&Serialization circuitry
- PLL prototype (discussed later...)
- SLVS I/O circuitry

10-bit SAR ADC for Lumical



Simulated performance of 10 bit ADC:

- Simulated ENOB ~ **9.5-9.7 bits**
- Maximum sampling rate **~50 MS/s**
- Power consumption ~ **1mW @ 40 MS/s**

ADC prototype contains:

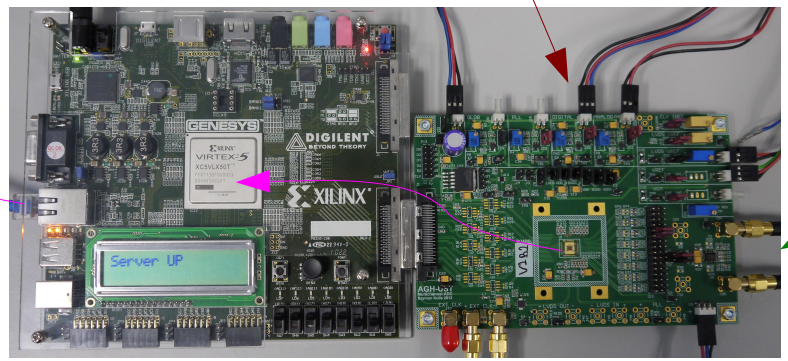
- 8 channels of 10-bit SAR ADC in **146µm pitch**
- Multiplexing&Serialization circuitry
- PLL prototype (discussed later...)
- SLVS I/O circuitry

ADC testing
Measurement setup

DFT and data analysis – custom software

Power supply

Differential function generator – Agilent 81160A



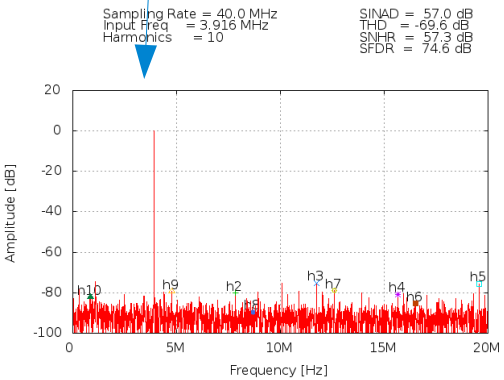
Input sine

Sample clock

Results

Sampled data (**low bitrate**)

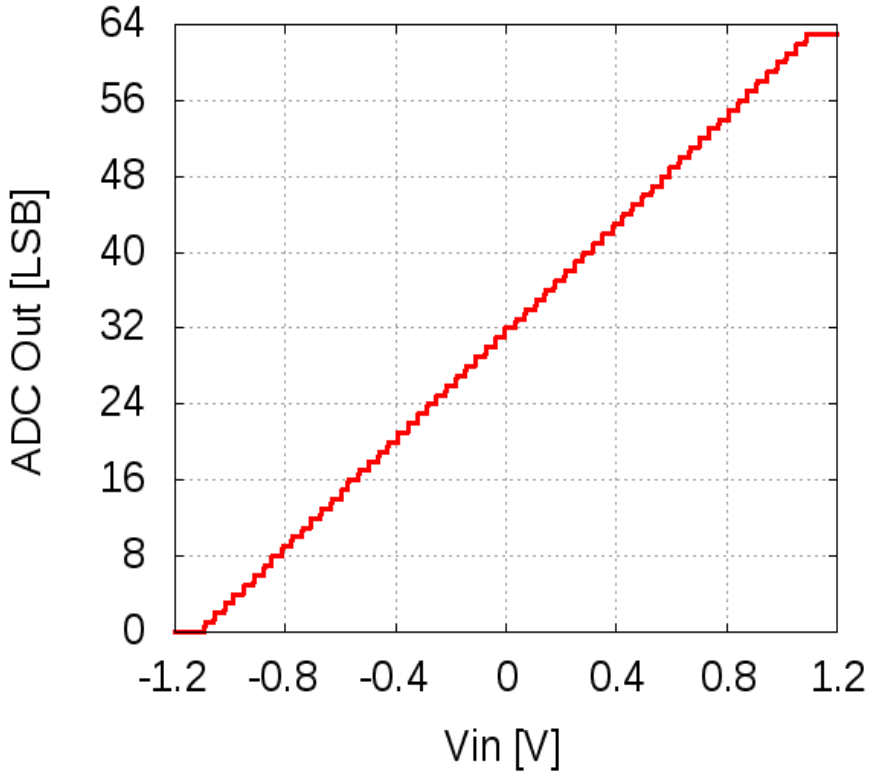
Sampled data (**high bitrate**)



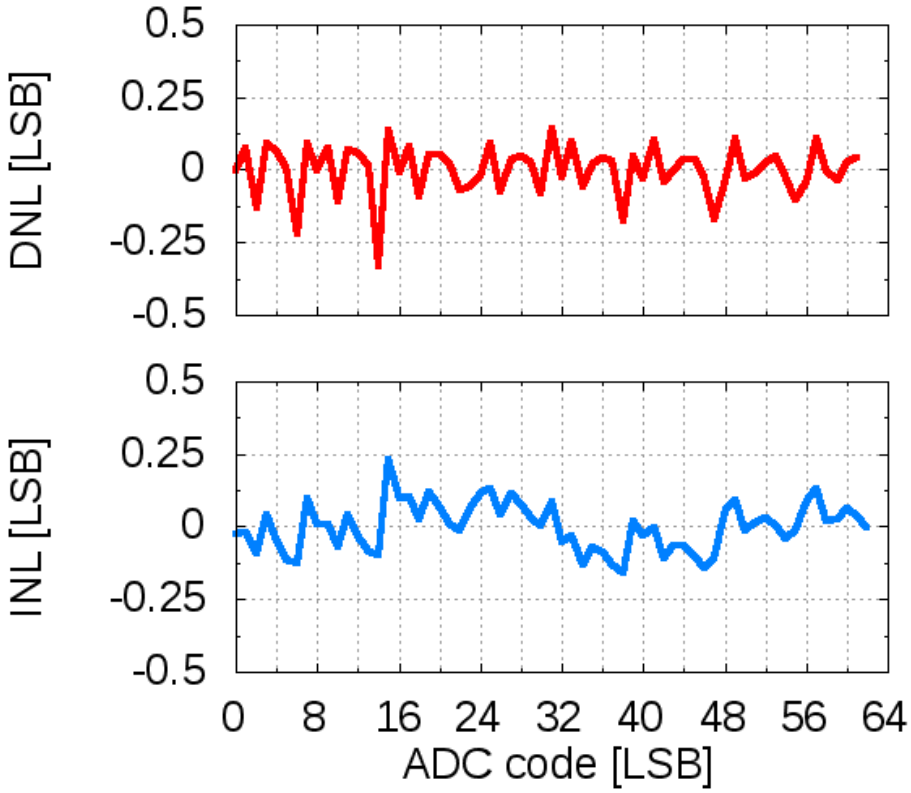
DAQ – receives fast transmission from ADC (up to 500 Mb/s), captures the data and sends to PC via Ethernet for offline analysis

6-bit SAR ADC for LHCb upgrade
Static tests – linearity (@50 MS/s)

Transfer function



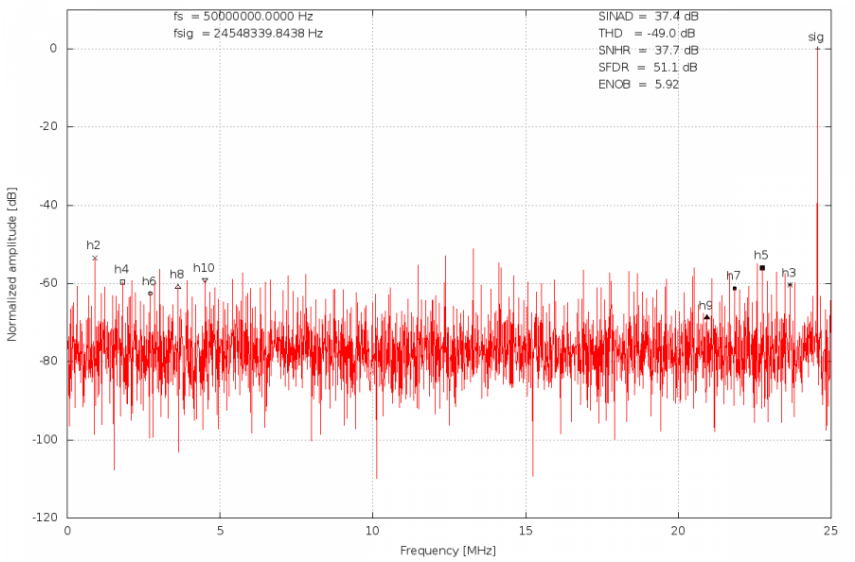
INL/DNL measurements



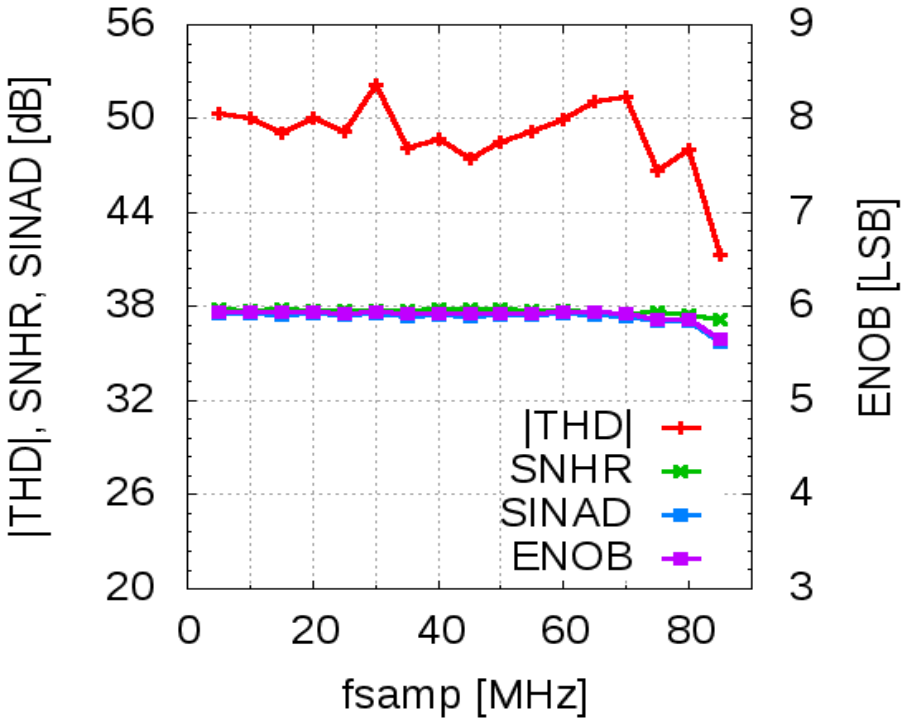
- Measurements show that ADC works very well
- At 50MHz sampling frequency good linearity INL, DNL < 0.5 is seen

6-bit SAR ADC for LHCb upgrade
Dynamic tests – ENOB effective resolution

Example DFT Spectrum @50MS/s



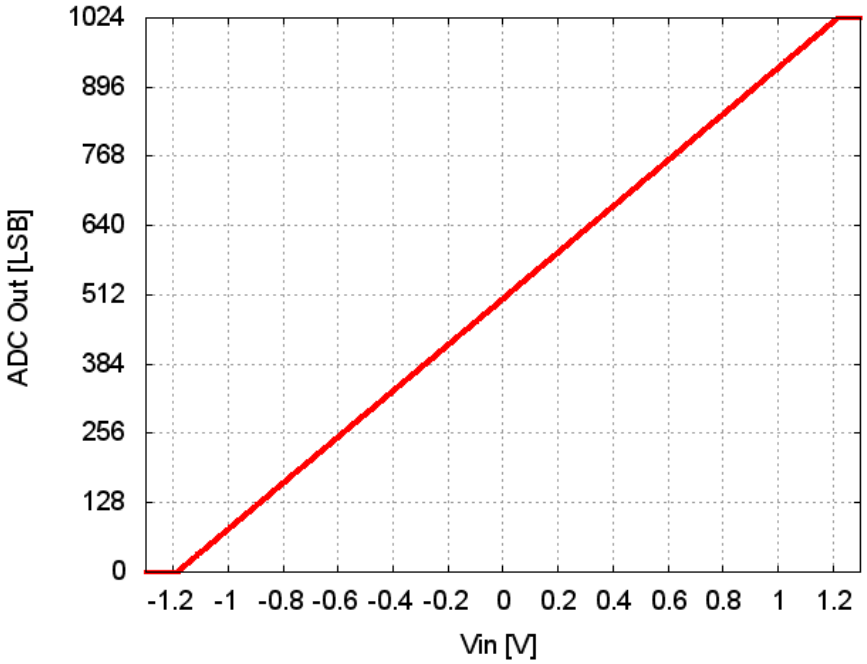
Sampling frequency sweep



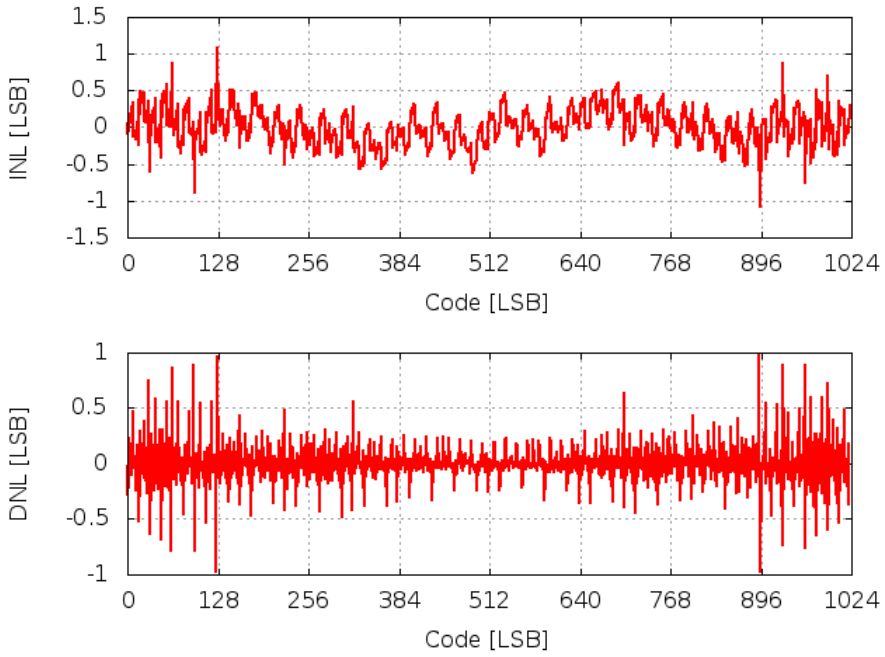
- Measurements show very good dynamic behaviour.
- The measured ENOB is between 5.7 – 5.9 bits
- The ADC works well for sampling frequencies beyond 80 MHz

10-bit SAR ADC for LumiCal
Static measurement results

Transfer function



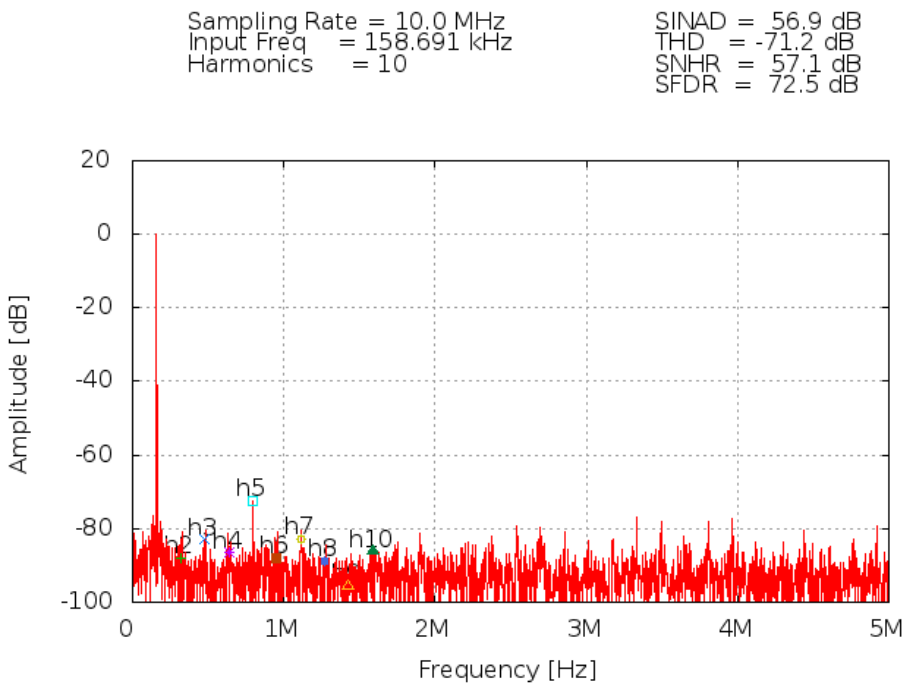
INL/DNL measurements



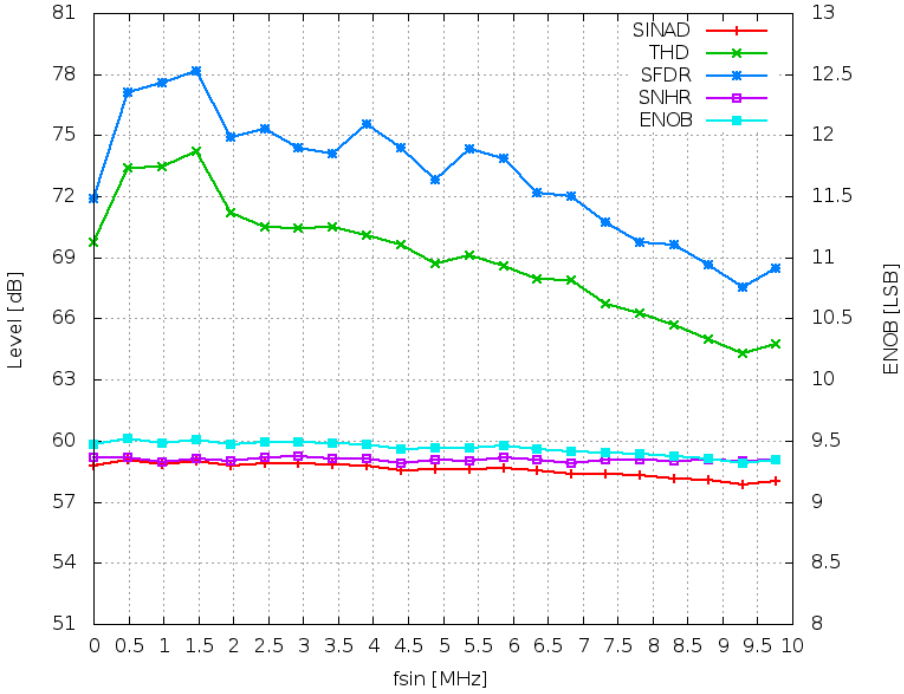
- ADC works well in the whole input signal range
- Generally, good linearity is measured, although for a few codes improvement is still needed

10-bit SAR ADC for LumiCal
Dynamic measurement results (@10 MS/s)

Example DFT Spectrum



Input frequency sweep



ENOB~9.3 up to Nyquist input frequency for f_{sample} ~20MHz

ADC works for f_{sample} up to about 50 MS/s, but above 20 MS/s ENOB start to decrease.
Problem with jitter above 20 MS/s found..., will be fixed in next submission.

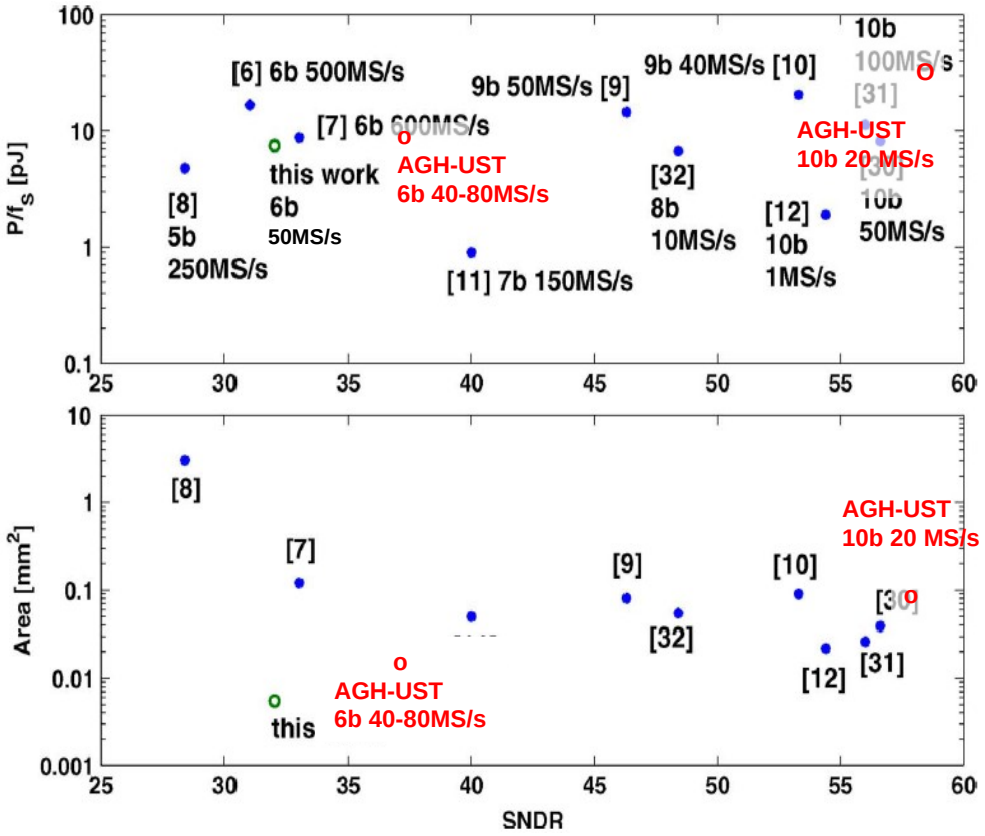
Prototypes of SAR ADC vs State-of-the-Art
Performance of first prototypes

Main features:

	LHCb	LumiCal
• Resolution [bits]	6	10
• Sampling frequency [MS/s]	>80	20 (50*)
• Power cons. [mW] @ 40 MS/s	0.35	1
• Size [mm^2] Dim. [µm]	0.016 40 x 400	0.087 146x600
• DNL/INL [LSB]	<0.4	~1.0
• SINAD@40MS/s [dB] ENOB [bits]	37.5 5.8	>56 9.3
• FOM [fJ/conv]	~150	~50

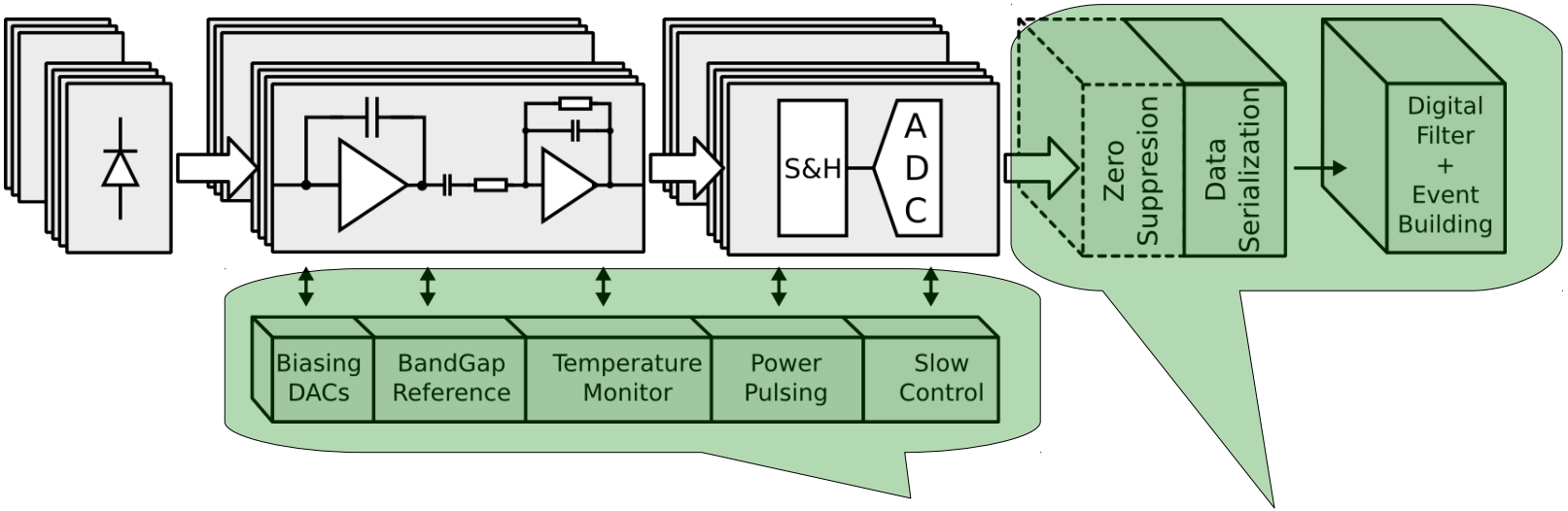
Performance of **our ADCs** is similar to **State-of-the-Art designs**

*) ADC works for f_{sample} up to about 50 MS/s, but above 20 MS/s ENOB start to decrease.



AGH-UST data were added to Table taken from “this work” :
P.Nuzzo, C. Nani, at el.,*“A 6-Bit 50-MS/s Threshold Configuring SAR ADC in 90-nm Digital CMOS”*,
IEEE Trans. On Circuits and Systems I vol.59 pp.80-92 January 2012

Multichannel readout aspects



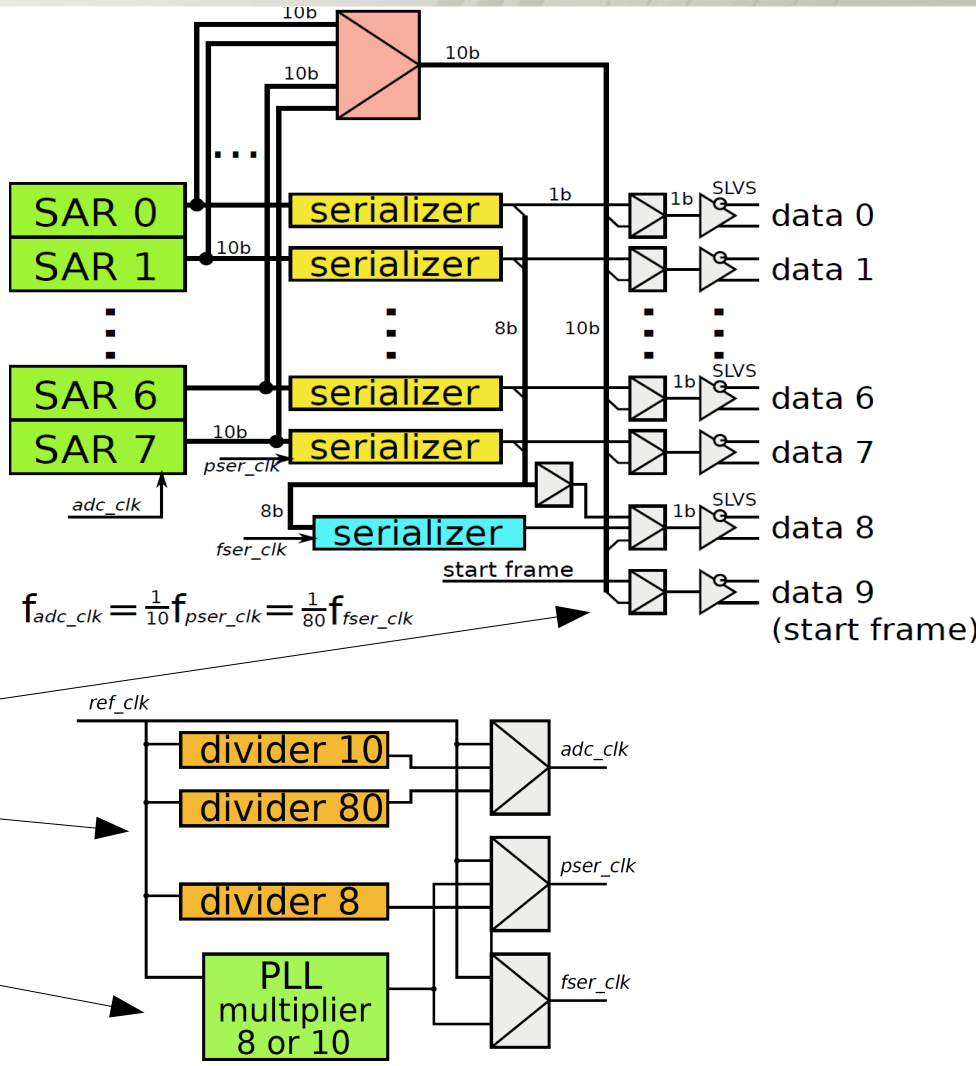
Multichannel readout with ADC conversion becomes real System on Chip (SoC) and needs peripheral circuits:

- PLL/DLL for data multiplexing&serialization,
- DACs,
- Precise voltage reference (bandgap),
- temperature sensor (PTAT),
- Slow control (eg. SPI or I2C),
- I/O circuits like LVDS/SLVS,
- Digital Signal Processing (Zero suppression, deconvolution, etc...)

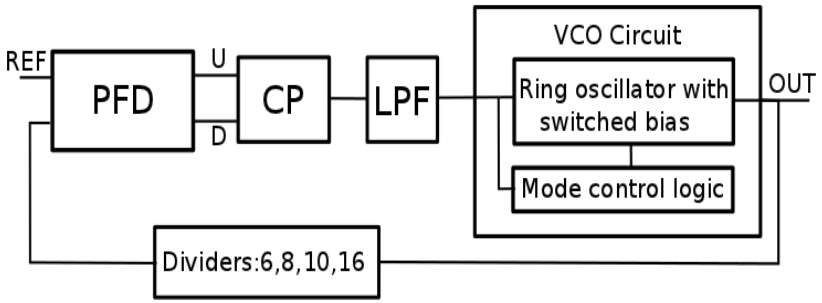
Prototype of multiplexer and serializer blocks for multichannel SAR ADC

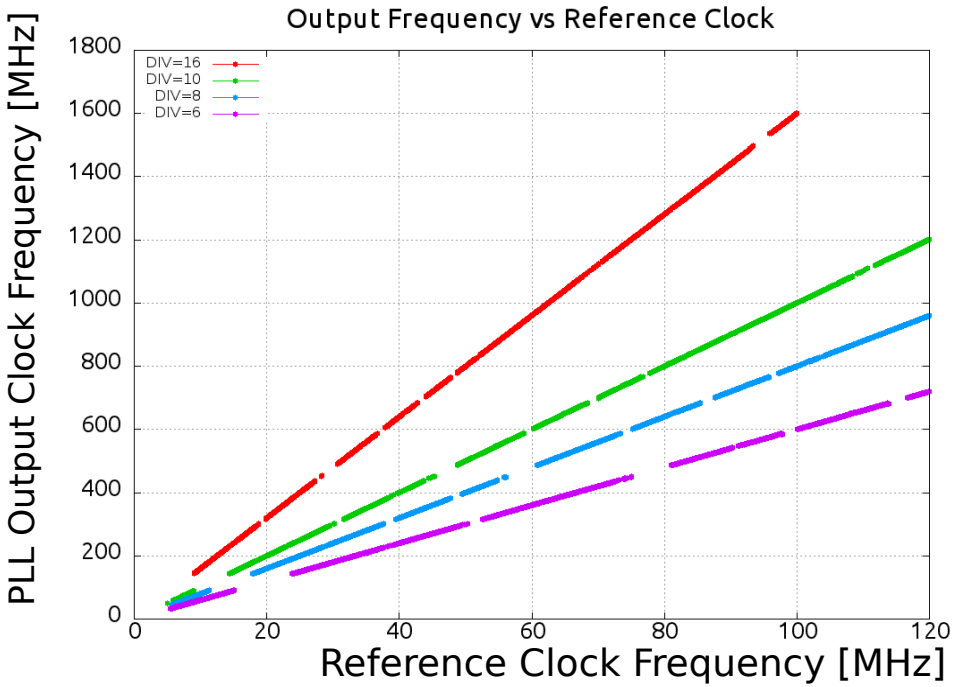
Specifications & implementation issues:

- 8 channels of 10-bit (6-bit) SAR ADC
- Technology 130 nm CMOS
- Multimode digital multiplexer/serializer:
  - Full serialization: one data link per all channels (external clk division or PLL clk generation)
  - Partial serialization: one data link per channel (external clk division or PLL clk generation)
  - Test mode: single channel output (max fsmp ~50 Msps)
- High speed SLVS interface (~1GHz)
- Multiple clock generation schemes (with or without PLL)
- PLL for data serialization
- Power pulsing



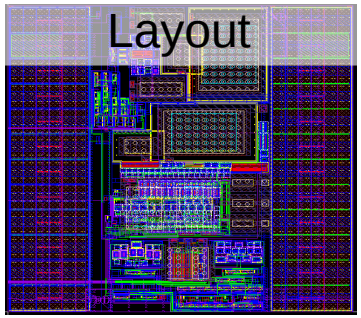
Multichannel readout aspects
Low power PLL in 130 nm CMOS





Main features:

- General purpose PLL block
- Very wide output frequency range: **10MHz – 3.5GHz** (tested up to 1.6GHz)
  - Gaps in frequency are found in the prototype – to be eliminated...
- 16 VCO modes - Automatically (or manually) changed
- Jitter 15-70 ps (to be improved...)
- Power consumption **~0.6mW@1GHz**
- Different loop division factors: **6,8,10, 16**
- Size 300um x 300um



Very low power PLL has been developed and the prototype is fully functional.
Few issues (frequency gaps, jitter) need to be improved

Summary

Potential of deep-submicron CMOS technologies, together with recent developments in ADC architectures (SAR in particular) allow to build multichannel front-end ASICs comprising ADC in each channel, without penalty on power consumption

(Modern ADC can consume significantly less power than preamp&shaper circuitry)

Multichannel readout ASIC becomes complex Systems on Chip (SoC), comprising hundreds of channels, preamplifier, shaper, ADC, DSP, PLL, DLL, serializer/deserializer, digital interfaces, etc...

Thank you for attention

References

- K. Świentek, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, T. Szumlak
  “SALT – new silicon strip readout chip for the LHCb Upgrade”,
  TWEPP2013 23-27 September 2013, Perugia Italy
- J. Moron, M. Firlej, T. Fiutowski, M. Idzik, Sz. Kulis, K. Swientek.
  “Development of variable sampling rate low power 10-bit SAR ADC in IBM 130 nm technology”,
  TWEPP2013 23-27 September 2013, Perugia Italy
- M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Swientek,
  “Development of scalable frequency and power Phase-Locked Loop (PLL) in 130nm CMOS technology”,
  TWEPP2013 23-27 September 2013, Perugia Italy
- Sz. Kulis, A. Matoga, M. Idzik, K. Świentek, T. Fiutowski, D. Przyborowski
  “A general purpose multichannel readout system for radiation detectors“
  Journal of Instrumentation, JINST 7 T01004, January 2012
- M. Idzik, Sz. Kulis, D. Przyborowski
  “Development of front-end electronics for the luminoisty detector at ILC“
  Nucl. Instr. and Meth. A 608 (2009) pp.169-174
- M. Idzik, K. Swientek, T. Fiutowski, S. Kulis, P. Ambalathankandy
  “A power scalable 10-bit pipeline ADC for Luminosity Detector at ILC“
  JINST 6 P01004 2011