R&D for a highly granular SiW ECAL
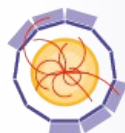
Thibault Frisson (CERN)

Thanks to Pr. Martin Breidenbach (SiD SiW)
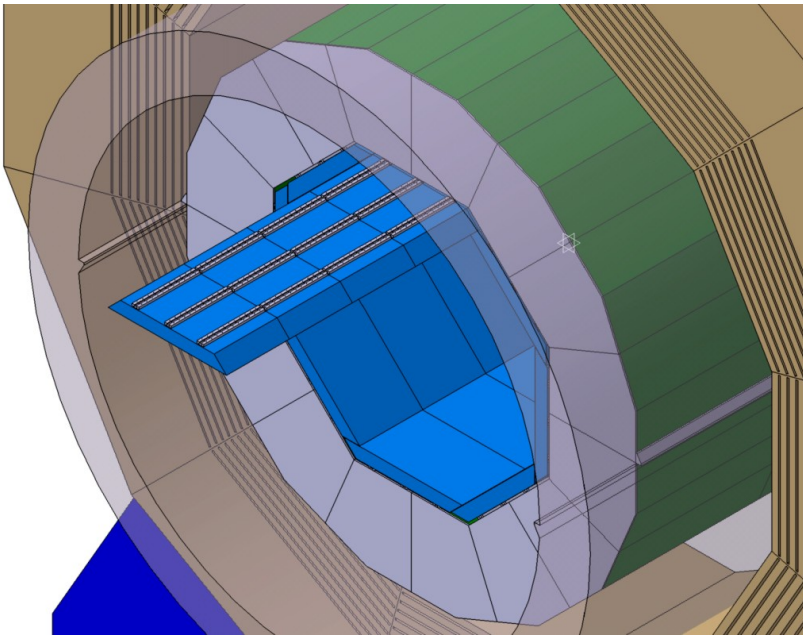
SiW ECAL for a future LC detector

➡️ Optimized for Particle Flow Algorithm

The SiW ECAL in the ILD Detector

Requirements:
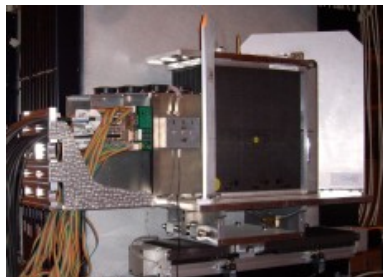- Extreme high granularity
- Compact and hermetic

Choices:
- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, λ_I=96mm
  - Narrow showers
  - Assures compact design

- Silicon as active material
  - Support compact design
  - Allows for pixelisation
  - Large signal/noise ratio

SiW ECAL R&D

CALICE SiW

Physics Prototype
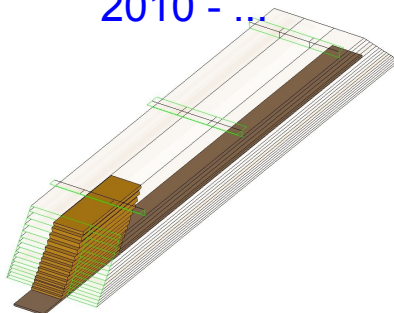Proof of principle
2003 - 2011

Number of channels : 9720

Weight : ~ 200 Kg

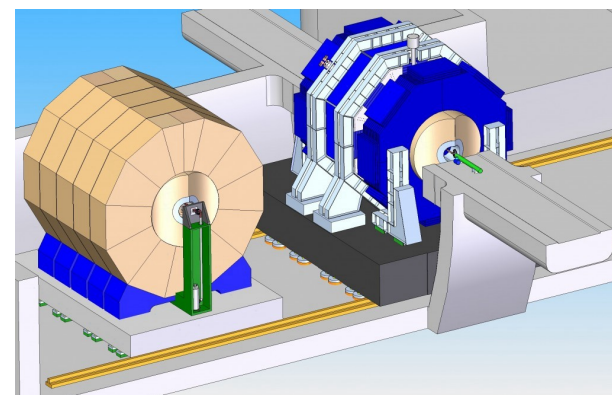**Technological Prototype**
Engineering challenges
2010 - ...

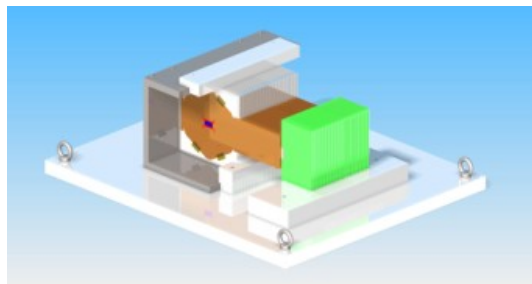

Number of channels : 45360

Weight : ~ 700 Kg

LC detector(s)

SiD SiW

Technological Prototype
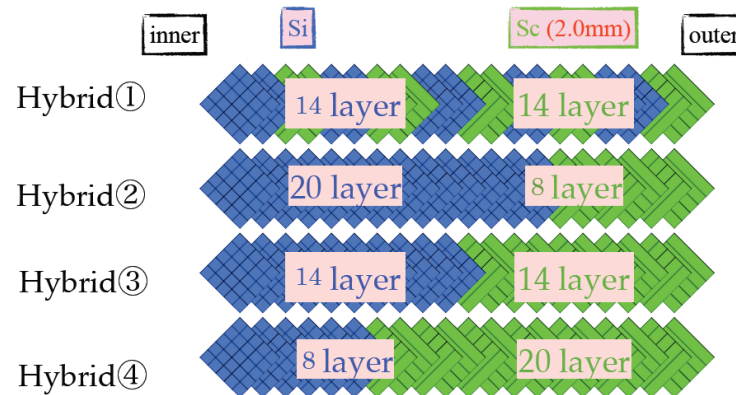Engineering challenges
2003 - ...

Number of channels : ~30000

Others SiW ECAL....

- MAPS

Ensure the pixels are small enough to avoid multiple particles passing through a single pixel

- Pixels: ~ 50x50 μm^2
- Binary readout
- total ECAL ~10^{12} pixels (need readout integrated into pixel)
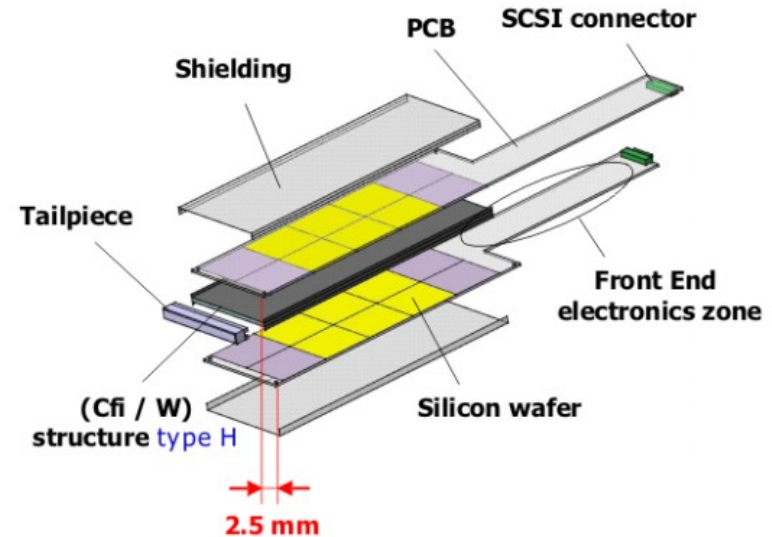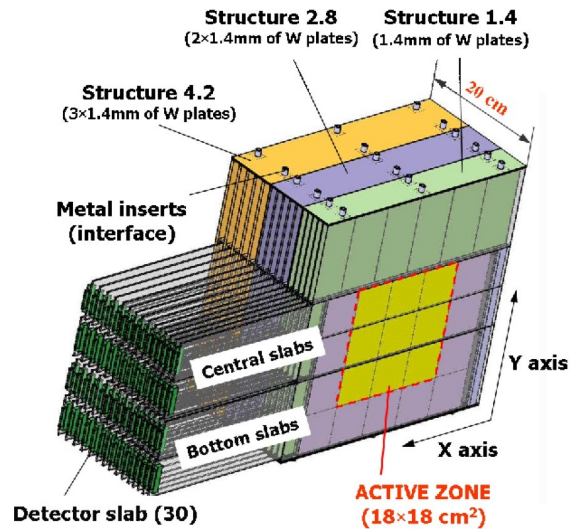- CMOS MAPS sensor

- Hybrid (Sci - Si)

- Others experiments:
  - Phoenix upgrade
  - ALICE upgrade (FoCAL)
  - PAMELA

Physics prototype – CALICE SiW
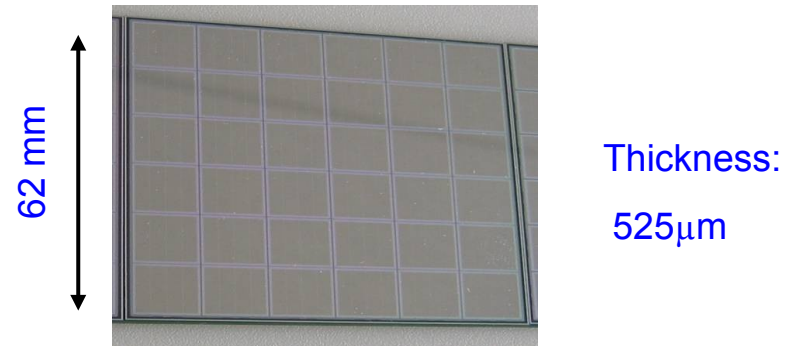

30 layers of tungsten: 24 X_0, 1 λ_I

Carbon-fibre mechanical structure

10k channels

S/N ~ 8

$\sigma_E / E = 16.5/\sqrt{E(GeV)} + 1.1\ \%$

→ Studied in various test beam facilities

2006-2011: DESY, CERN, FNAL

e-, μ, π, p (1 - 180 GeV)

6x6 PIN Diode Matrix – **1 x 1 cm²**

62 mm

Thickness:

525μm

Resistivity: 5kΩcm

80 (pairs e/hole)/μm

Imaging interactions – CALICE SiW


Two pions entering
the SiW Ecal
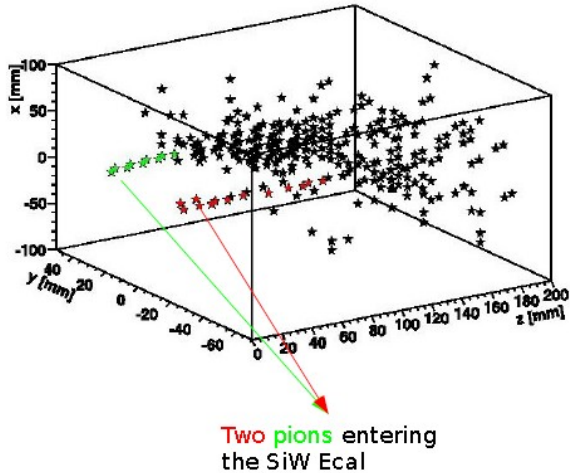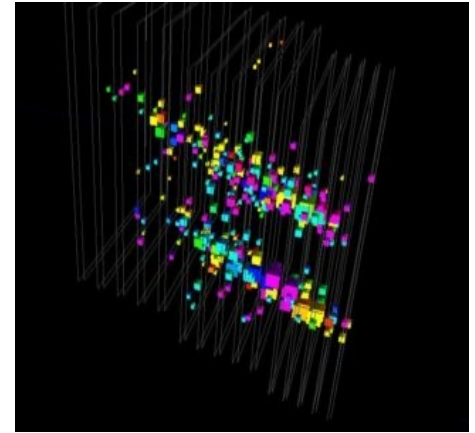
Proof of principle for high granularity calorimeter

high transverse and longitudinal granularity
→ unprecedented details of the showers

Small X_0 / λ_i
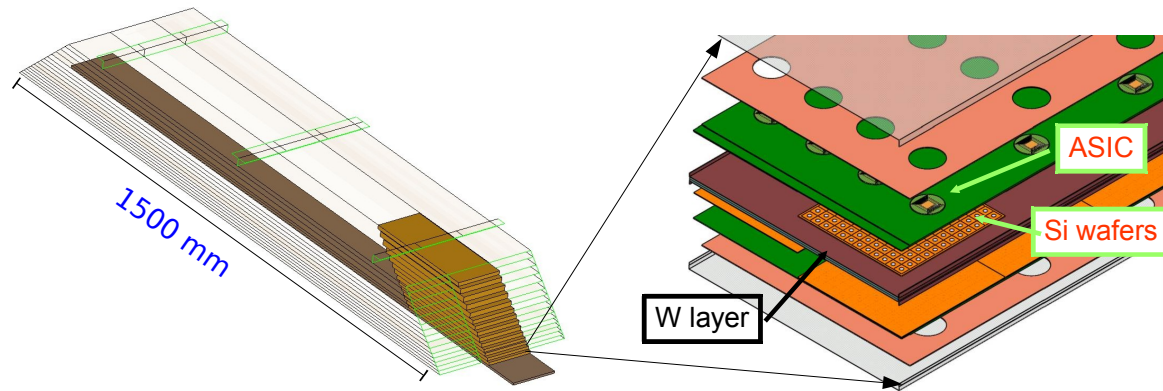→ study the components of the shower

High granularity allows particle tracking through detector
→ Imaging processing techniques (Hough transformation)

High granularity permits detailed testing of G4 simulations
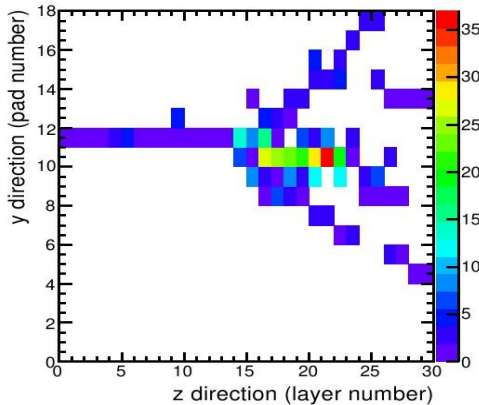
Technological prototypes

Technological solutions for the final detector

- Realistic dimensions
- Integrated front end electronic
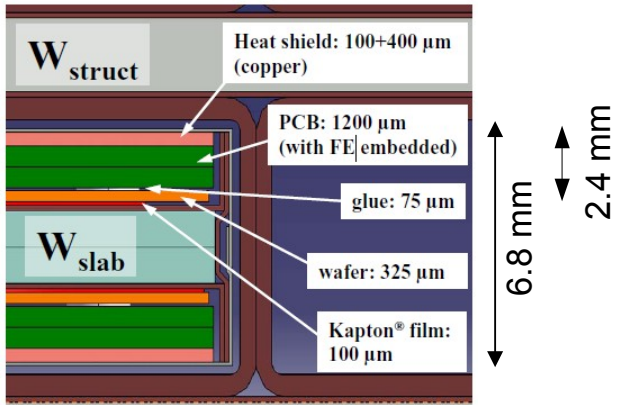- Small power consumption (Power pulsed electronics)

SiW technological prototypes

CALICE SiW

24 X_0 ~1 λ

Tungsten:

- 2.1 mm (20 layers)
- 4.2 mm (9 layers)

Wstruct Heat shield: 100+400 μm (copper)

PCB: 1200 μm (with FE embedded)

glue: 75 μm

Wslab wafer: 325 μm

Kapton® film: 100 μm

6.8 mm

2.4 mm

25 mm² square,
256 pixels

SKIROC
64 channels, 15-deep buffer...

SiD SiW
(Very ambitious design)

29 X_0 ~1 λ

Tungsten:
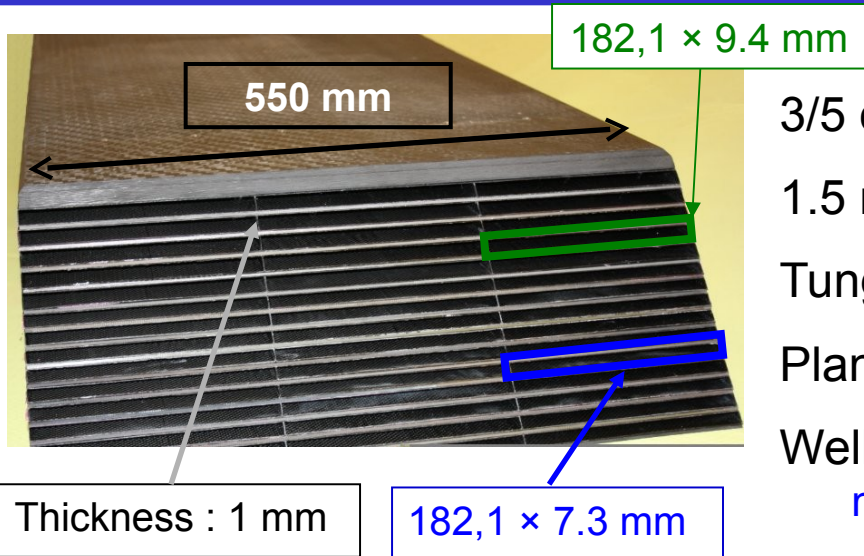
- 2.5 mm (20 layers)
- 5 mm (10 layers)

Metallization on detector from KPix to cable

Bump Bonds

Tungsten

KPiX

Si Detector

Tungsten

Kapton Data (digital) Cable

Kapton

Heat Flow

Gap ≤ 1 mm

Thermal conduction adhesive
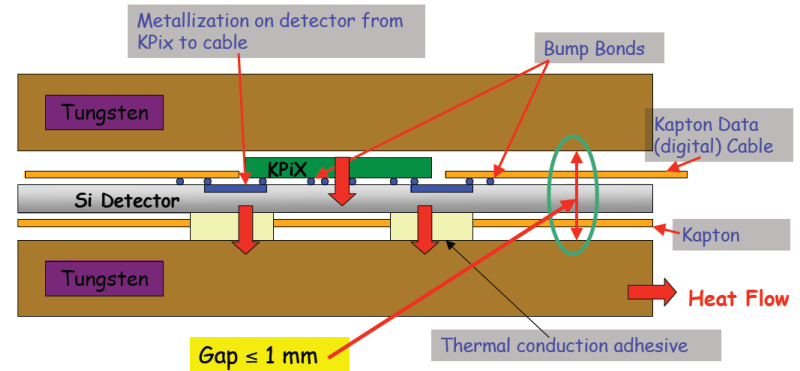
13 mm² hexagons,
~1000 pixels
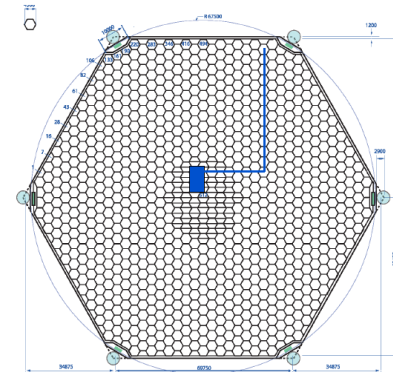
KPiX
1024 channels, bump-
bonded, 4-deep buffer...

Mechanical structure – CALICE SiW

550 mm

182,1 × 9.4 mm

182,1 × 7.3 mm

Thickness : 1 mm

3/5 of a barrel module of the ILD concept

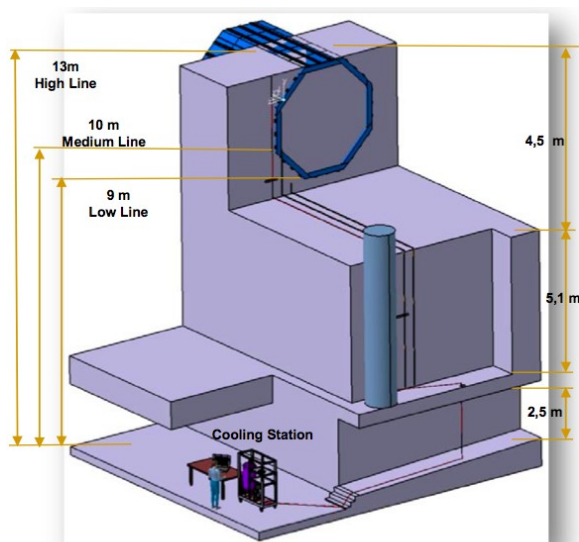1.5 m long alveolar structure to house ECAL layers

Tungsten plates wrapped into Prepreg

Planar within 5 mm

Well understood
mechanical constraints, thermal behavior

Work on longer structures are ongoing

Evacuation of (residual) power of 0.2-0.35 W / layer

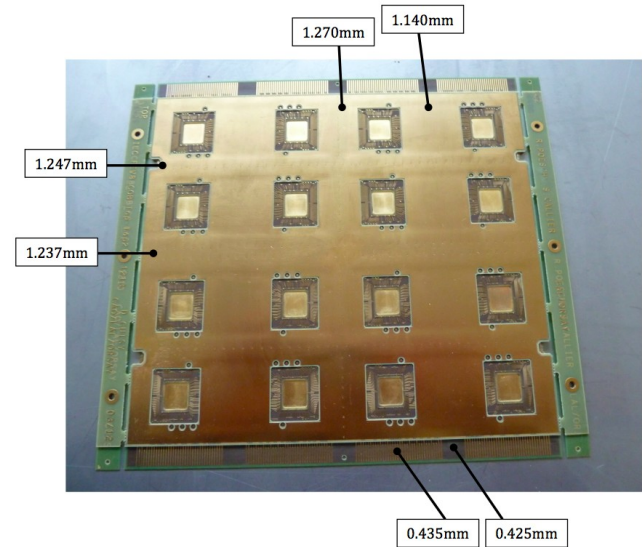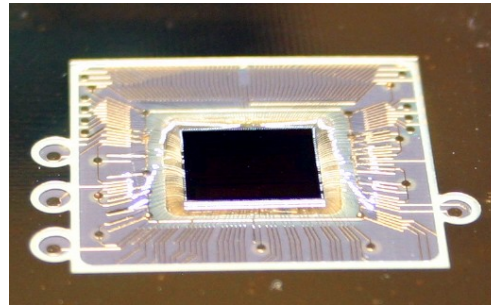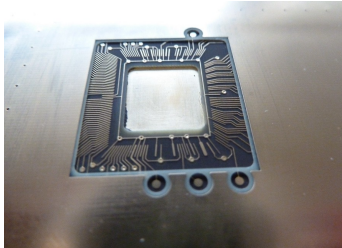Development of a leak less cooling system for a full detector

PCB – Embedded electronics – CALICE SiW

PCB prototype for embedding the chips: aggressive design

1.2 mm height for a board of 18 x 18 cm² and 9 layers
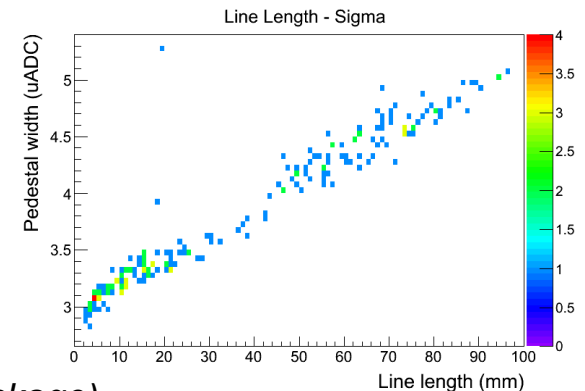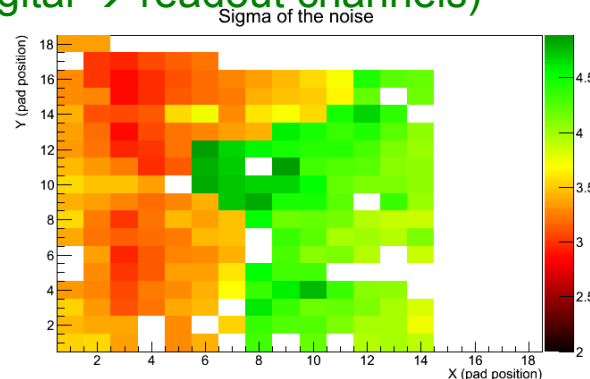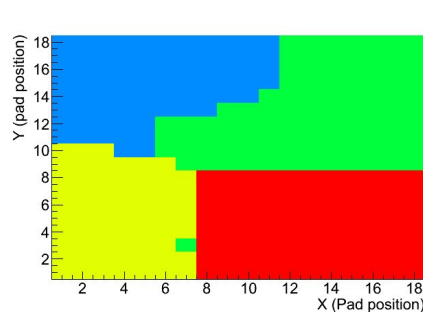Deviation from total flatness max: 0.5 mm
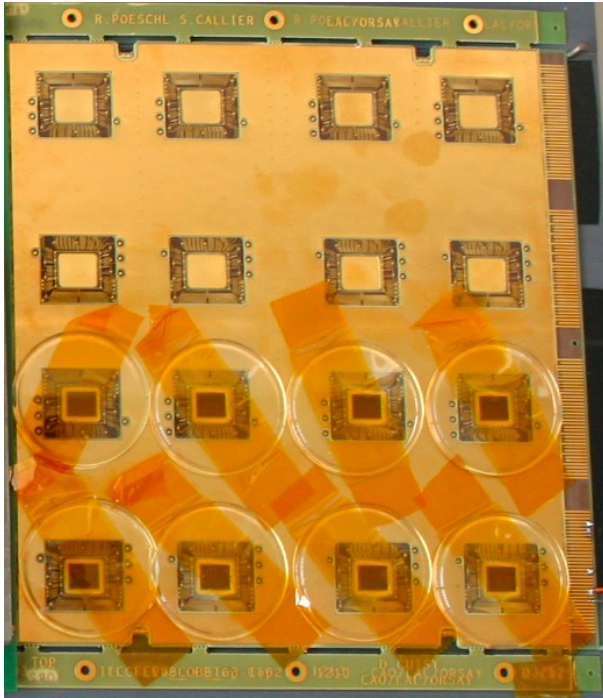ASICs bounded into

Line density in PCB → routing is crucial

Critical points are :

- Noise ∝ line length
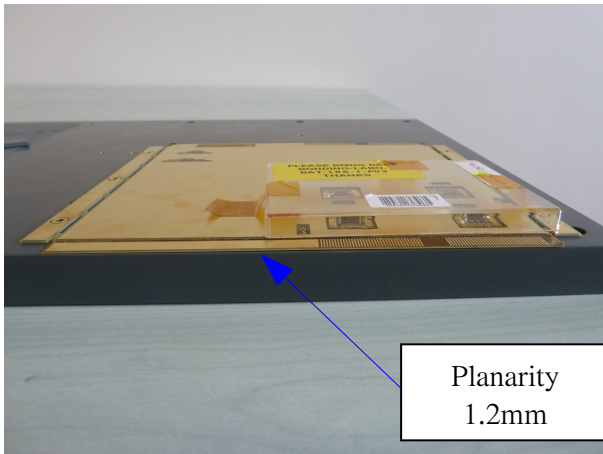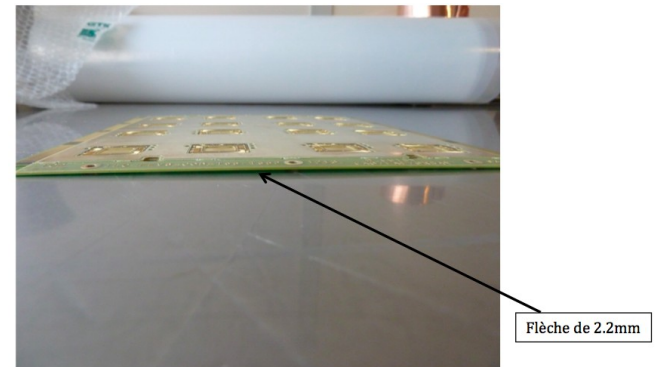- Cross talk (Digital → readout channels)

Results with conservative design (chip in package)

PCB – Embedded electronics – CALICE SiW

- First board for 16 ASICs (4 wafers)
- Equipped with 8 SKIROC ASICs (Bonding by CERN)
  → Bonding was not straightforward, thin bonding pads to be improved
- On-going electronic tests

Flèche de 2.2mm

Planarity
1.2mm

Test production at EOS company (FEV7)
- Very promising from mechanical point of view...
  ...however issues with gluing of wafers
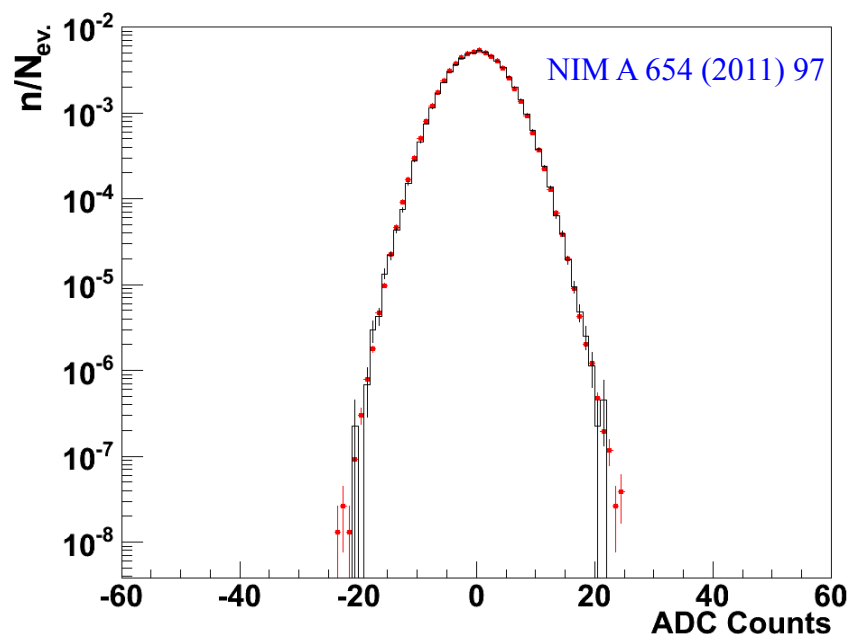- Could not be tested since it came somewhat late

→ FEV8

Embedded electronics - Parasitic effects?

Exposure of front end electronics to electromagnetic showers

Comparison: Beam events
(Interleaved) Pedestal events

NIM A 654 (2011) 97
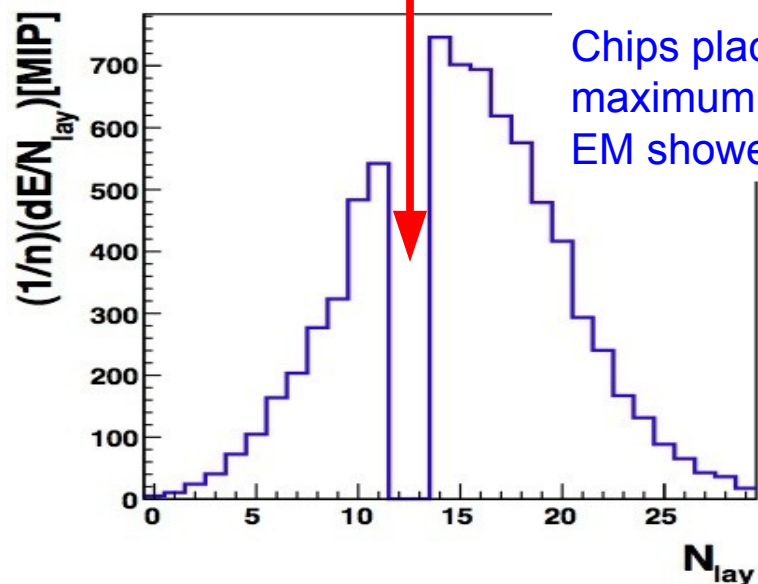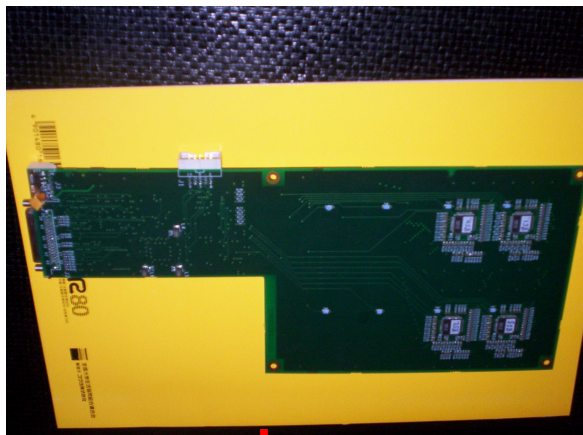
Chips placed in shower maximum of 70-90 GeV EM showers

- No sizable influence on noise spectra by beam exposure

ΔMean < 0.01% of MIP ΔRMS < 0.01% of MIP

- No hit above 1 MIP observed

=> Upper Limit on rate of faked MIPs: ~7x10^-7

Possible Effects: Transient effects
Single event upsets

Front end electronics: SKIROC – CALICE SiW

SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

- SiGe 0.35μm AMS (7.5 mm x 8.7 mm)

- High integration level (variable gain charge amp, 12-bit ADC, digital logic)

- 64 channels

- Energy measurement (14 bits):

  - 2 gains (1-10) + 12 bit ADC: 1 MIP (4fC) $\rightarrow$ 2500 MIPs

  - Shaping time 180 ns

- Auto-trigger at ½ MIP

  - MIP/noise ratio > 10

  - Fast shaper ~30 ns

- Analog memory

  - Depth = 15 (time and charge)

- Low consumption: ~25μW/ch (power pulsing)
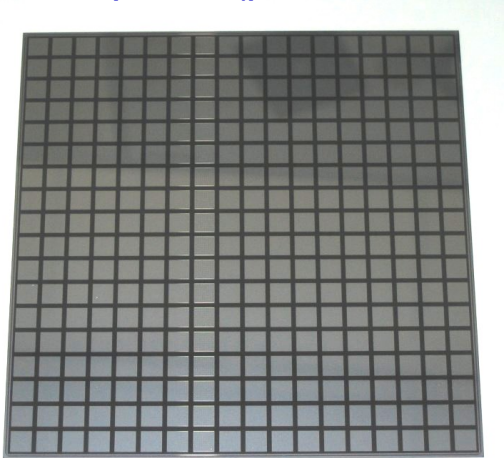
- On chip zero suppression (not yet)

Trigger delay
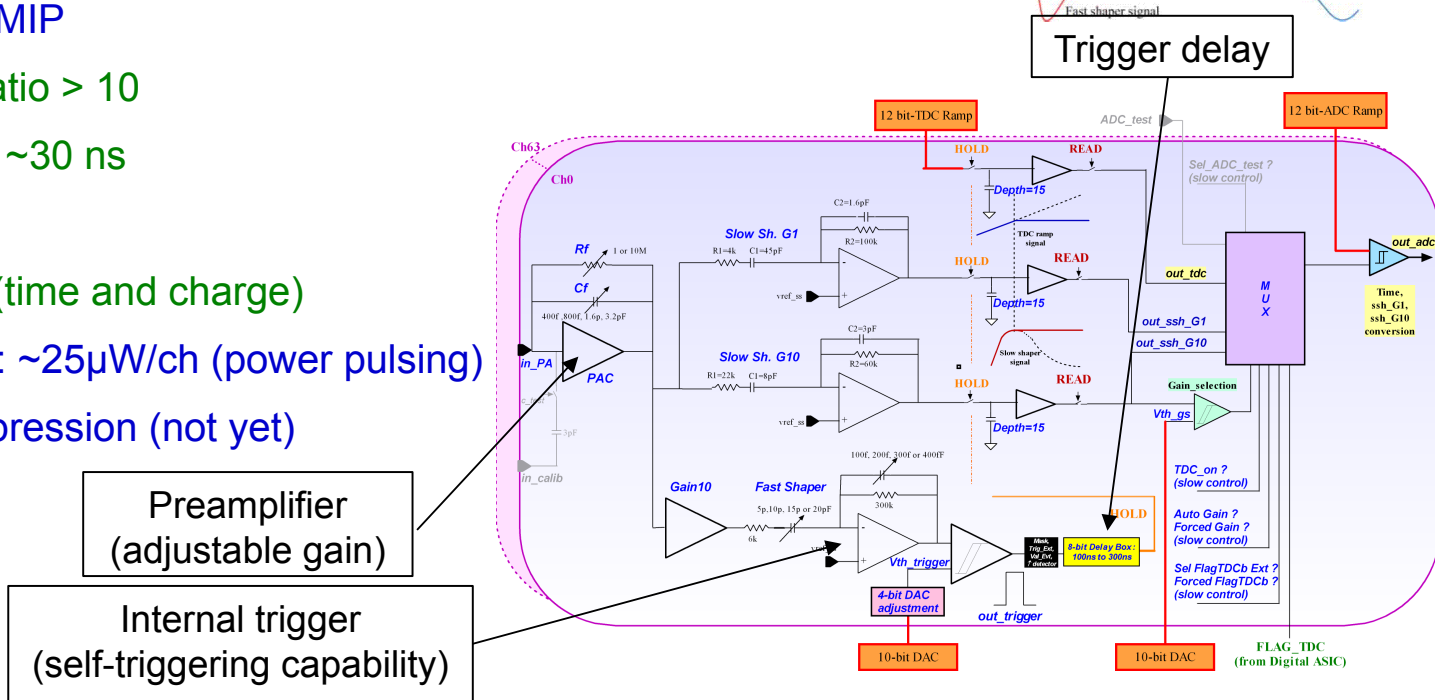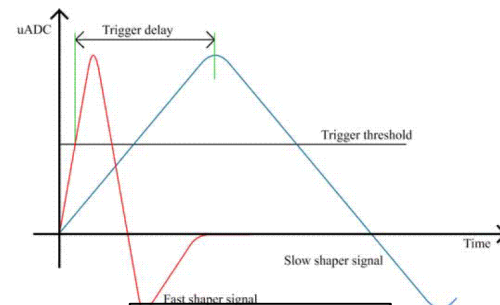
Preamplifier (adjustable gain)

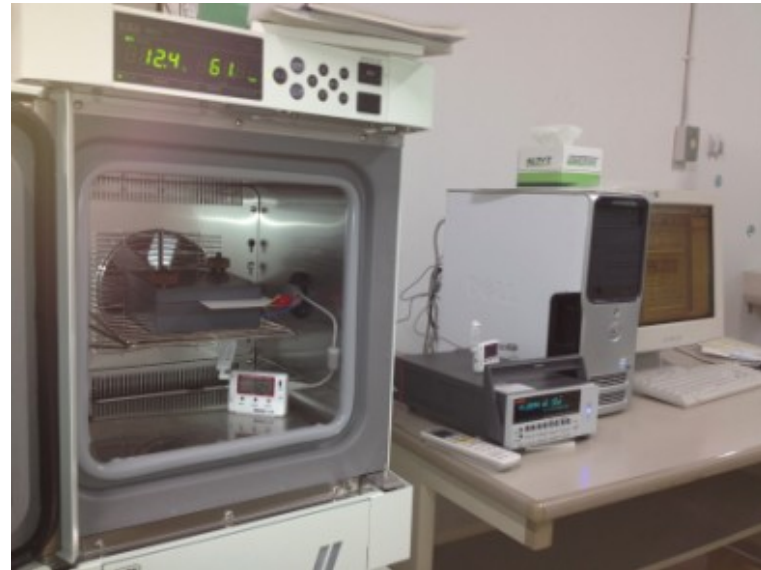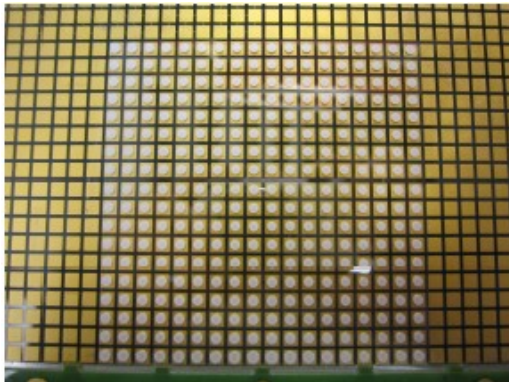Internal trigger (self-triggering capability)

Silicon wafers – CALICE SiW

Si wafer (HPK):

- 9x9 cm²
- Thickness = 320 µm (breakable → 500 µm ?)
- 256 pixels (pixel size = 5 x 5 mm²) → lateral granularity = 4 x better than physics prototype

Gluing onto PCB and development of automatised procedure


- Optimization studies on guard rings and characterization.

- Guard ring around the wafer to control the leakage currents

- Different technologies are tested

Test beam

Goals:

- Understand FE (SKIROC, KPiX)
- Complete understanding of the detector
  - → Filtering of non-physic events

- Establishment of calibration procedures for a larger number of cells
- Homogeneity of response (x,y scan of detector)
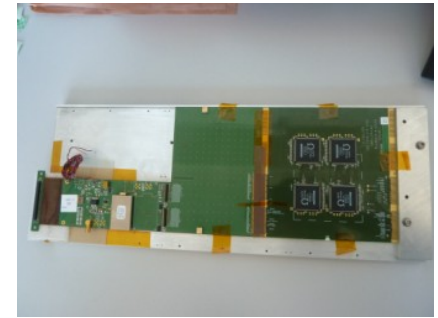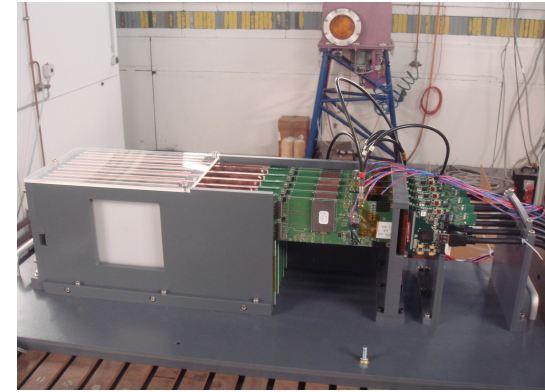
- Measure S/N

- First showers
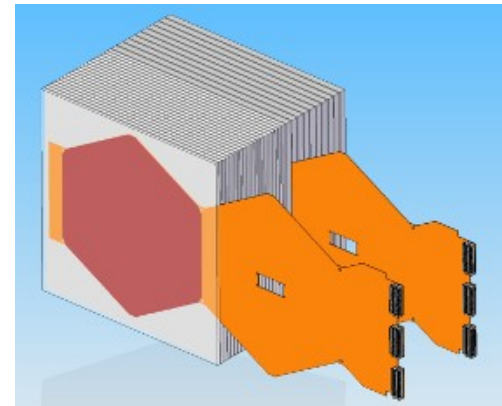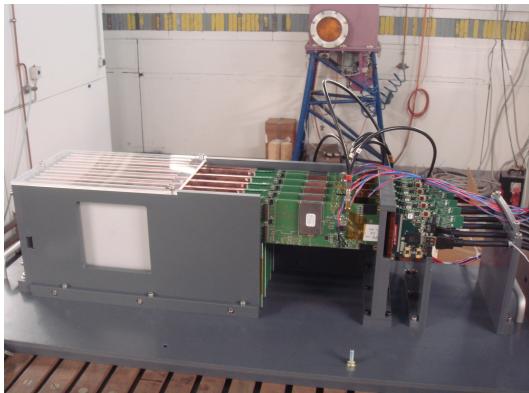
Test beam

CALICE SiW - DESY : e- (1 - 5 GeV) – 2012 / 2013

Intermediate step: Conservative layer design for beam tests
- First test in beam
- Benchmark to go further

- Single detection layer
- 4 ASICs per slab (¼ final design) – conservative design (chip in package)
    - 4 SKIROCs x 64 channels = 256 channels/slab
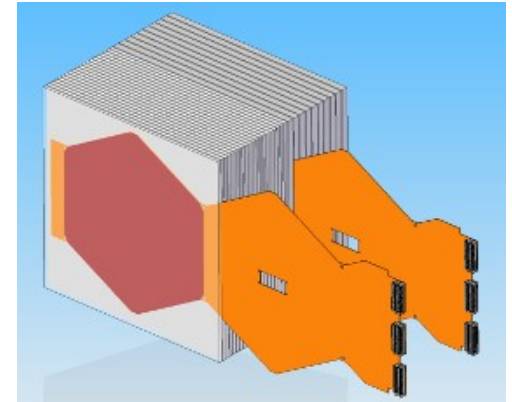- 6 – 8 layers → ~1500 - 2000 channels
- Power pulsing

SiD SiW - SLAC : e- (12.1 GeV) – 2013 / 2014

First test beam (End station A at SLAC - July 2013)
- Final design
- 9 layers interleaved with W-plates (6 X_0) → ~9000 channels
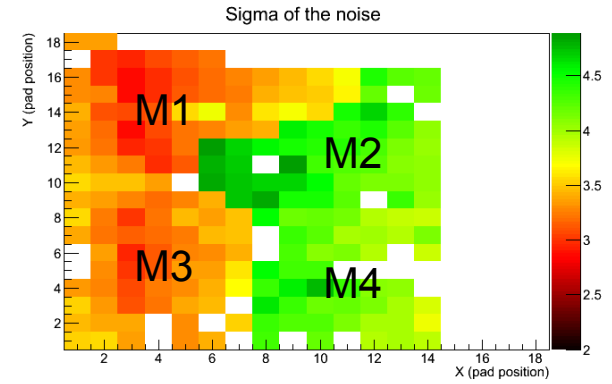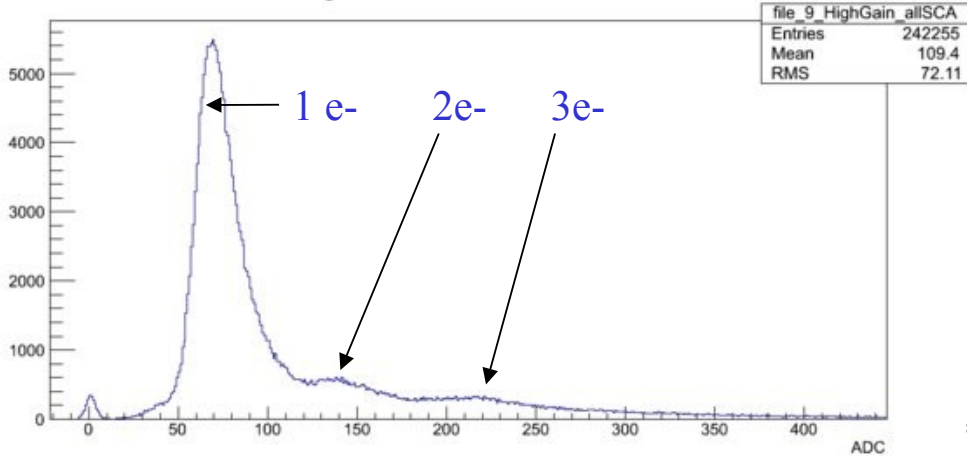- Power pulsing   See LCWS 2013 !
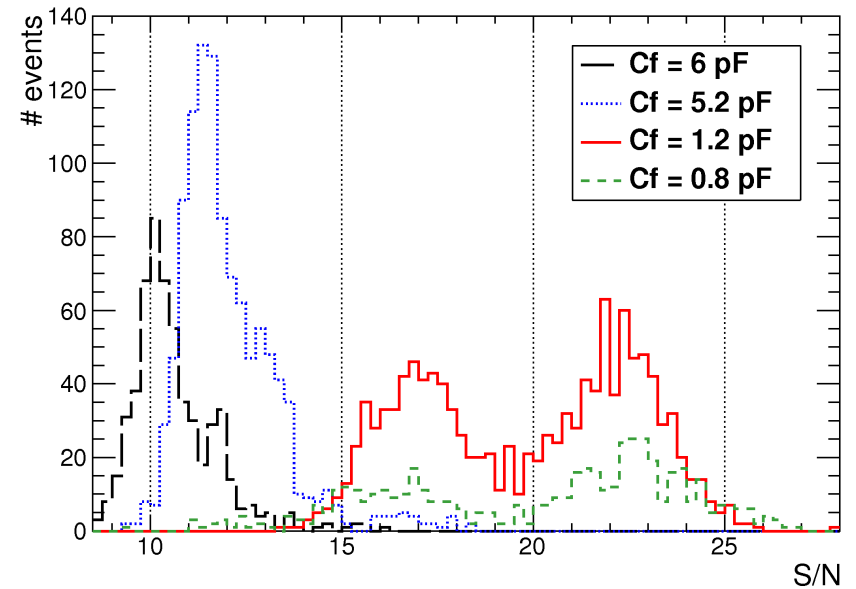
Next test beam (Early in 2014)
- Additional layers
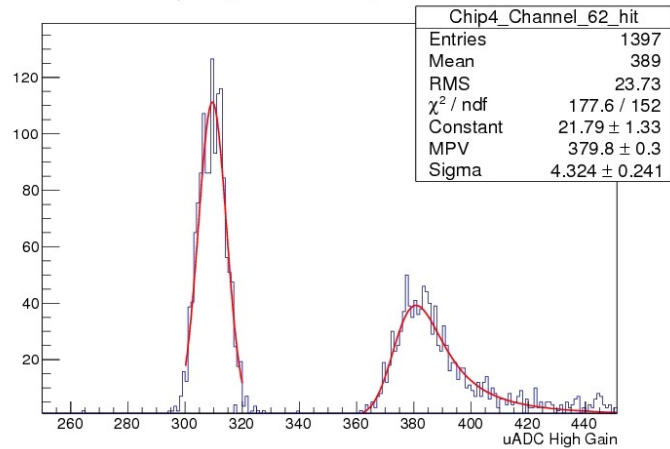
MIPs – CALICE SiW

Sigma of the noise

M1 M2 M3 M4

High Gain for all the SCA - file 9

file_9_HighGain_allSCA	
Entries	242255
Mean	109.4
RMS	72.11

1 e-   2e-   3e-

Gain : 1.2pF - SigmaDet = 4.90 - Signal over Noise ratio = 14

Chip4_Channel_62_hit	
Entries	1397
Mean	389
RMS	23.73
χ^2 / ndf	177.6 / 152
Constant	21.79 ± 1.33
MPV	379.8 ± 0.3
Sigma	4.324 ± 0.241

uADC High Gain

events

— Cf = 6 pF
····· Cf = 5.2 pF
— Cf = 1.2 pF
---- Cf = 0.8 pF

S/N

MIPs – SiD SiW

Cosmics Run with Calorimeter Sensor

MPV: 3.64
σ = 0.60167
Entries: 3257

Signal amplitude (fC)

Test beam run

detected charge, fC

•Upstream layer
•Two overlaid runs

2 test beam runs
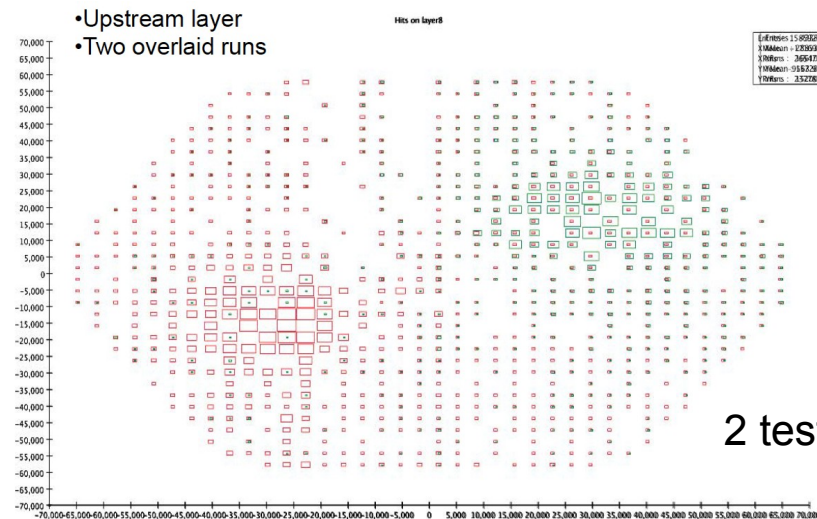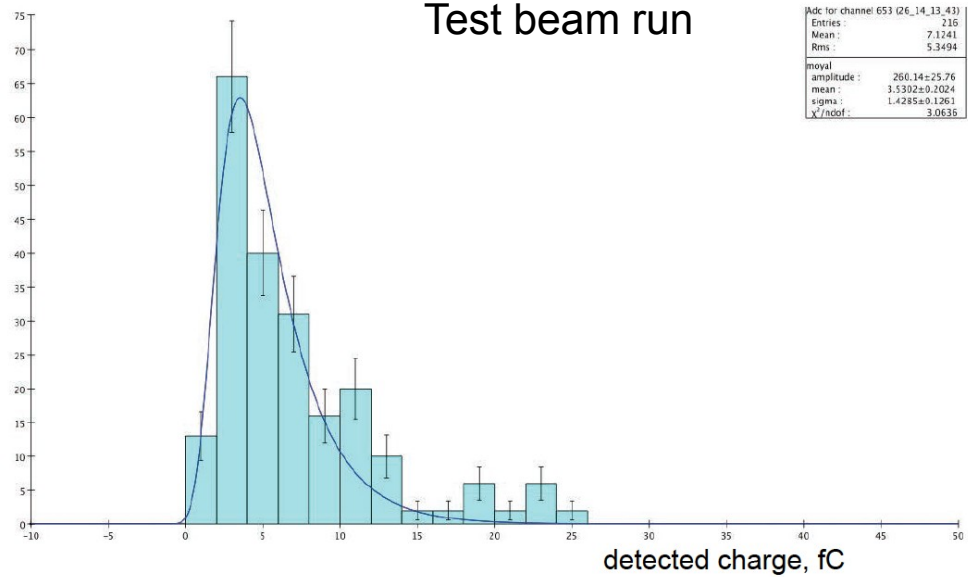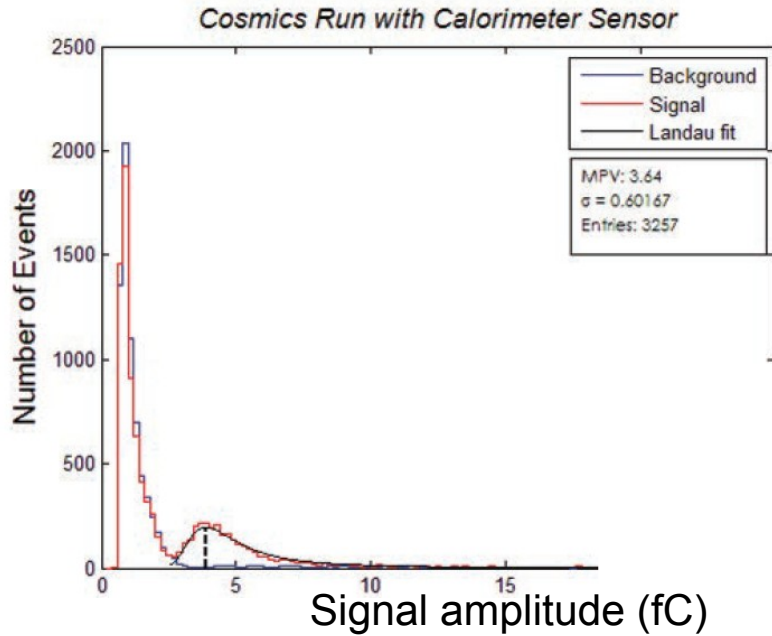
Power pulsing – CALICE SiW

Sigma of the noise

M1 M2 M3 M4

Noise for all the Pad of the detector

Layer 1   Layer 3   Layer 4   Layer 6

Noise in uADC

CC
PP

Trigger threshold too high

ASIC M1 and M3

ASIC M2 and M4

MPV for all the Pad of the detector

MPV in uADC

Pad Index

MIP Position - PP (uADC)

MIP Position - CC (uADC)
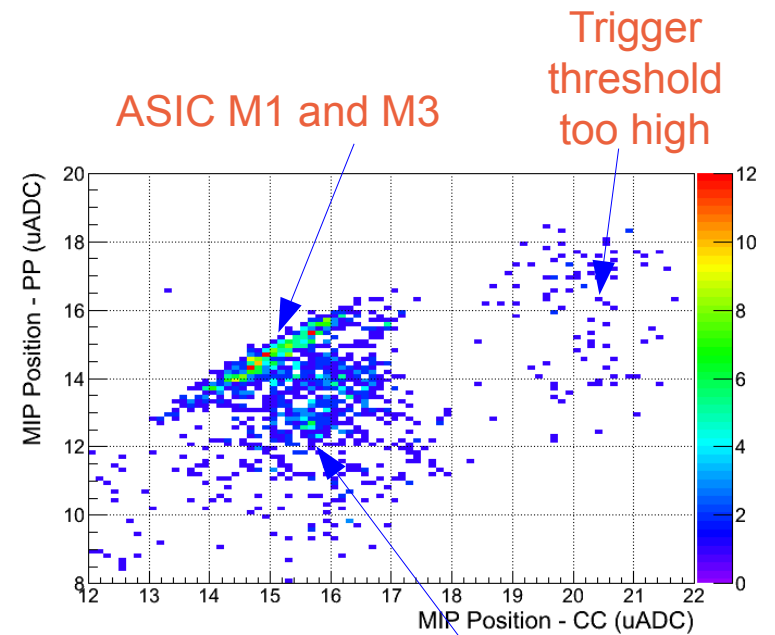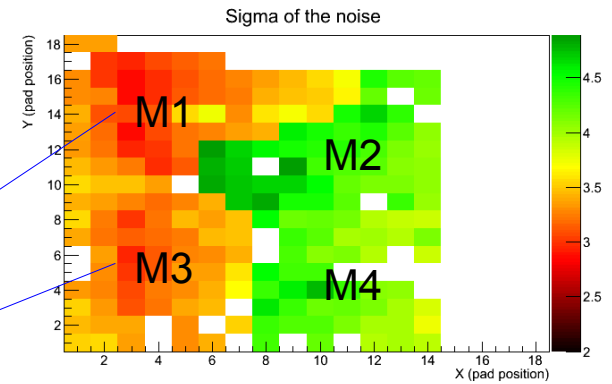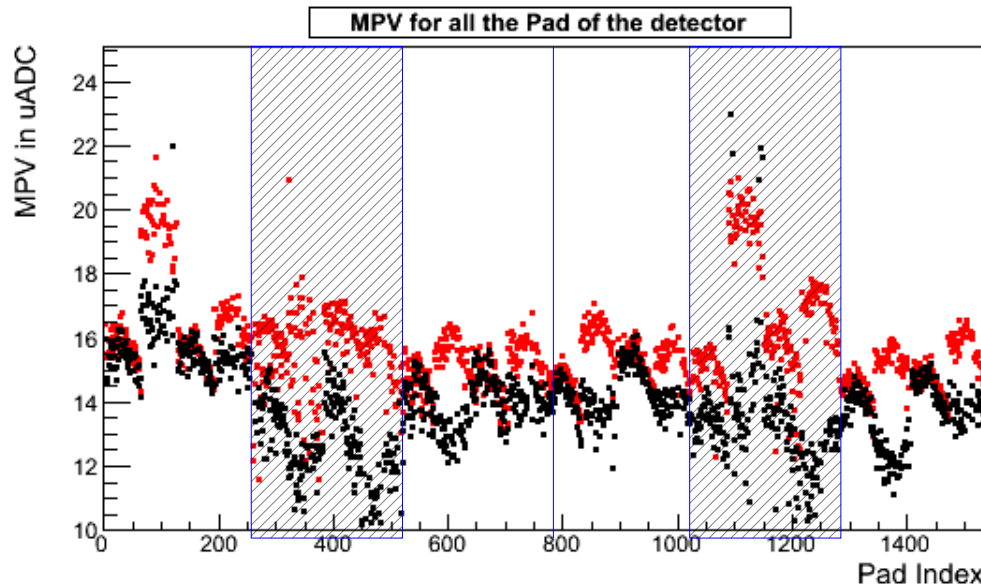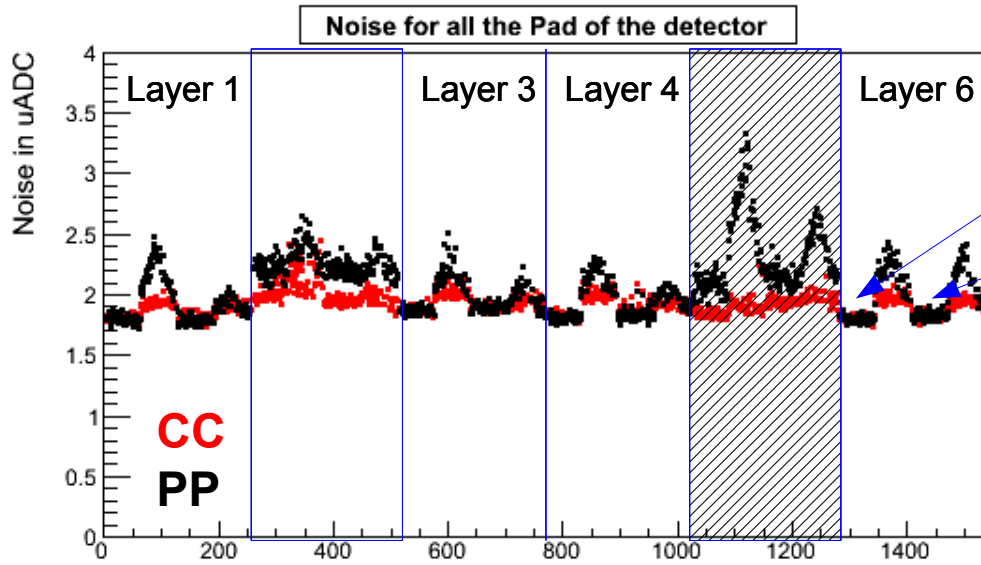
Summary and outlook

Successful R&D for a highly granular CALICE SiW ECAL physics prototype

Operated over several years

Exposed to several particle beam types and energies

Capacity of separating particles impressively demonstrated

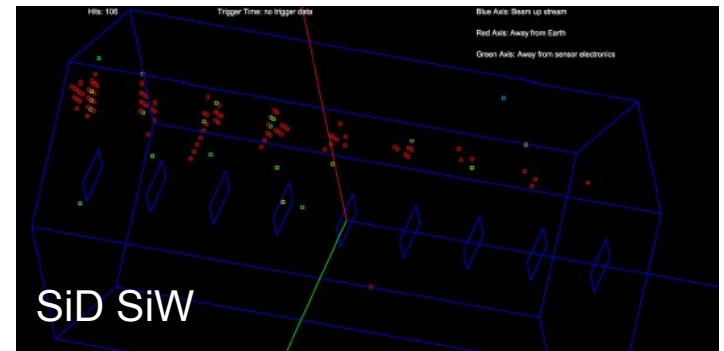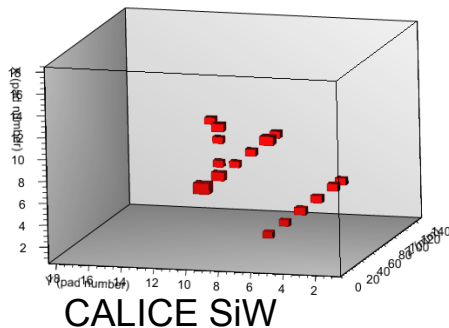The R&D(s) for technological prototypes is ongoing

A lot of work on different aspects to prove the engineering feasibility of the projects

- ASIC bump bonded to wafer

- long layers

- power consumption (power pulsing) → critical point
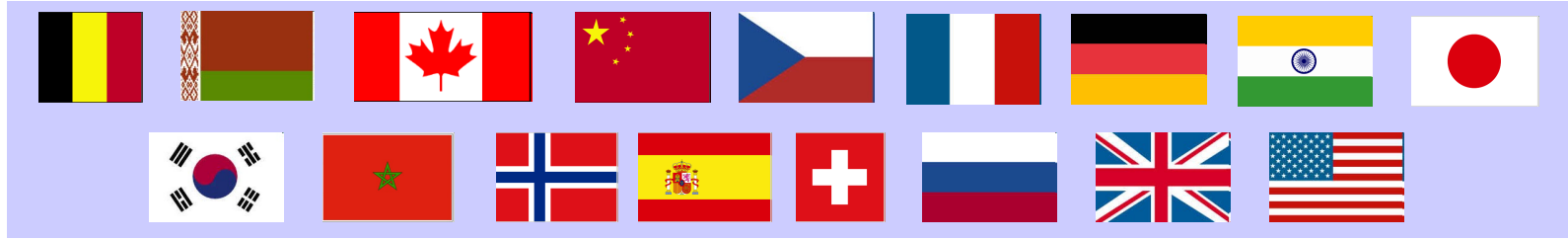
- ...

First test beams:

- encouraging results

- identification of open issues

Hardware development depends on optimization

CALICE SiW

SiD SiW

Back up

The CALICE collaboration

+300 people, +50 institutes, 17 countries

R&D detector for futur linear e+/e- collider

   (ECAL, HCAL, muon detectors, tail catchers…)

➔ Common approach:

Ultra-granular "imaging" calorimetry ➔ particle flow algorithm

- Physics Prototypes
  - Small prototypes. Proof of principle of technologies.
- Technological prototypes
  - Testing more realistic hardware designs which could be scaled up to full detector
- Combined beam tests
  - Reconstruction algorithms
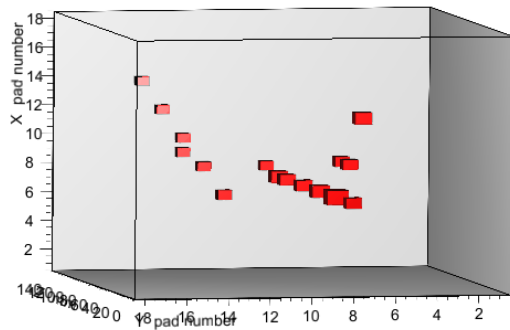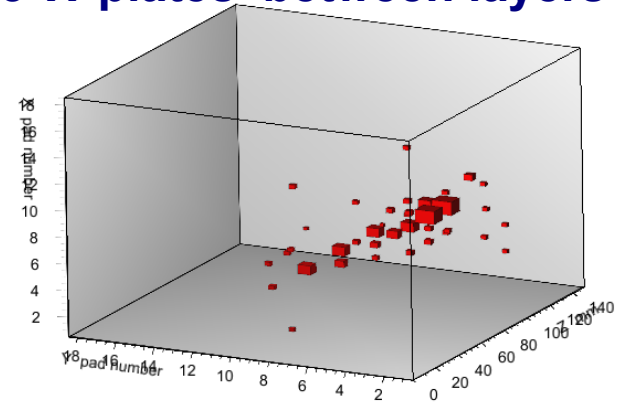 - Validate MC simulations

Event display

2 e- (3 GeV, no tungsten)
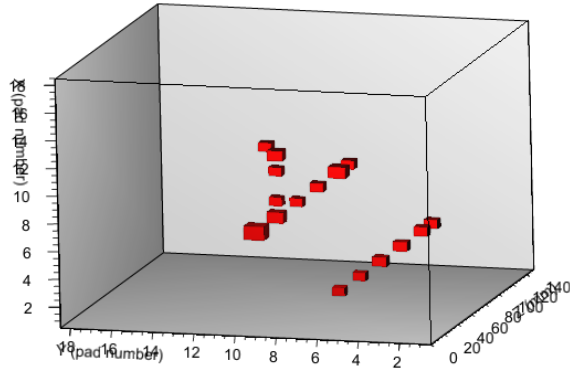
3 e- (3 GeV, no tungsten)
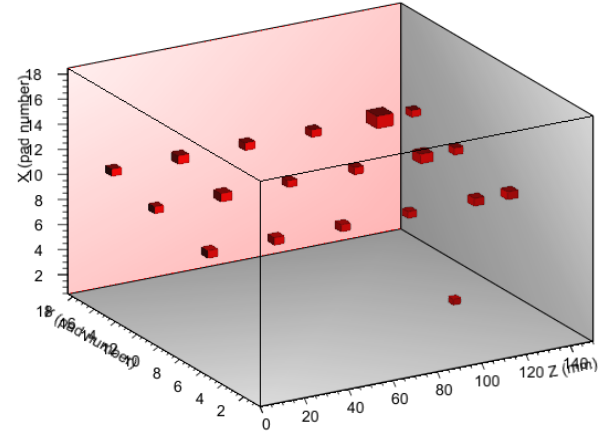
1 cosmic + 1 e- (3 GeV, no tungsten)

1 e- (5 GeV)
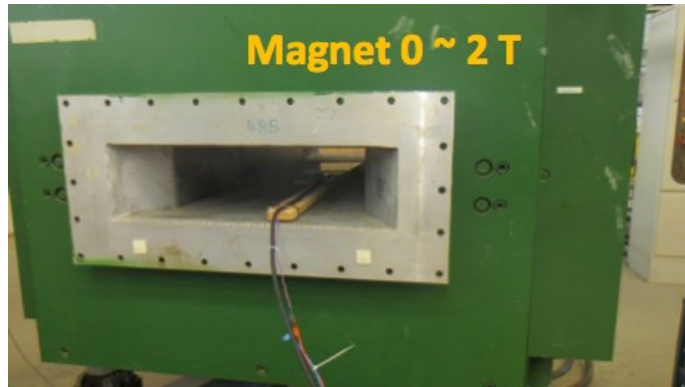**5 W plates between layers**

Power pulsing

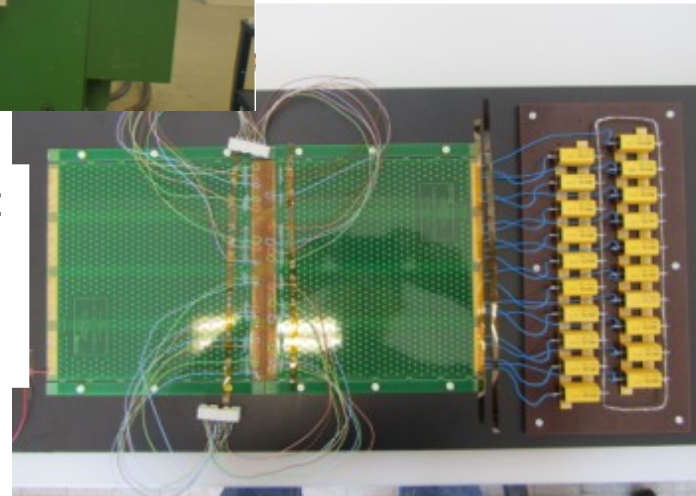Power pulsing (PP): duty cycle 99% , 10Hz

Operation in power pulsing mode requires removal of decoupling capacitances
→ Do not expect as stable performance as in continuous mode

Tests in magnetic field

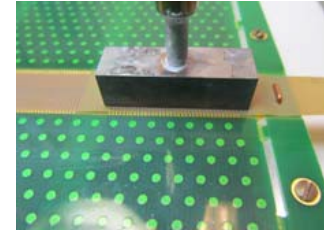Measurement of the pedestal in 1 layer

Interconnection (2 ASUs):
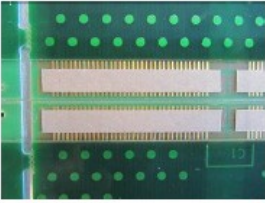Measurement of the ohmic resistance

Interconnexions

Up to 9 equipped PCBs interconnected to make detector slab

→ Electrical and mechanical connection made thanks to Kapton connecting cable

Technology	Advantages	Disadvantages
N°1 Solder	-Proven technology -Possible to repair -~3 euros/connector	-Difficult procedure -Too much heat for the glue of wafers -Cannot be industrialized
N°2 ACF	-Easy to install -Easy to remove -Easy to industrialize	-Needs to have a perfect planarity -Needs to have a thermode ~15Keuros -10mA maximum per wire -~30 euros/connector -Too much pressure =mechanical stress for the wafers
N°3 Spécial Kapton	-Easy to install -Good reliability -Possible to repair -Easy to industrialize -Good strength -~4 euros/connector	-I don't know yet

Max 600N before destruction
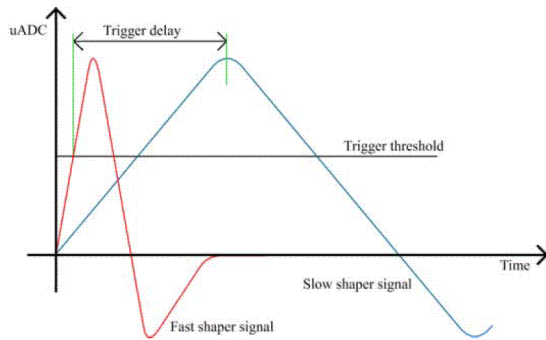

Signal integrity → In progress

Filtering

- **Ricochet / BCID+1 effect (without hit)**
  - Seen with SKIROC2 test bench and in TB
  - Understood
  - Easy to cut in TB analysis (cut event if delta BCID == 1)

- **Plane events**
  - Instabilities of power supply level → fake events
  - power supply common to the 4 ASIC, Self-sustained → sometimes filled all the 15 ASIC memories, Highly dependant of the number of ASIC with hits, dependant of the number of triggered channels
  - Cut in TB analysis:
    - delta BCID <= 5

- **Isolated hits**
  - Reconstruction needed to see this effect (not yet well studied: noise, cosmic, related to plane events?)
  - Cut in TB analysis:
    - we ask at least 3 planes with hits in the same event (after reconstruction)
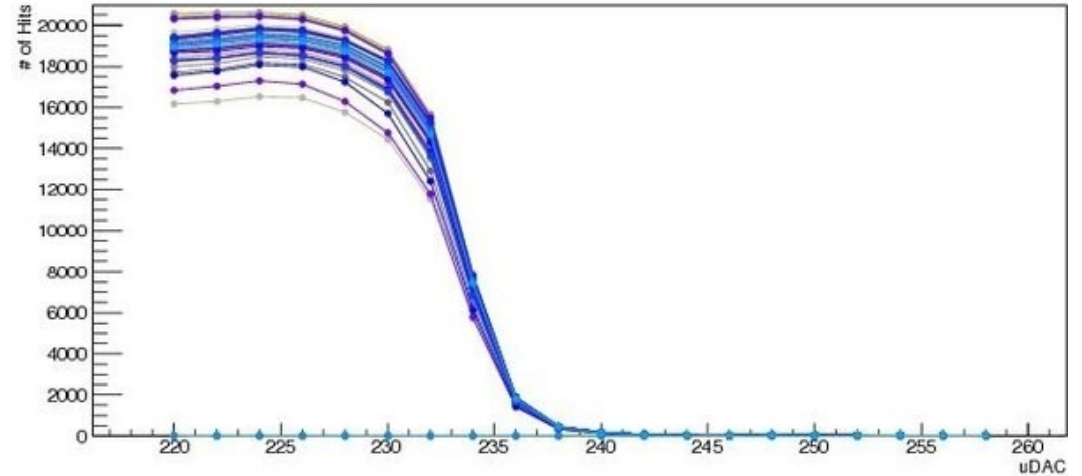
Calibration of ASICs

Establishment of calibration procedure for a larger number of cells
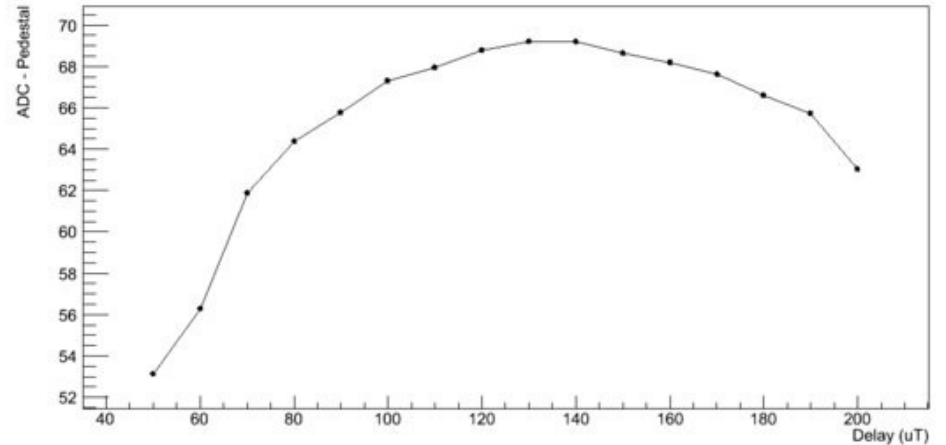
Trigger threshold
- depends on the gain

S-Curves for all the channels

Trigger delay
- depends on the trigger threshold

Holdscan - All SCA - Pedestal corrected

Signal over noise ratio

Gain : 1.2pF - SigmaDet = 4.90 - Signal over Noise ratio = 14

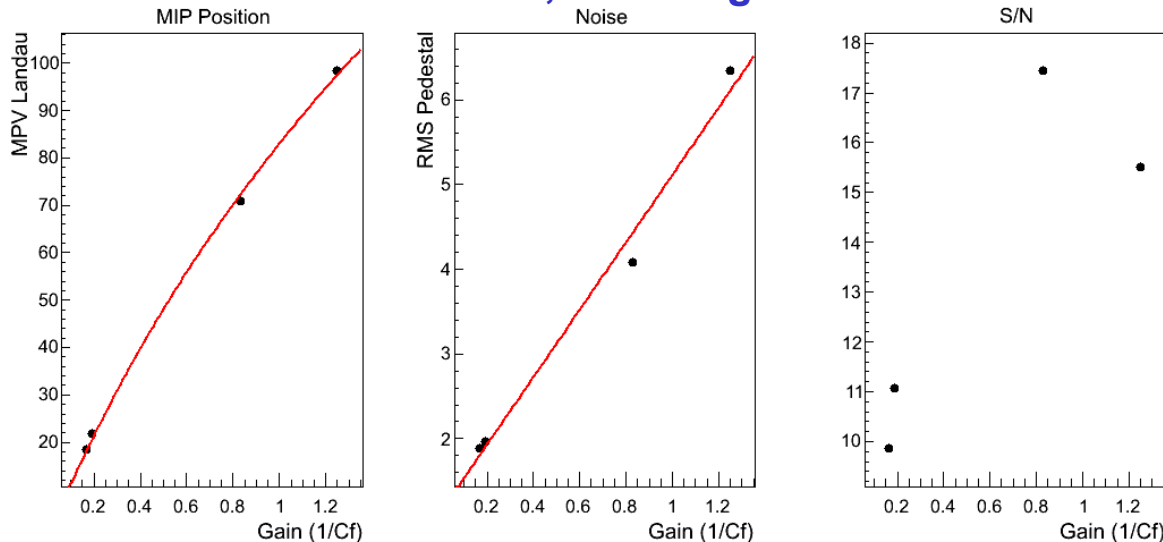| Chip4_Channel_62_hit	
Entries	1397
Mean	389
RMS	23.73
χ^2 / ndf	177.6 / 152
Constant	21.79 ± 1.33
MPV	379.8 ± 0.3
Sigma	4.324 ± 0.241
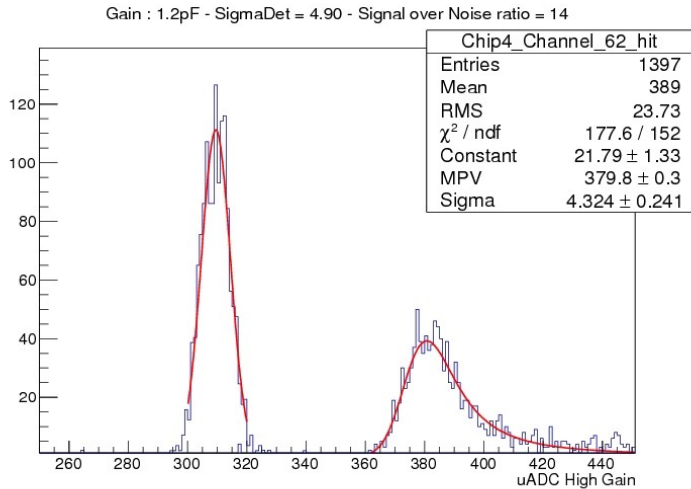
All channels, 1 gain (Cf = 1.2 pf)
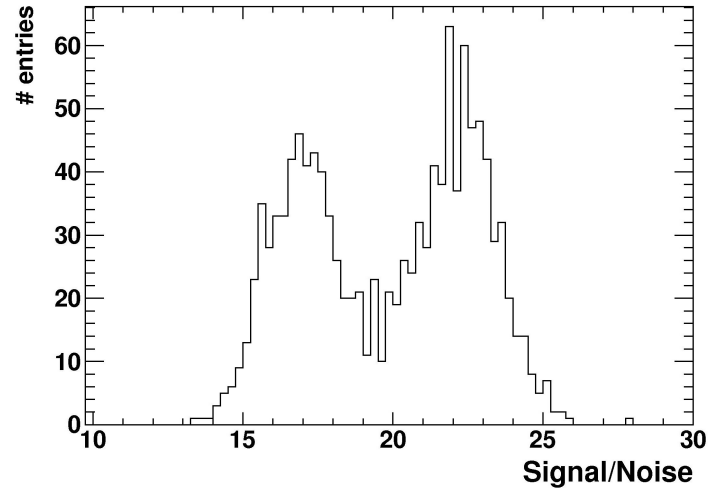
1 channel, several gains

R&D target is 10:1

S/N ≥ 10
(for all gains available with SKIROC2)