Development of a TPC readout based on GridPix

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CLIC Workshop
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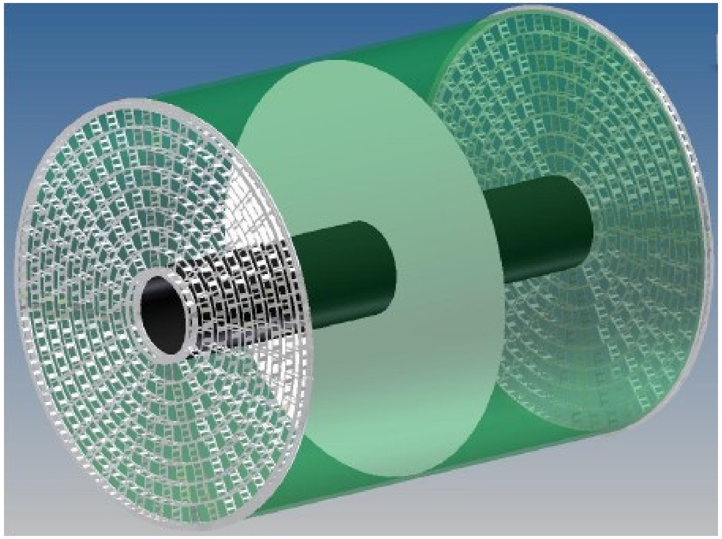
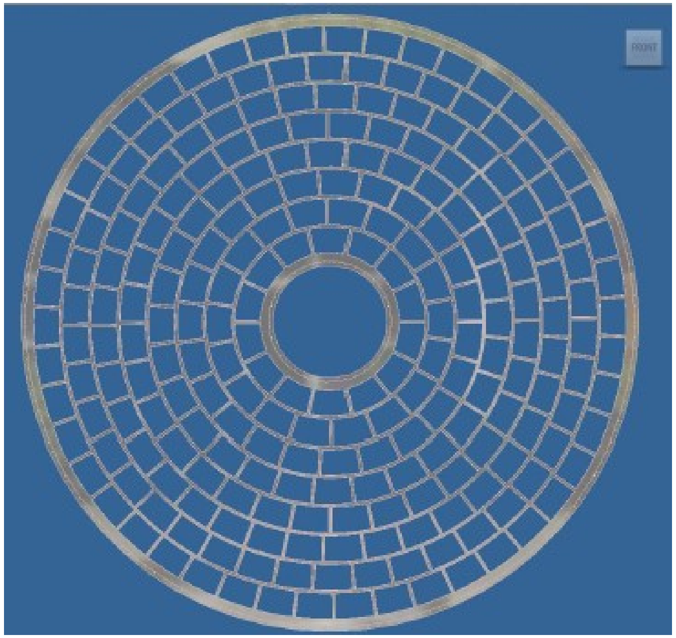
TPC for CLIC





One of the two detector concepts described in the CLIC CDR foresees a large TPC as a central tracking device.

<u>Advantages are:</u>

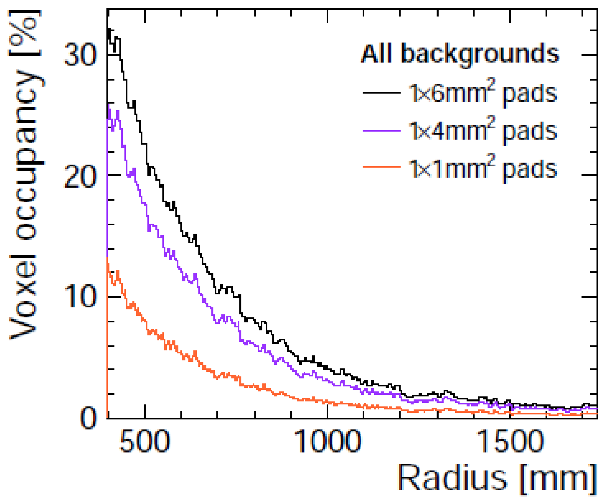
1.) continuous tracking
2.) minimum amount of material budget in barrel region
3.) topological time stamping
4.) reconstruction of non-pointing tracks
5.) dE/dx

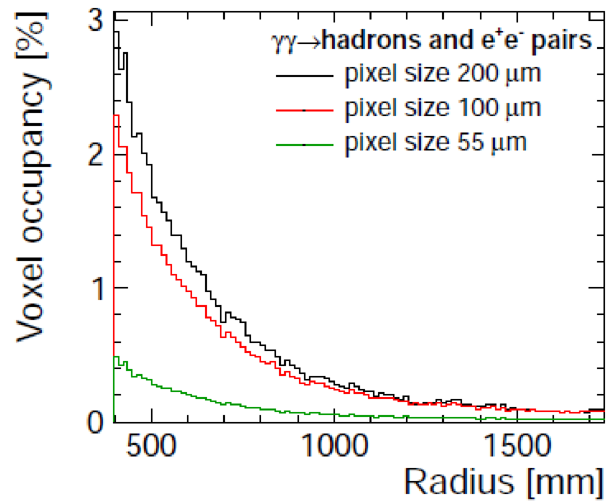
<u>Current design:</u>

Inner/outer radius 329/1808 mm
Maximal length 2250 mm
size of endcaps ~10 m^2
8 rows of MPGD detector modules;
module size ~17×23 cm^2
240 modules per endcap

Occupancy

The beam induced background
($\gamma\gamma$ → hadrons, e^+e^- → pairs and beam halo muons)
is accumulated in the TPC creating a significant occupancy
(Simulation for the CLIC detector, M. Killenberg, LCD-Note-2013-005)

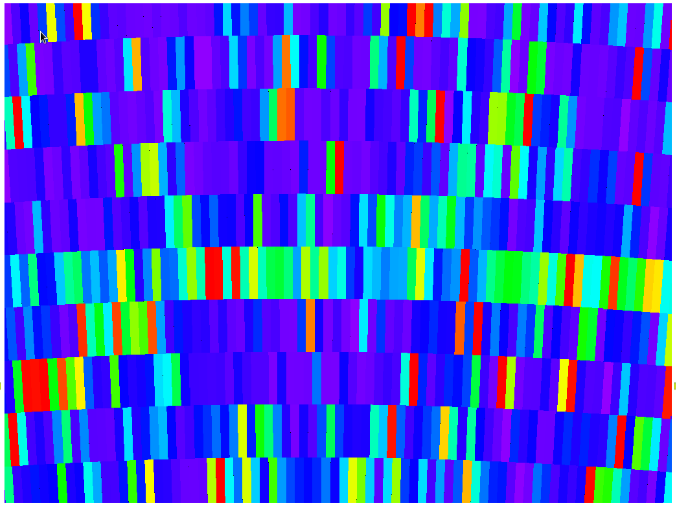




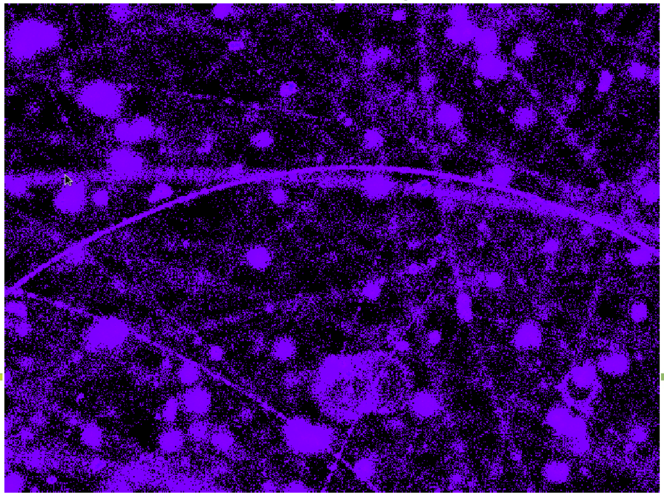
For standard readout pads with a size of several mm² high occupancies are expected.

⇒ Need to go to smaller pixel sizes (50-200 µm)

1×6 mm^2 pads

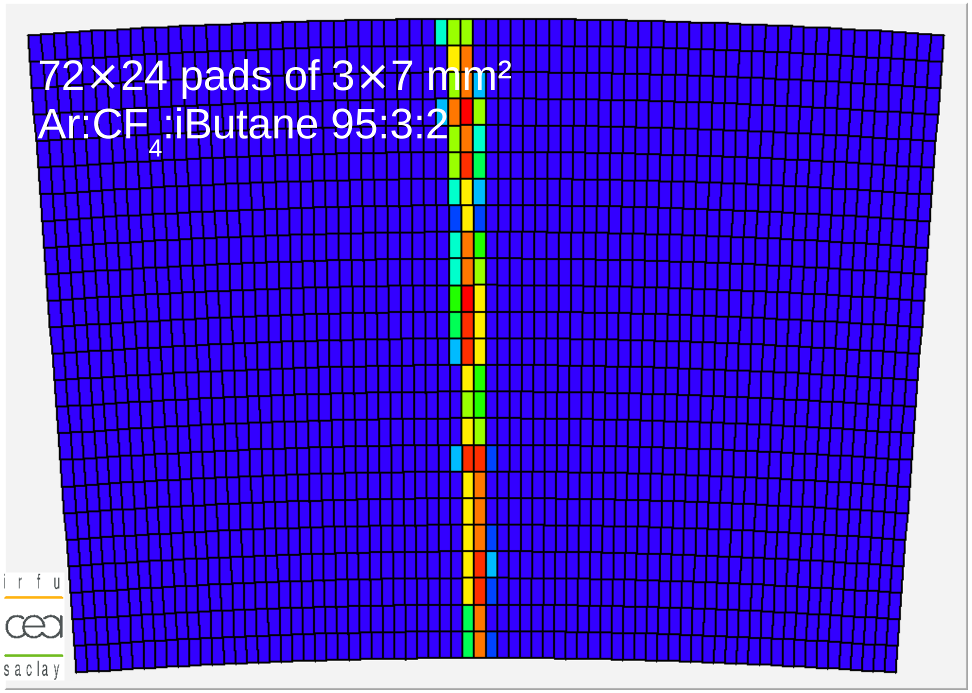


100×100 µm^2 pixels



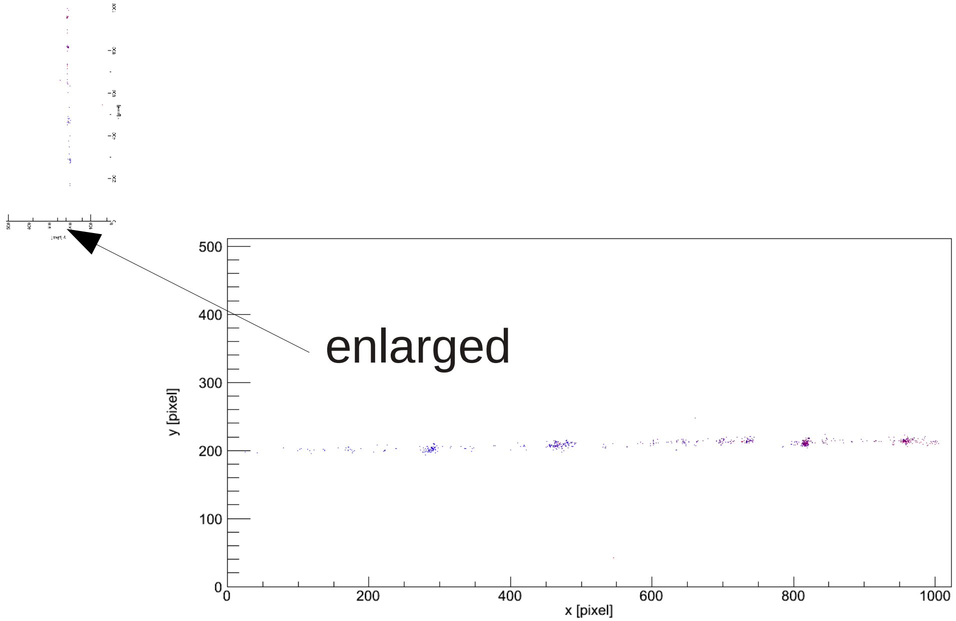
Pixelated TPC

Standard charge collection: Pads of several mm²



To readout the TPC with GridPixes:
~100-120 chips/module
→50000-60000 GridPixes

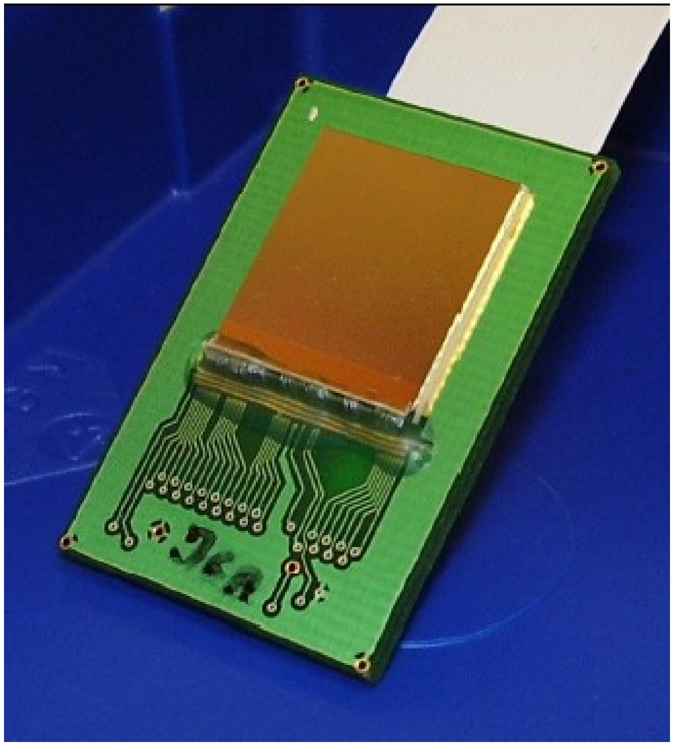
8 GridPixes
B = 1 T
Ar:CF_4:iButane
95:3:2

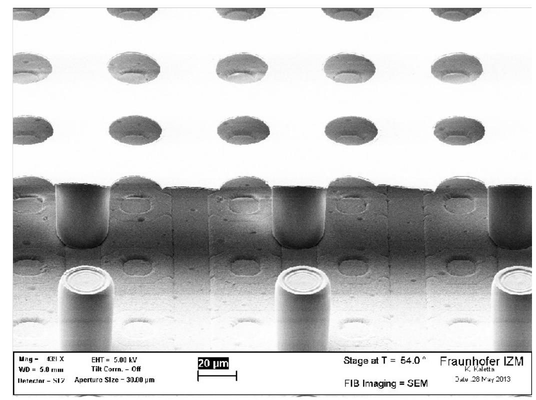


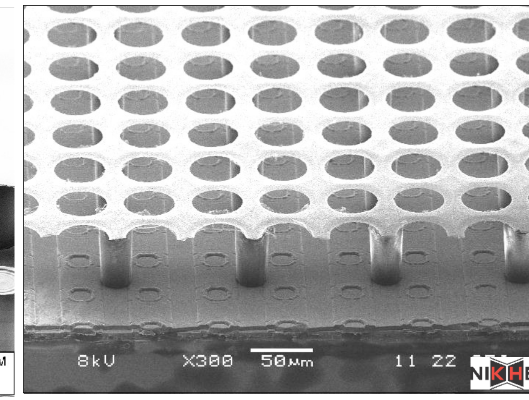
- Lower occupancy
  → better track finding
- Identification and removal of δ-rays and kink removal
- Improved dE/dx, because of primary electron counting
- Pad plane and readout electronics fully integrated

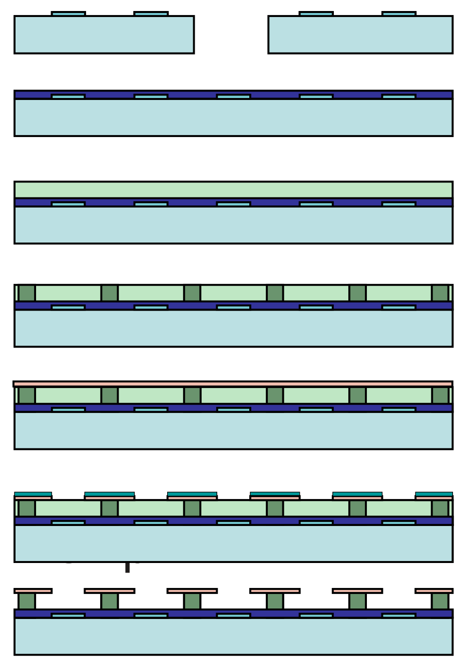
GridPix

Micromegas ontop of a pixelized readout chip: bump bond pads for Si-pixel detectors serve as charge collection pads.









1. Dicing of Wafer
2. Formation of Si_xN_y protection layer
3. Deposition of SU-8
4. Formation of pillar structure
5. Deposition of thin Al layer
6. Formation of Al grid
7. Development of SU-8

Timepix derived from Medipix-2

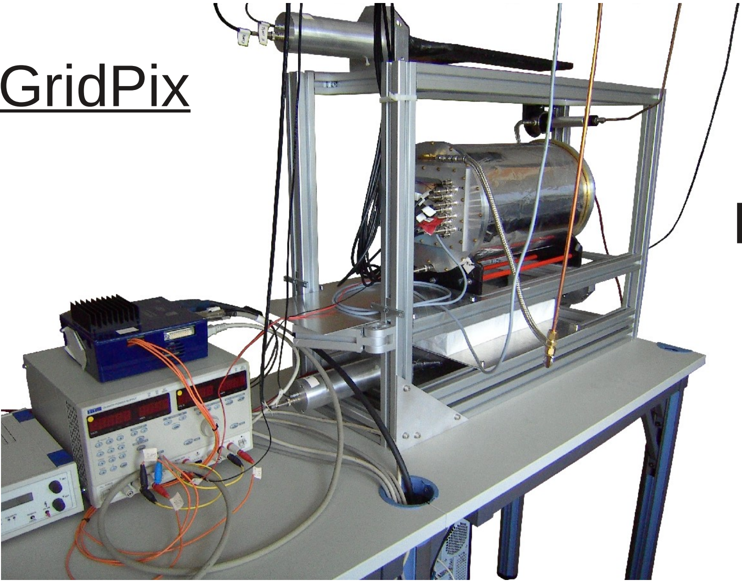
256 × 256 pixel of size 55 × 55 µm²

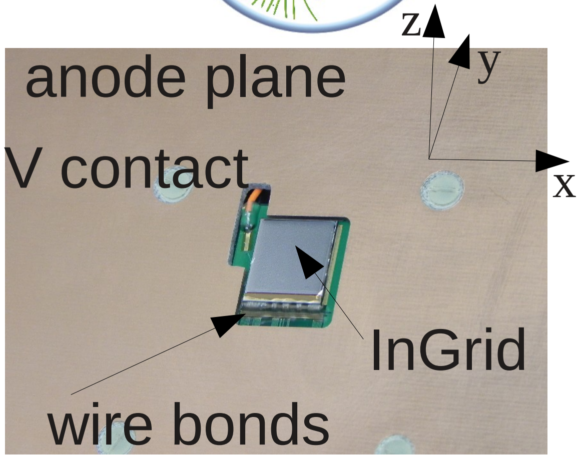
Each pixel can measure either arrival time or charge.

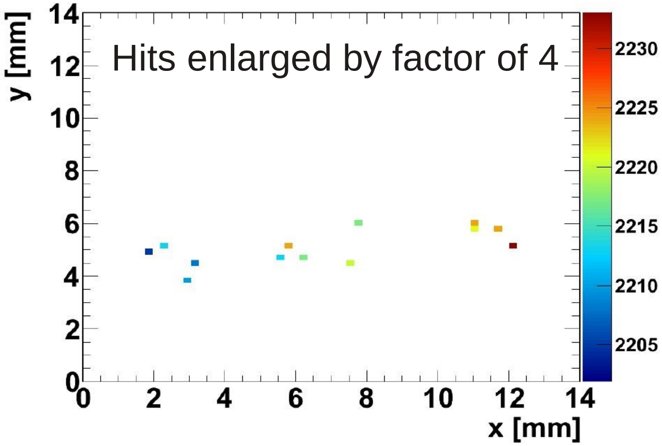
Noise is ~ 90 e^- (ENC)

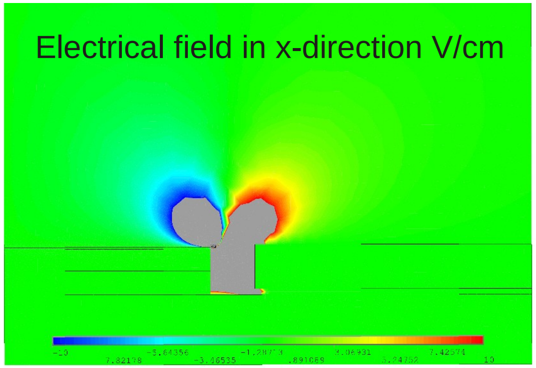
Proof of Principle

<u>Prototype detector with 1 GridPix</u>
Max. drift length: 26 cm
Measures cosmic muons
Drift field: 450 V/cm
Gas: He:CO_2 (70:30)

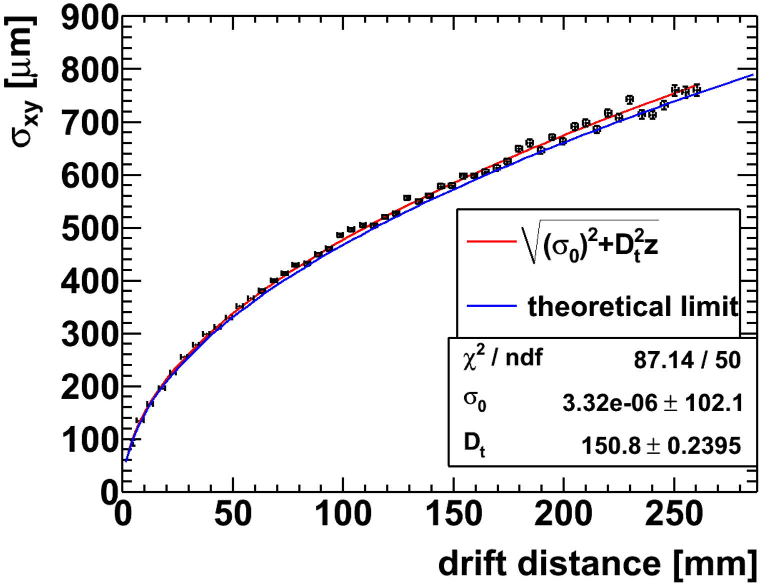








Spatial resolution on the area not affected by field distortions (~1/3 of chip).



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Towards a full TPC Module

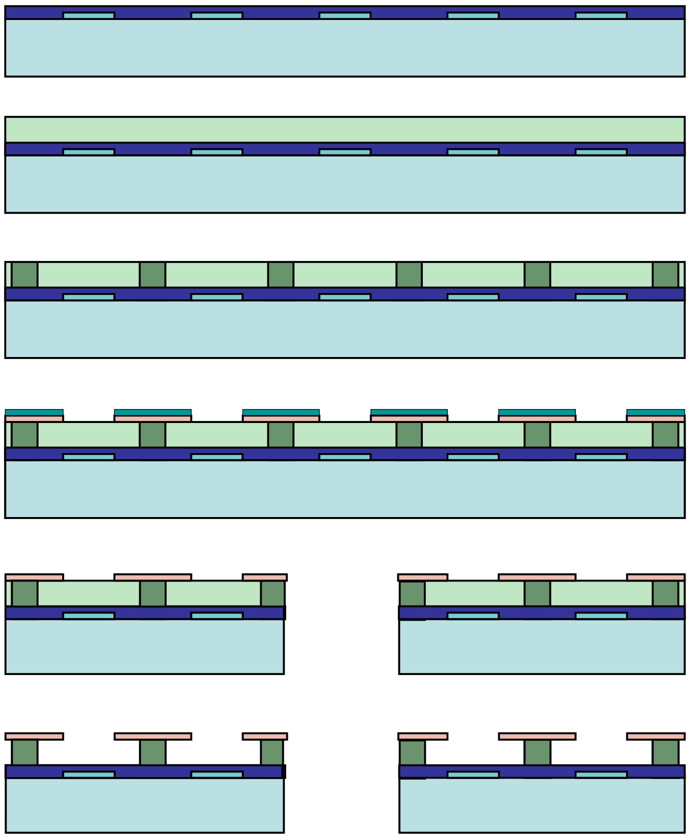
Principle of a highly pixelized readout has been demonstrated successfully!
Now increase the number of chips to 8 (also accomplished), then 100.

But what is missing for application in particle physics experiments?

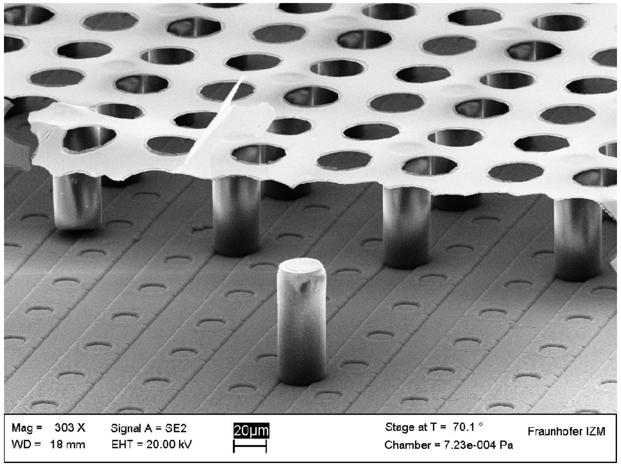
1. Mass production of GridPixes → Production at IZM
2. Adapted readout system → SRS system
3. Deal with field distortions (correction and/or anode/guard-ring)
4. Cooling
5. LV-power supply
6. Better chip → Timepix-3

Wafer production of GridPixes

Production at Twente was based on 1 - 9 chips process.
This could not satisfy the increasing demands of R&D projects.
New production set up at the Fraunhofer Institut IZM at Berlin.
This process is wafer-based → 1 wafer (107 chips) is processed at a time.



1. Formation of Si_xN_y protection layer
2. Deposition of SU-8
3. Pillar structure formation
4. Formation of Al grid
5. Dicing of wafer
6. Development of SU-8



Results Wafer scale Production

1. batch (10/2011): Problems with resistive layer and Al-grid

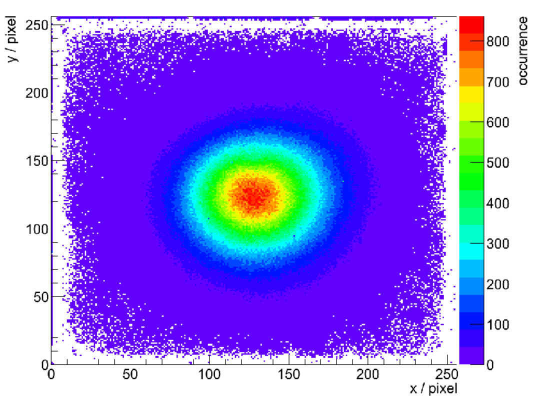
2. batch: GridPixes worked well, good energy resolution ($\sigma_E/E{\sim}7\%$)
(12/2011) Resistive layer proved vulnerable (chips died after 2 weeks)

3. batch: Chips survived many thousand X-ray-induced sparks
(9/2012) But 7 out of 10 chips died in a hadronic test beam at CERN

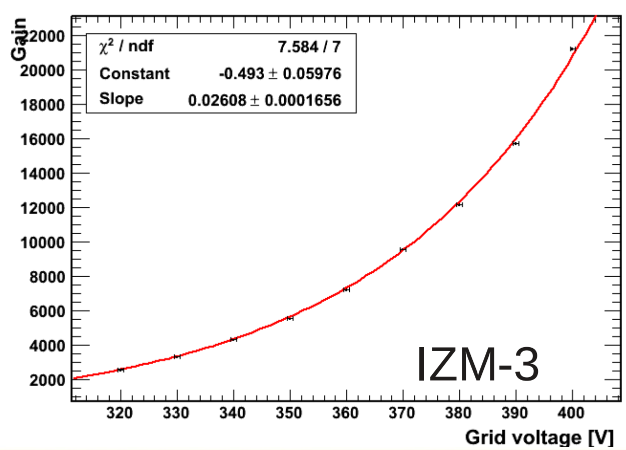
4. batch: 4 wafers with different resistive layer thicknesses (4 µm, 8 µm)
(12/2012) Problems with the production (machine failure)
→ only few good chips

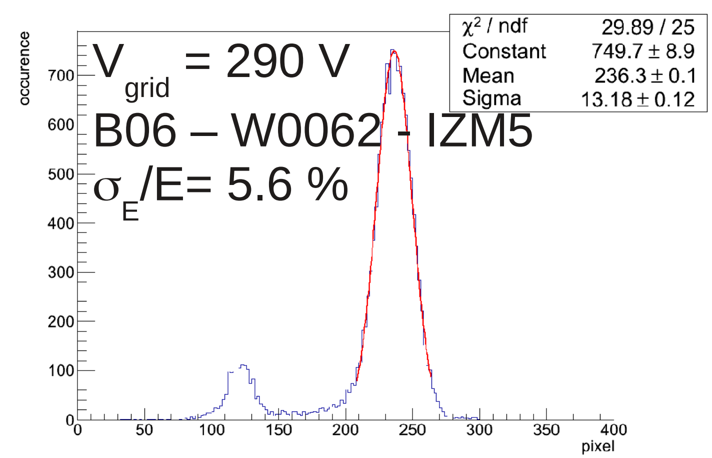
5. batch: still under investigation, chips show good performance, but stability
(8/2013) yield unclear yet

6. batch: planned, 4 wafers for the full module



F01 with V_{grid} = 300 V

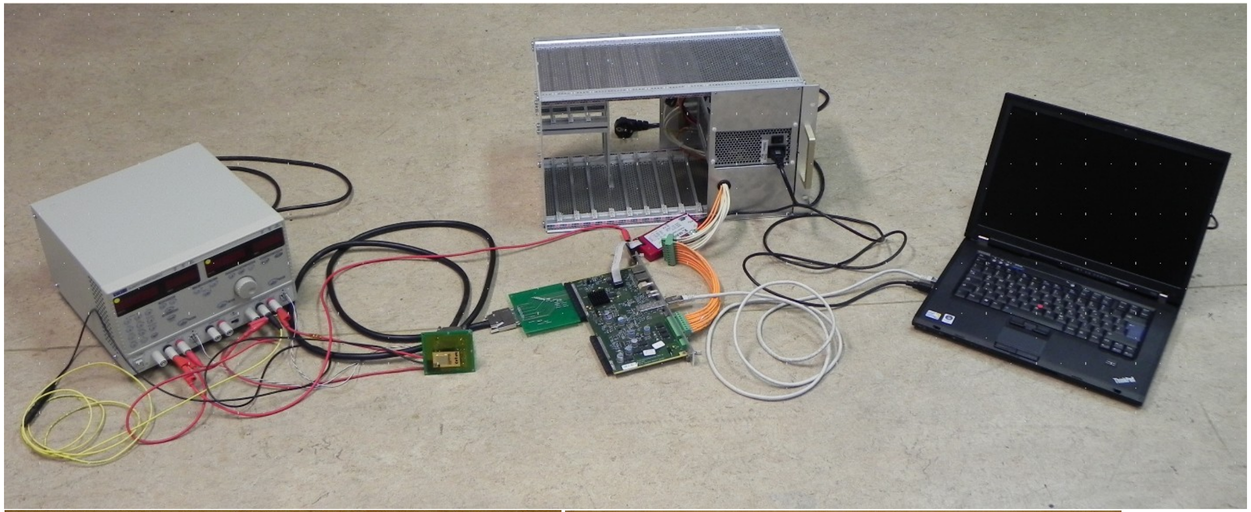


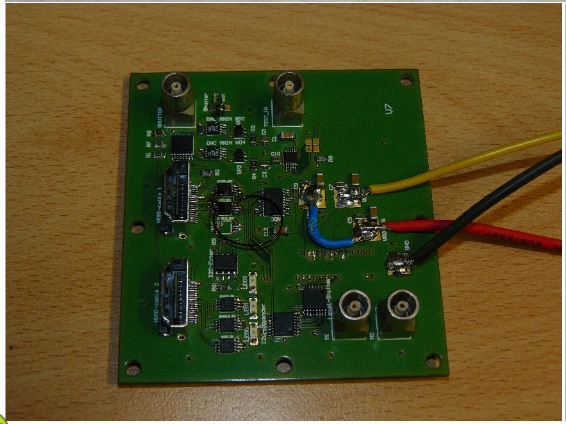


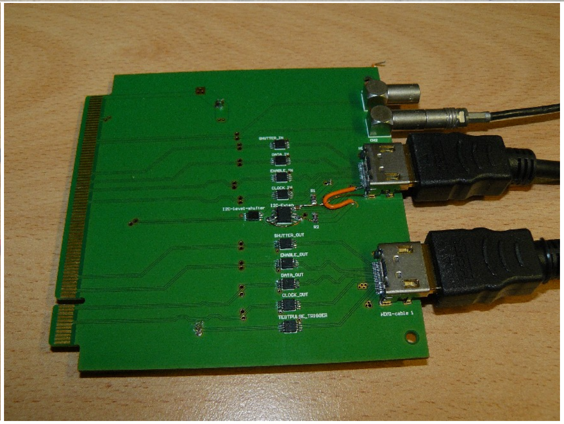
Electronics for 100 Chips

The Scalable Readout System is designed by the RD51 collaboration with CERN as a main developer.

Idea: produce a flexible readout electronics, which can handle different chips (new FPGA code, chip carrier), which many groups can use



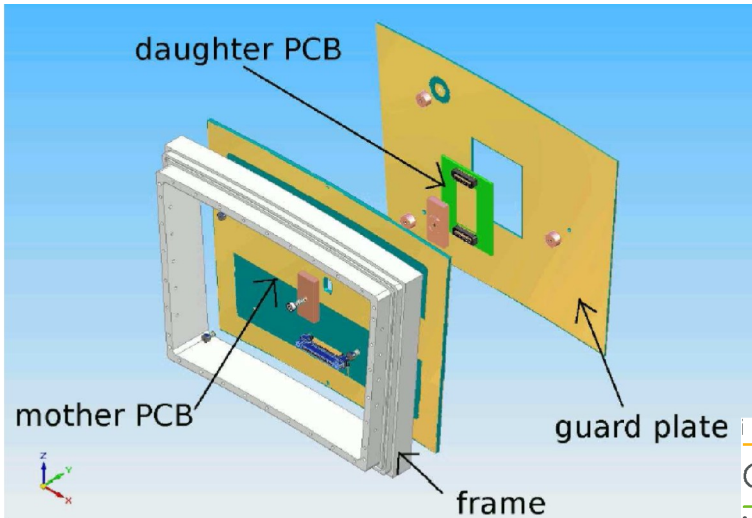




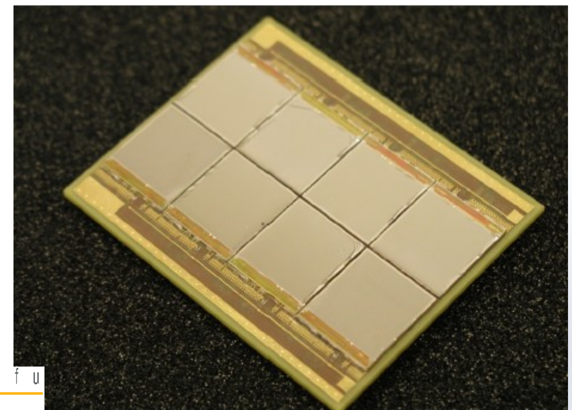
U. Bonn is developing a readout for the Timepix chip.
Operation has been demonstrated for a eight chip.
All functionality is available.
Some functions still have to be tested and implemented in the software.
Next steps, scaling to more than 8 chips.

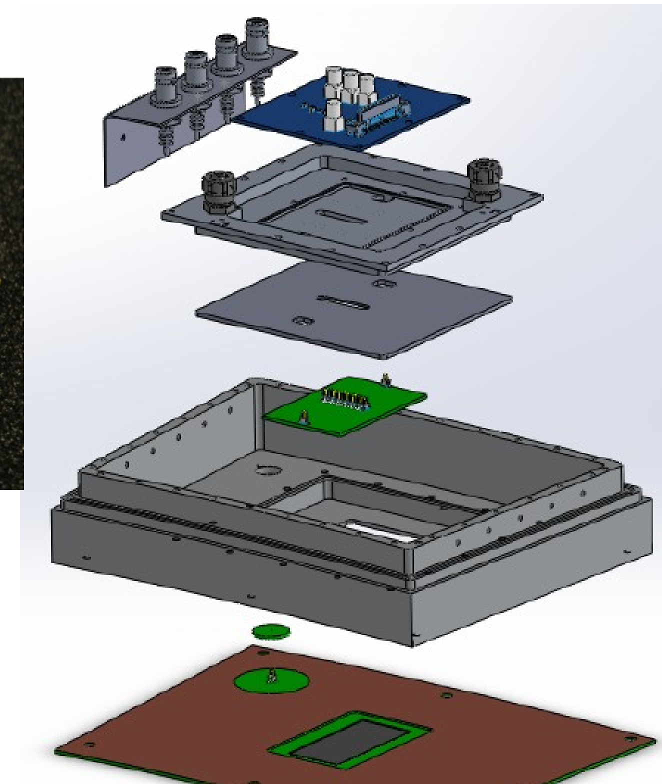
Test Modules with Octoboard

2 LCTPC modules with 8 GridPixes have been built:
one in NIKHEF/Saclay and one in Bonn



irfu cea saclay





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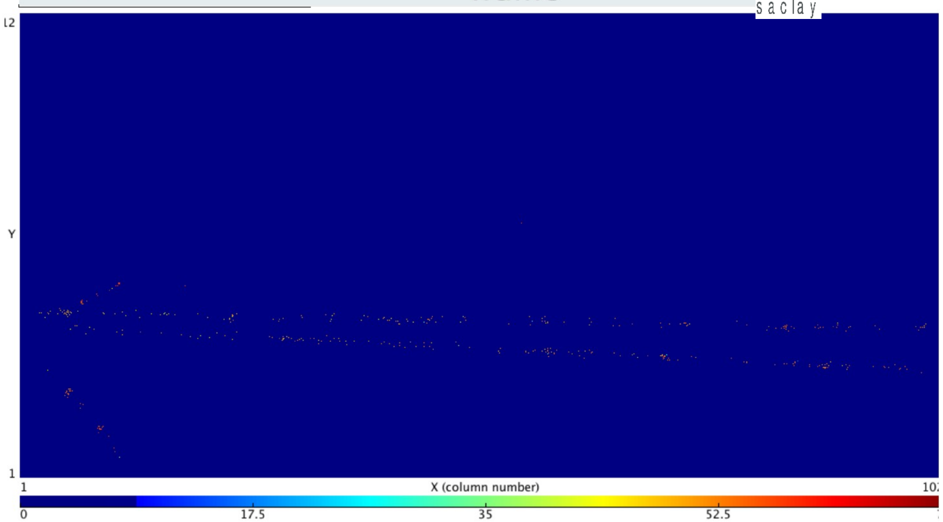
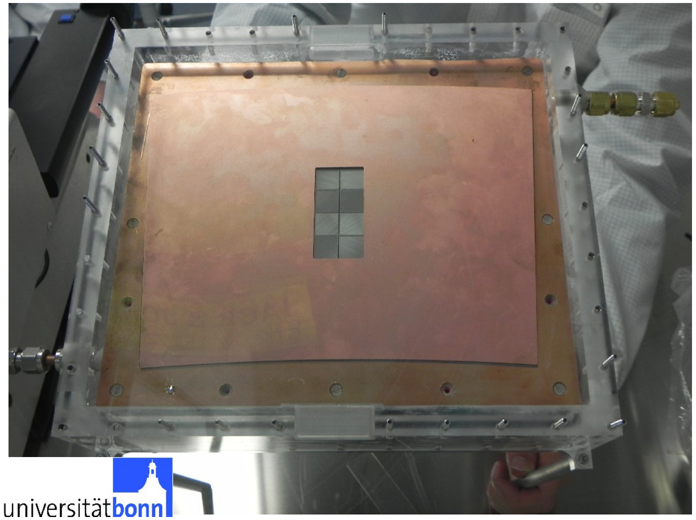
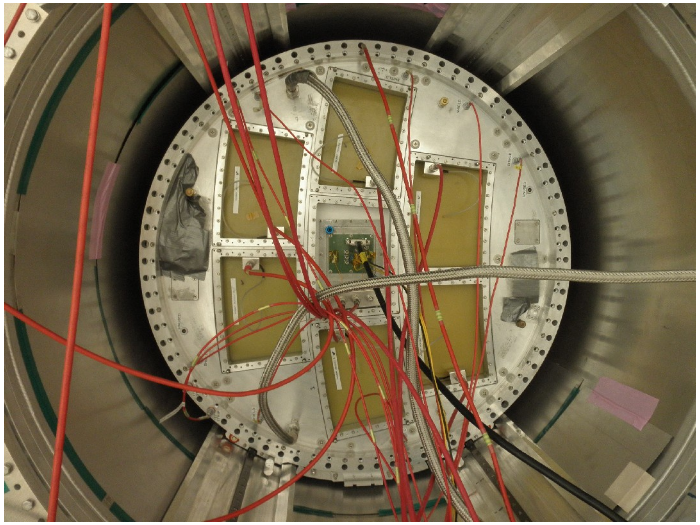


Both modules have successfully been tested in the 5 GeV test beam at DESY.

Test beam at DESY

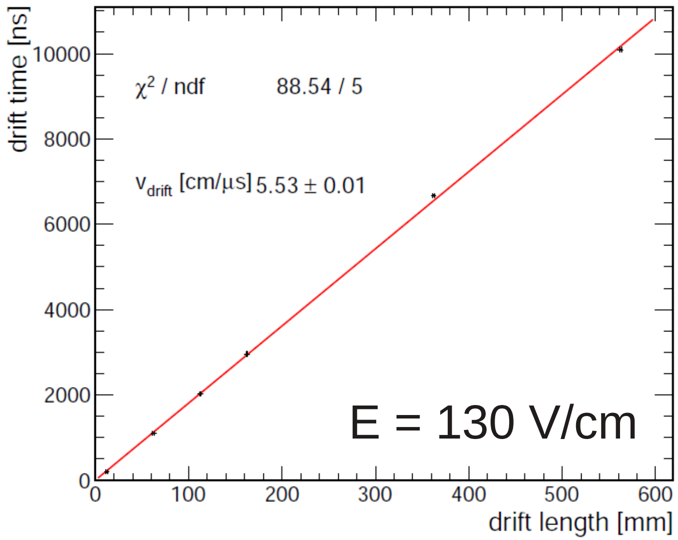
EUDET/AIDA setup:
- Electron test beam
  with beam energy 1-6 GeV
- Solenoid with B < 1.25 T
- Movable support structure
- Field cage
- Cathode
- End plate with space for 7 modules
- Readout electronics
- Slow control

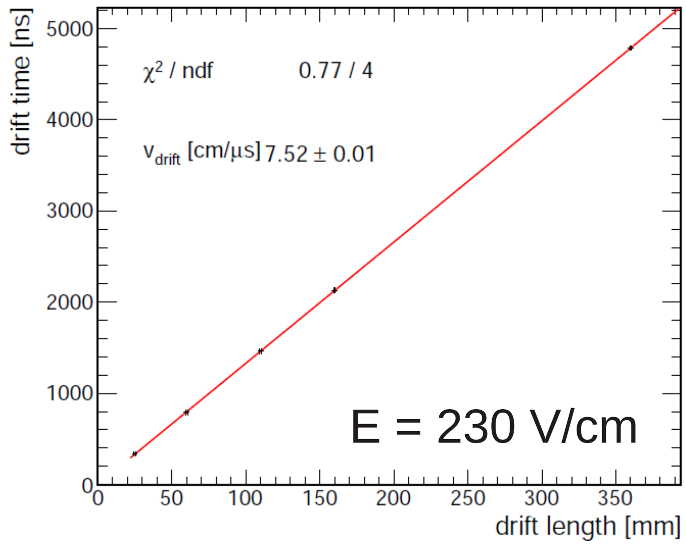


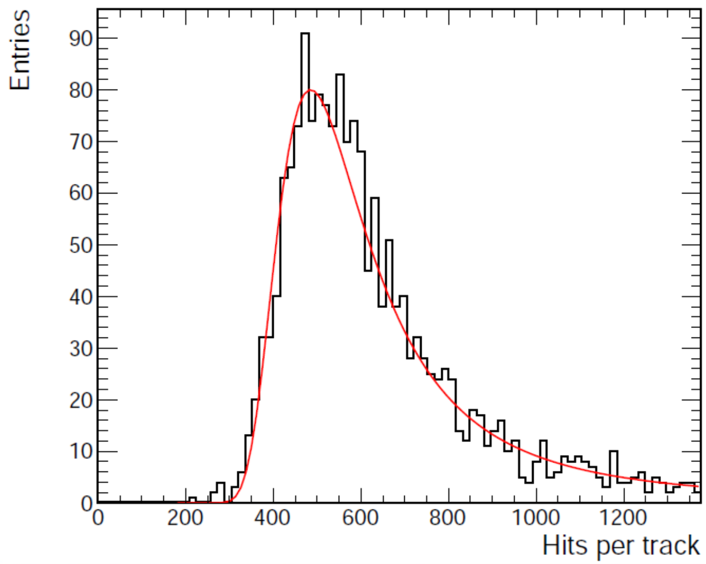


Test beam results – 1

Drift velocity in good agreement with simulation results.

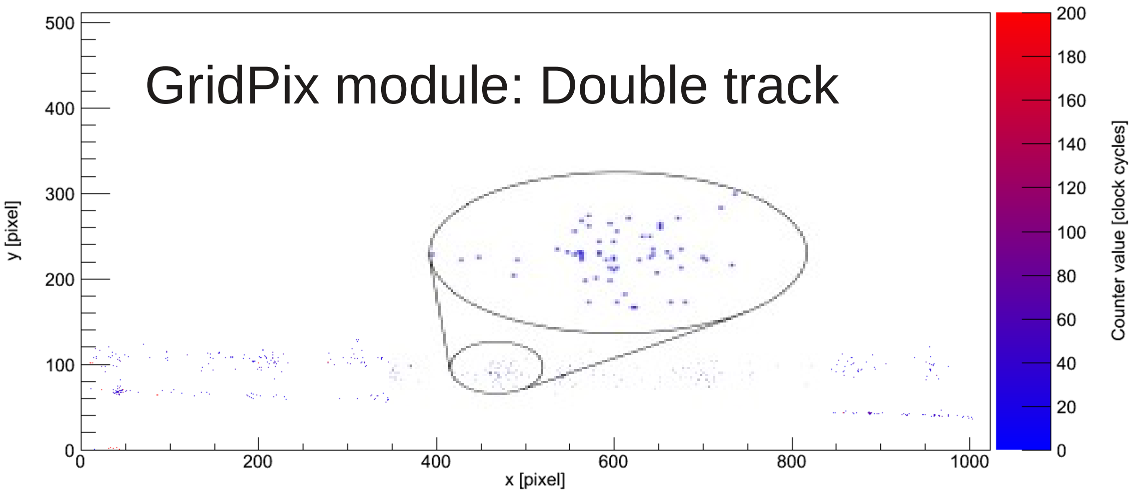




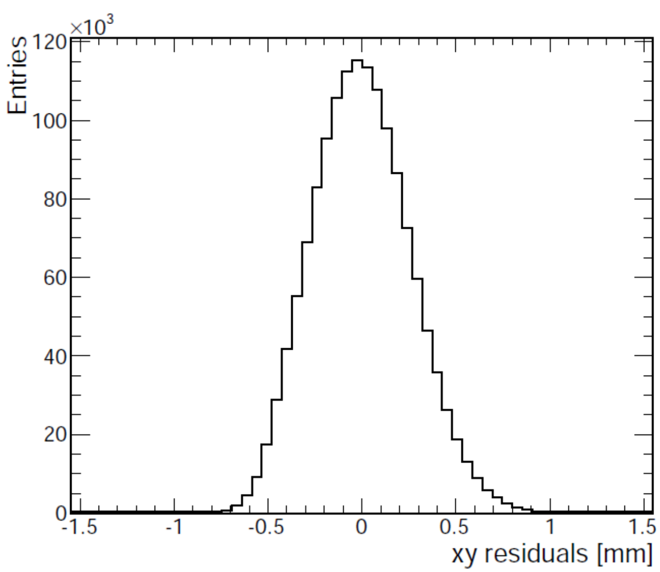


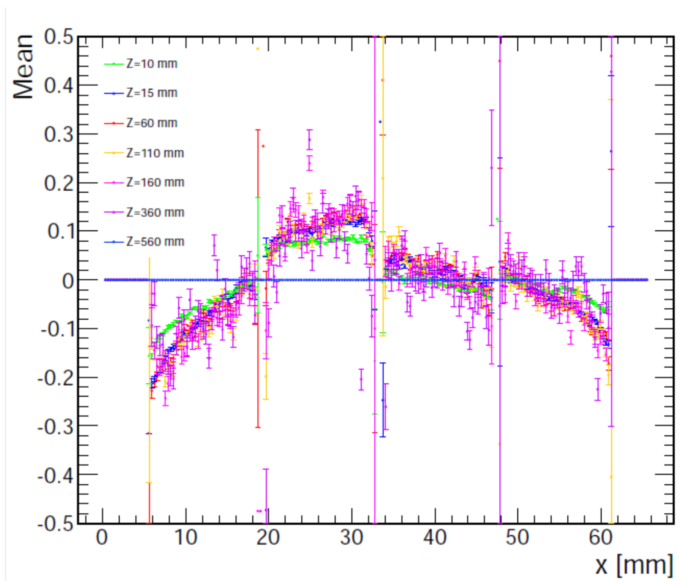
- Hits per tracks are main indicator for a detectors resolution
- Expectation value for GridPix octoboard: 538
- Measured: 513 ± 3

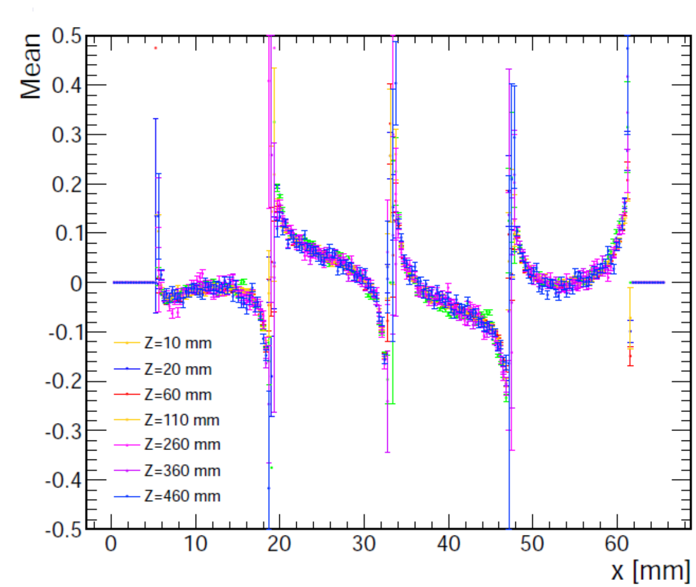
Test beam results - 2



- 10^6 events recorded with GridPix octoboard
- Analysis is stagnating currently
- Field distortions at the boarder of chips are clearly visible and changes with B-field.

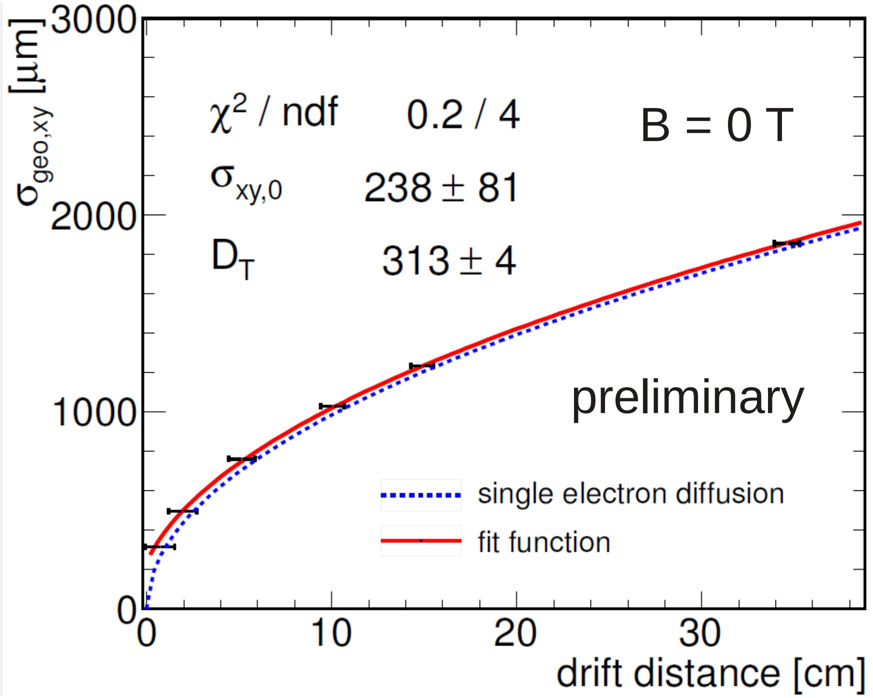


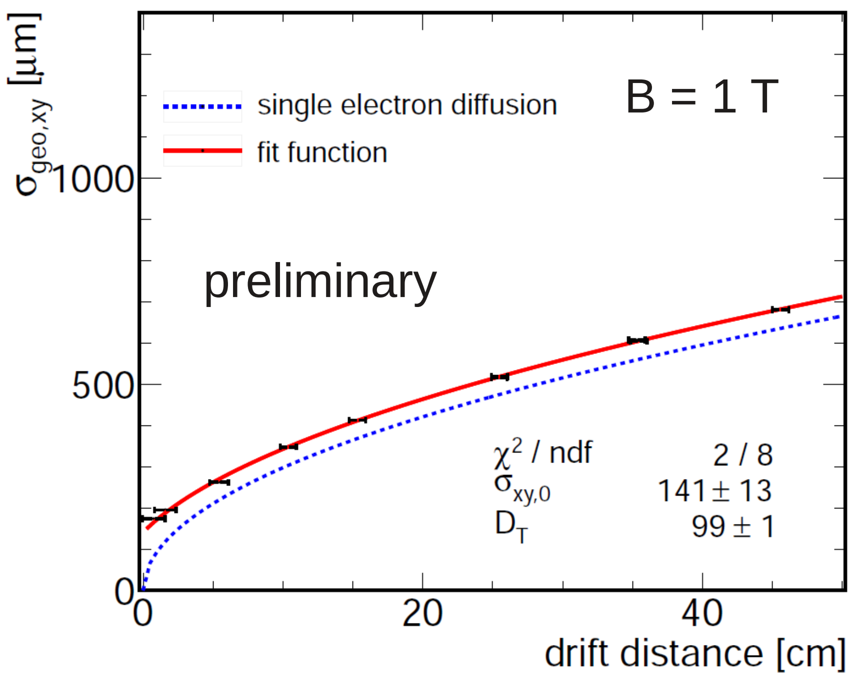




Test beam results - 3

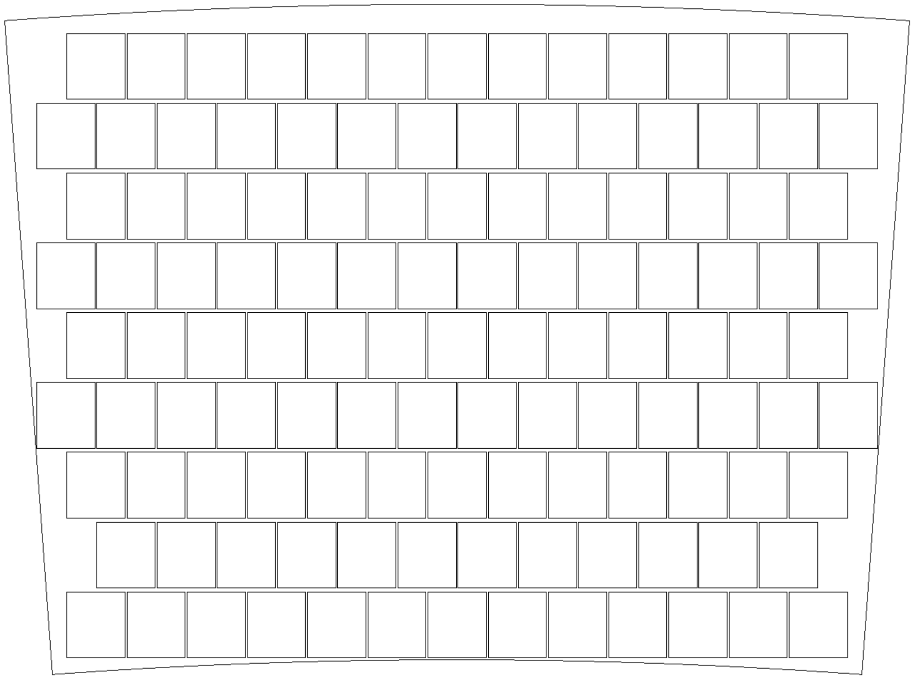
Spatial resolution in dependence on the drift distance:
NO correction for field distortions!

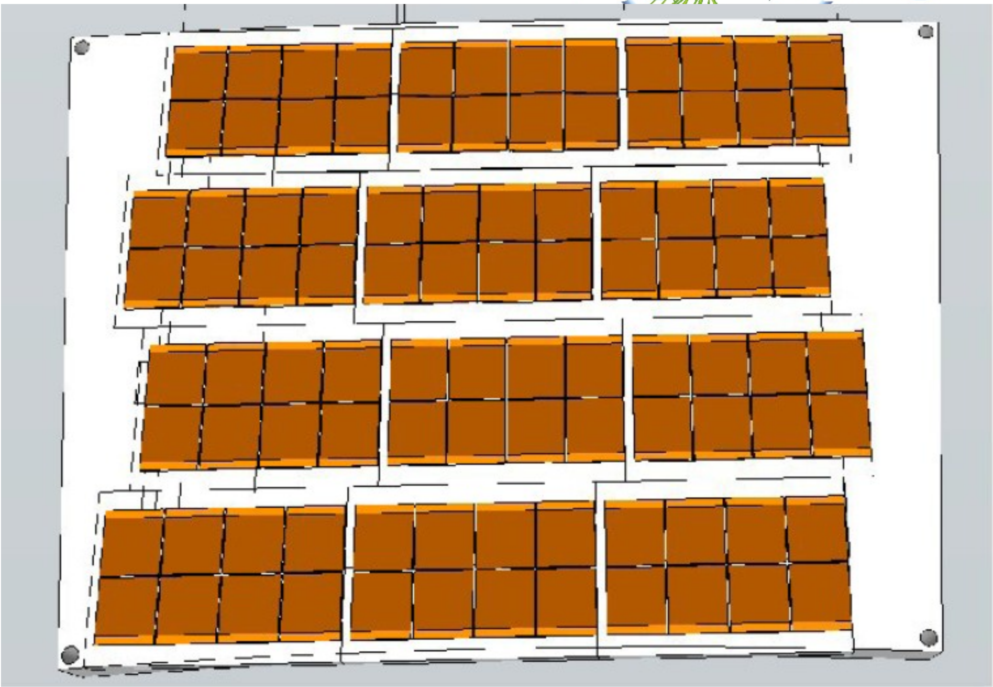




Good agreement with diffusion coefficient,
but large σ_0 because of field distortions.

Towards a 100 chip module





Planning for a 100 chip Module are starting, currently looking at:

- Modular structure – which is the base-unit? 4-8?
- How do we cool? Water or 2PCO2? Can we have a 100% duty cycle?
- HV distribution, connection...

For later versions:

- “flipped-chip” mounting of FPGA for N GridPixes
- TSV, Timepix-3

Timepix-3

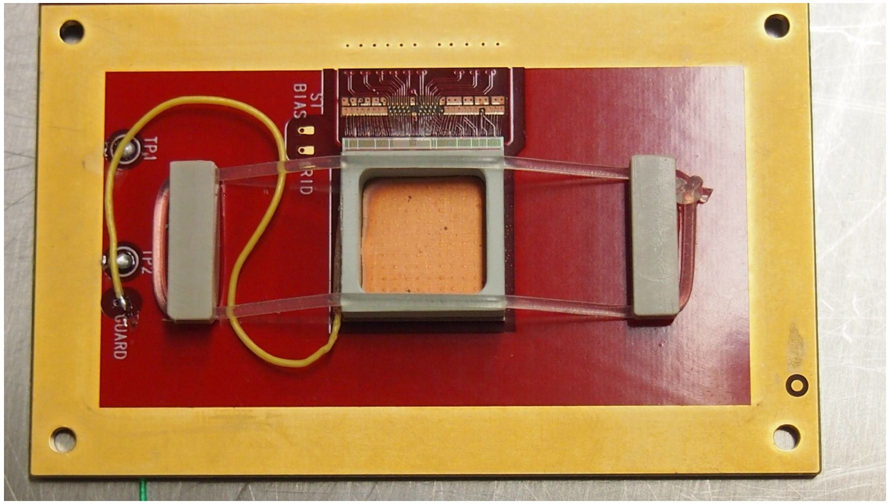
Timepix-3 has been produced.
Specs see table (from:
Timepix3 Designer Manual v1.0)

Most importantly:
- Charge and time are available for every pixel,
- Multi-hit capable
- Very high output rate: 8×640 MHz
- Time resolution of ~1.5 ns

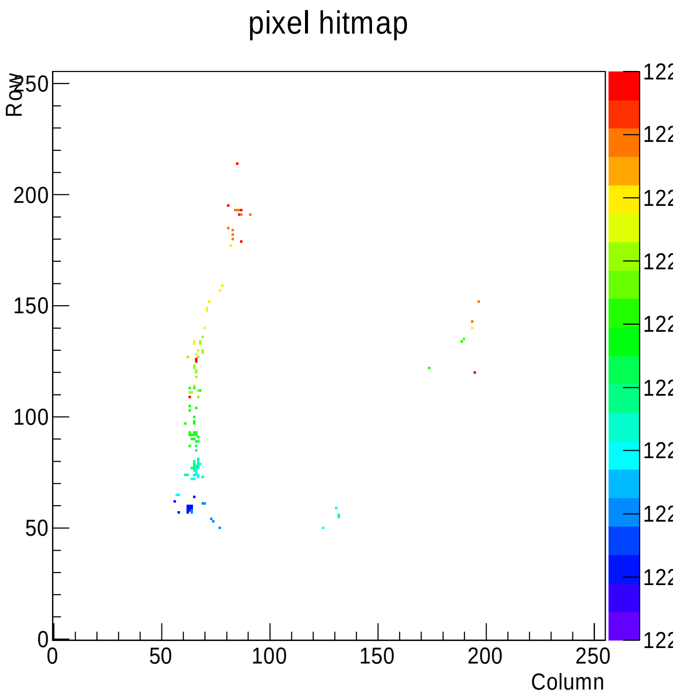
Delivered in fall 2013.
Tests have shown no problems yet.

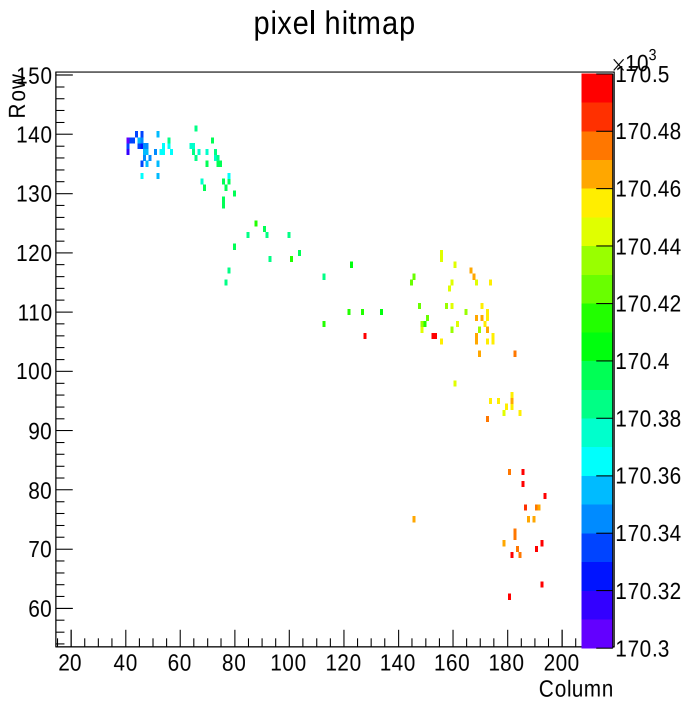
General Requirements	
Pixel size	55 µm x 55 µm
Pixel matrix array	256 x 256
Target floorplan	3 sides buttable and minimum periphery
Highly Configurable	HEP platform for many projects
Time stamp and TOT recorded simultaneously	YES
No event counting mode	Only for testing
Technology	IBM 130nm DM 4-1
Power consumption	<1.5W/cm^2 (~45 µW/pixel) @1.2 V
TSVs possibility	YES
Chip Readout Modes	
Data-driven readout (token pass)	YES
Zero-suppressed and Sparse data readout	YES
Dead time free	YES (if moderated count rate)
Time Stamp	
Global Time stamp (bunchID)	40 MHz (25ns)
Global Time stamp range	14bits (409.6 µs)
Accurate Time stamp per pixel	4bits → 1.56ns resolution (640 MHz)
Local Oscillator frequency	640 MHz
On-pixel local oscillator tuning	Locked using periphery PLL
TOT	
TOT Clock reference	40 MHz (25ns)
TOT range	10 bits
Periphery	
Analog Blocks	Band-Gap, DACs and Test Pulse
E-fuses (chip ID, hard-wire configuration)	YES
Programmable PLL	40 → 40, 80, 160, 320, 640 MHz
Periphery/output clock	40, 80, 160, 320 MHz
RO architecture	[1 ... 8] LVDS DDR 8b/10b Encoding

MM detector with Timepix - 3



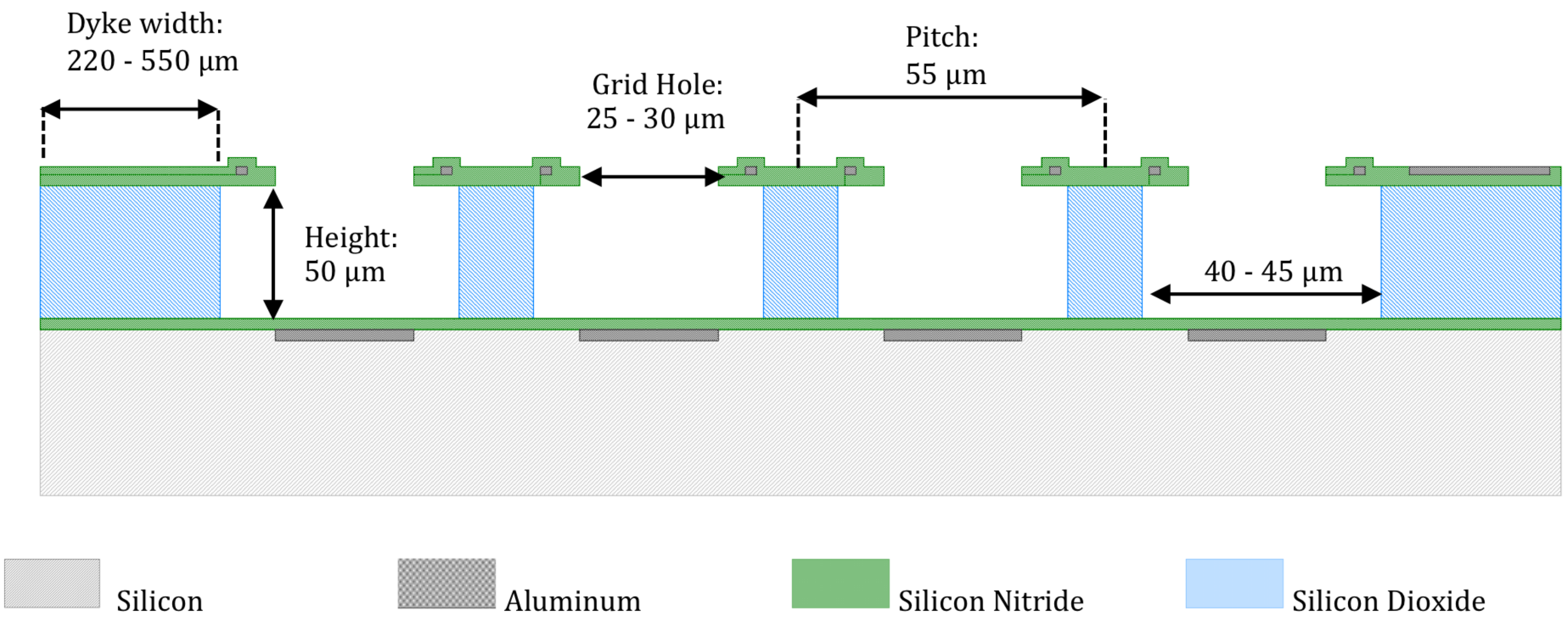
Drift gap: 8 mm
Pillar height: 50 µm
Pitch of holes: 60 µm
Gas: He:iButane 95:5
Source: ^{90}Sr
The chamber unit is read out by a Spidre prototype.





More advanced grids

All ceramics InGrids



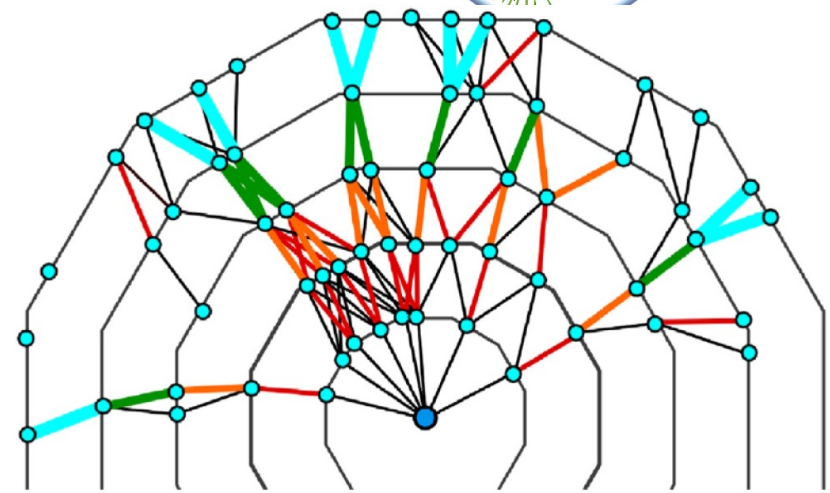
- Double discharge protection
- Equal coefficient of thermal expansion throughout GridPix: Needed for operating in cryogenic environments
- No outgasing: Plastics (like SU8) outgas and can not be used in ultra clean (cryogenic) environments
- Different pillar structures are possible.

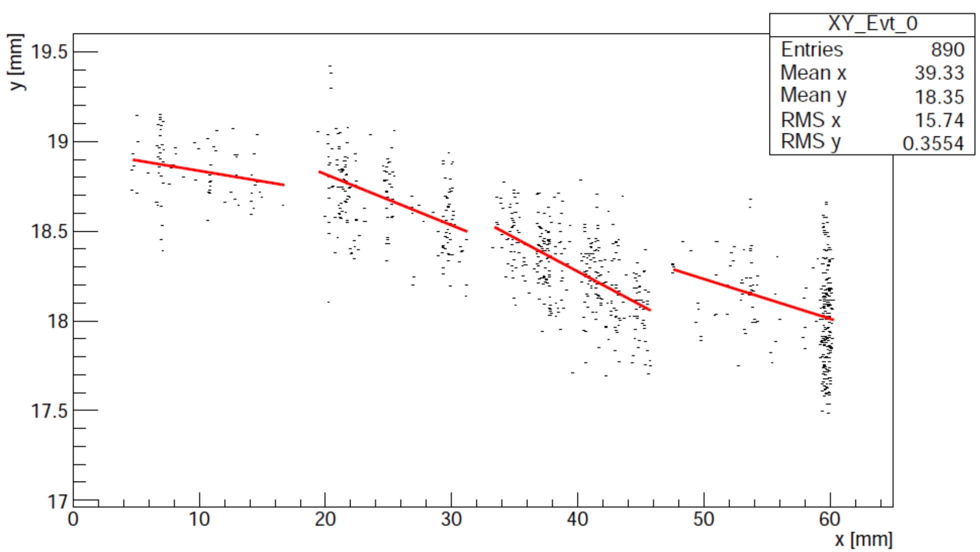
Reconstruction

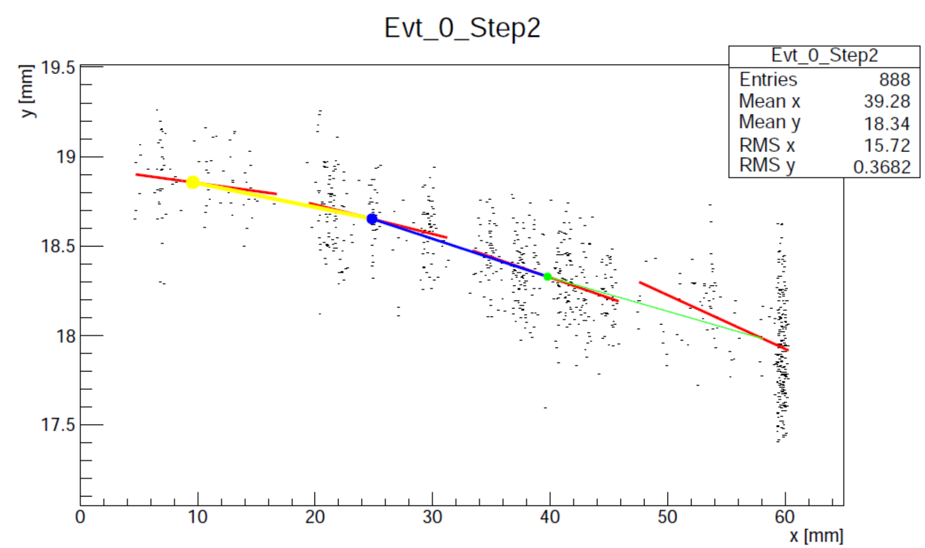
Current track finding is based on a 2D Hough transformation
→ good for single tracks, but not for more!

Need a better algorithm in particular for simulating and reconstructing of full events.

Looking into different algorithms. Currently: Reconstruct on single chips, and join tracklets with modified algorithms of FTD.







Summary

Study of a TPC end plate fully equipped GridPixes is continuing:
- Demonstration with 1 GridPix shows good results
- Demonstrator with 8 GridPixes was successfully operated
  in the DESY testbeam
- Plans for a 100 GridPix modules are being addressed now.
  Main issues like mass production of GridPixes and electronic
  readout of chips looks very promising
- Detailed simulation on modules has started with ANSYS and Garfield++.

Need some more effort in the reconstruction and data analysis.

Presentation of a summary of the activities of the LCTPC Pixel group, where Bonn, IRFU Saclay, Kiev and NIKHEF contribute.

Many pictures were taken from presentation during our last face-to-face meeting 27-28/1/2014