Timepix3 and TSV status

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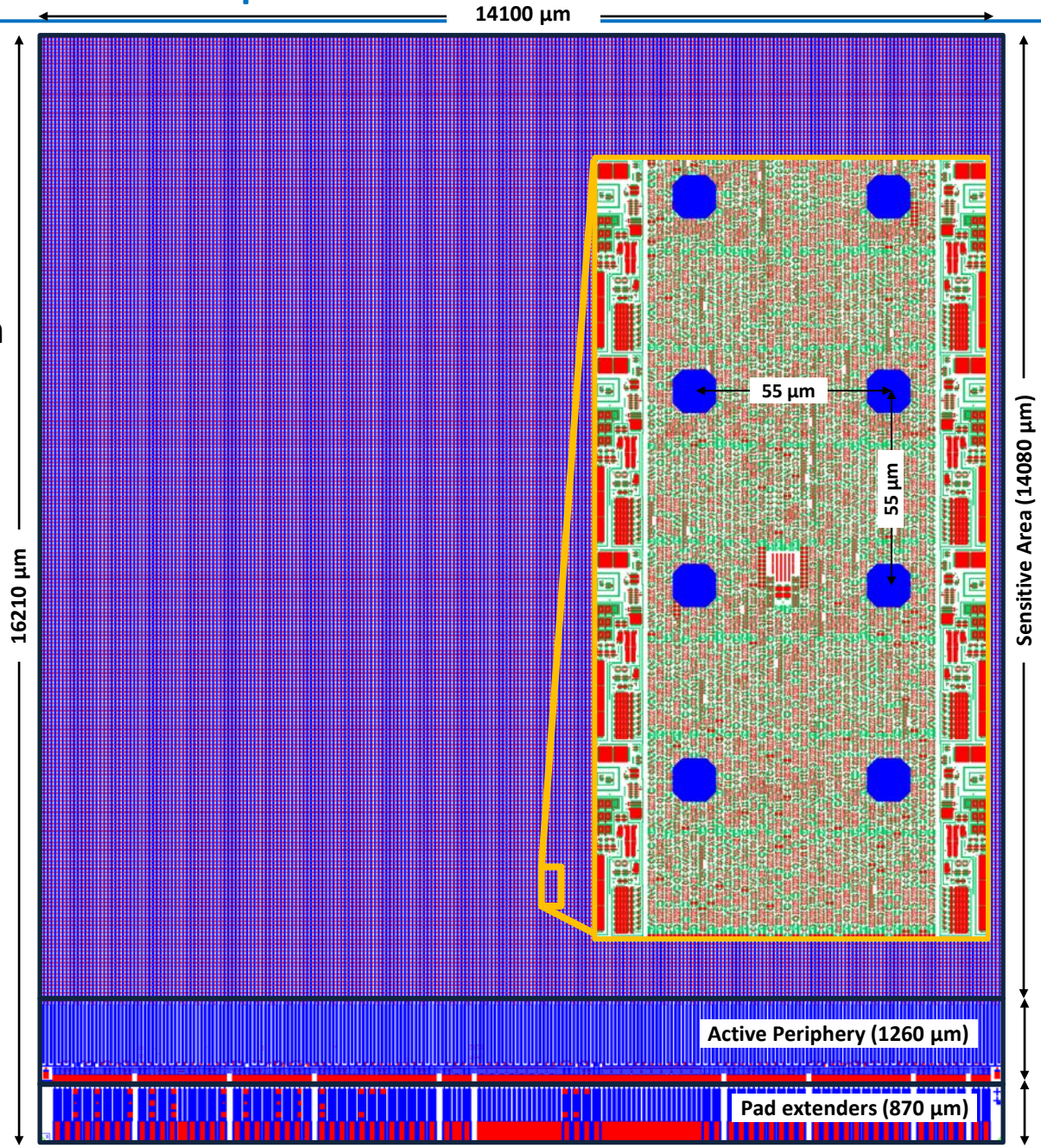
Timepix3

Readout chip for hybrid pixel detectors:
- 256x256 pixel matrix
- 55x55 um pixel size
- Both charge polarities accepted and leakage current compensation
- Simultaneous time (TOA) and charge (TOT) measurement per pixel
- Fast TOA resolution of 1.56ns
- Event counting (PC) and total charge (iTOT) mode available
- Sequential or data-driven readout (minimize dead time)

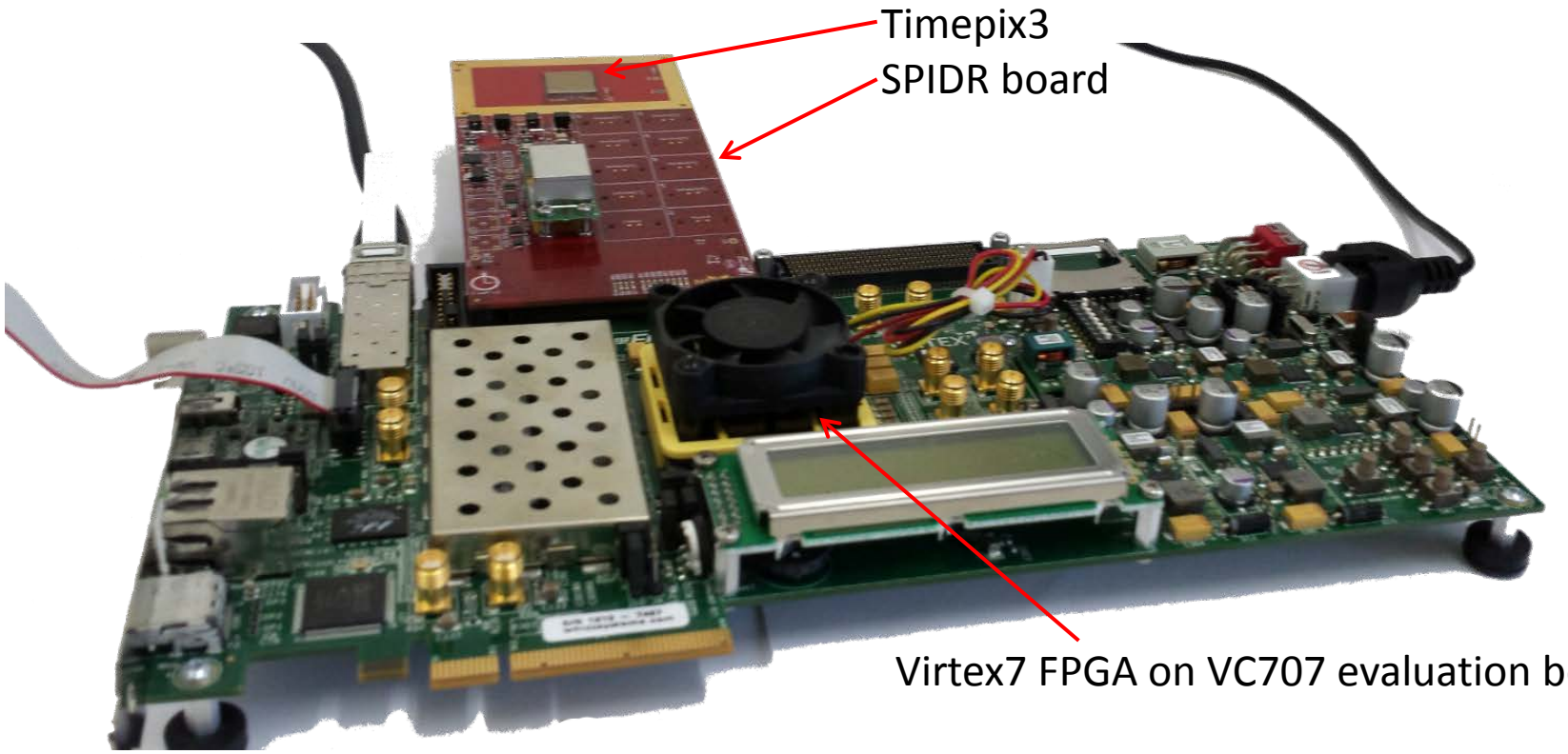
Design effort shared between CERN, NIKHEF, University of Bonn

Design submitted in May 2013, diced chips received in September



Timepix3 readout with SPIDR board (NIKHEF)

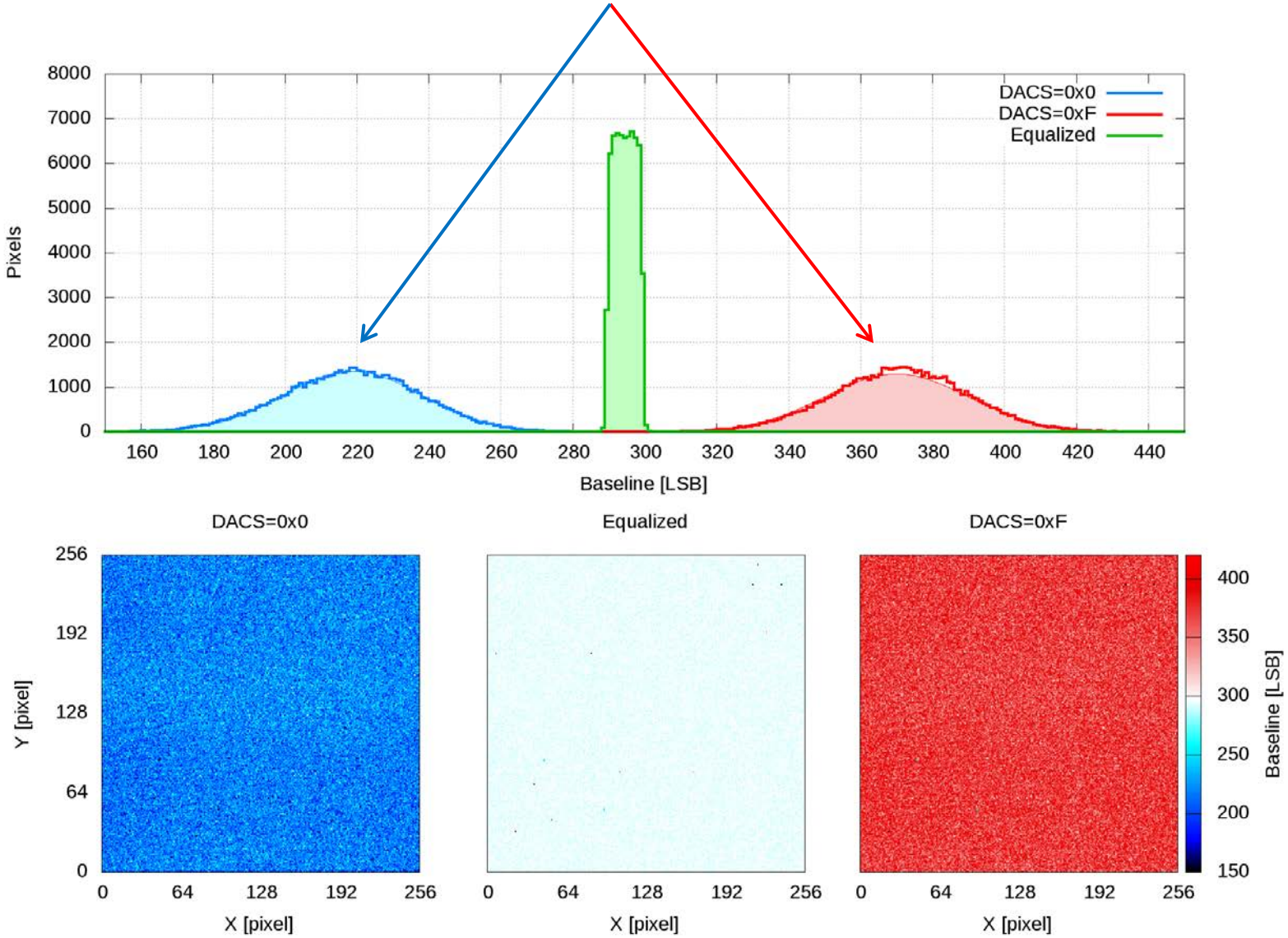
So far 17 Timepix3 tested between CERN and NIKHEF: all functional
Current consumption after reset: 450mA analog, 370mA digital
All 8 digital links working at 640MHz frequency, as expected



Conversion LSB->e^- in the next slides based on a front-end gain of 50mV/ke^-: to be verified once assemblies with sensor are available ➔ preliminary results!
Results shown for I_{krum}=3nA and positive test pulses only

Pixel matrix baseline equalization (noise-based)

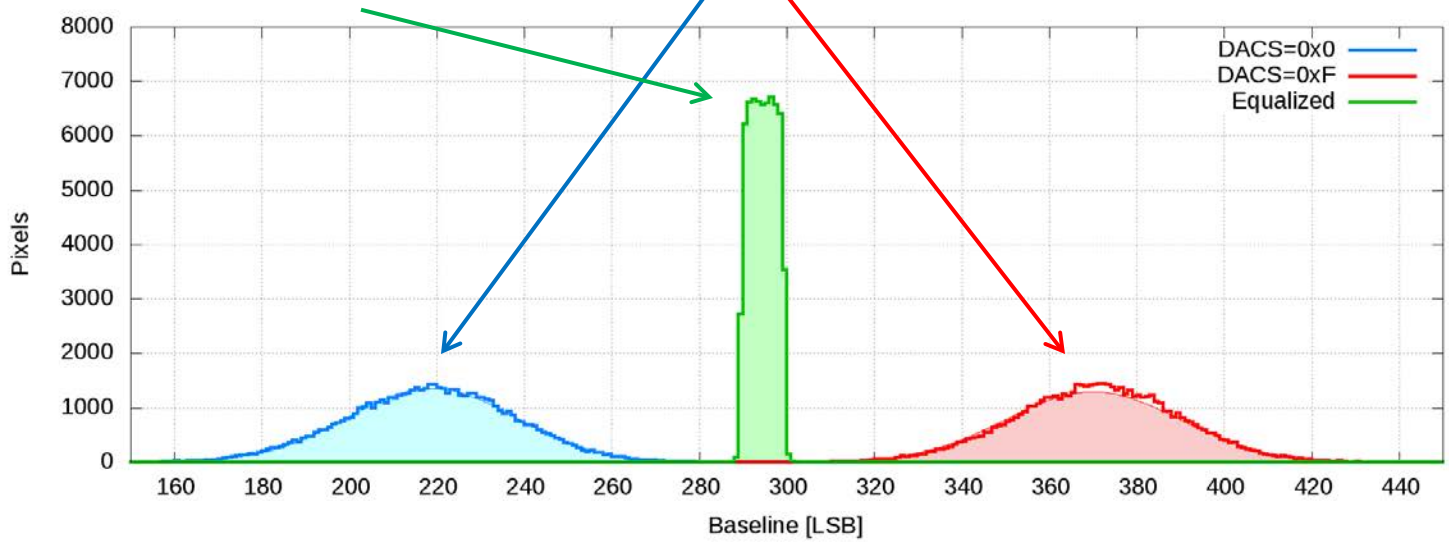
Mismatch before equalization: 19.0LSB=190e$^-$ rms

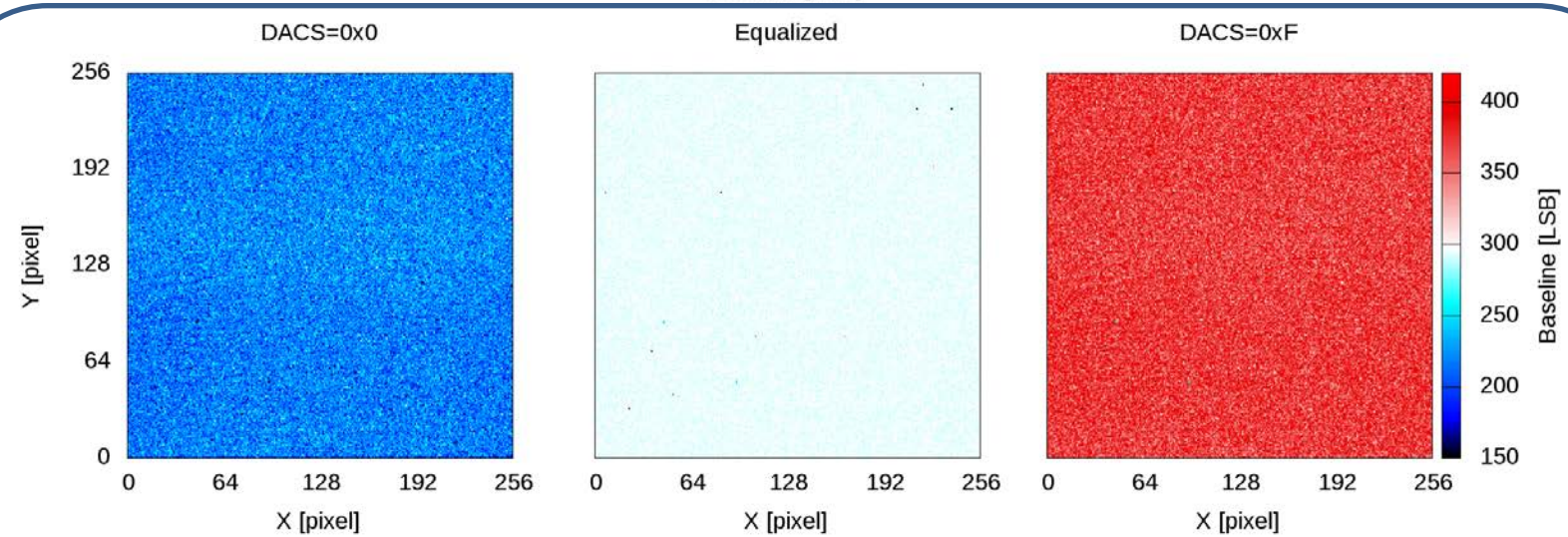


Pixel matrix baseline equalization (noise-based)

Mismatch before equalization: 19.0LSB=190e$^-$ rms

Afterwards: 2.9LSB=29e$^-$ rms



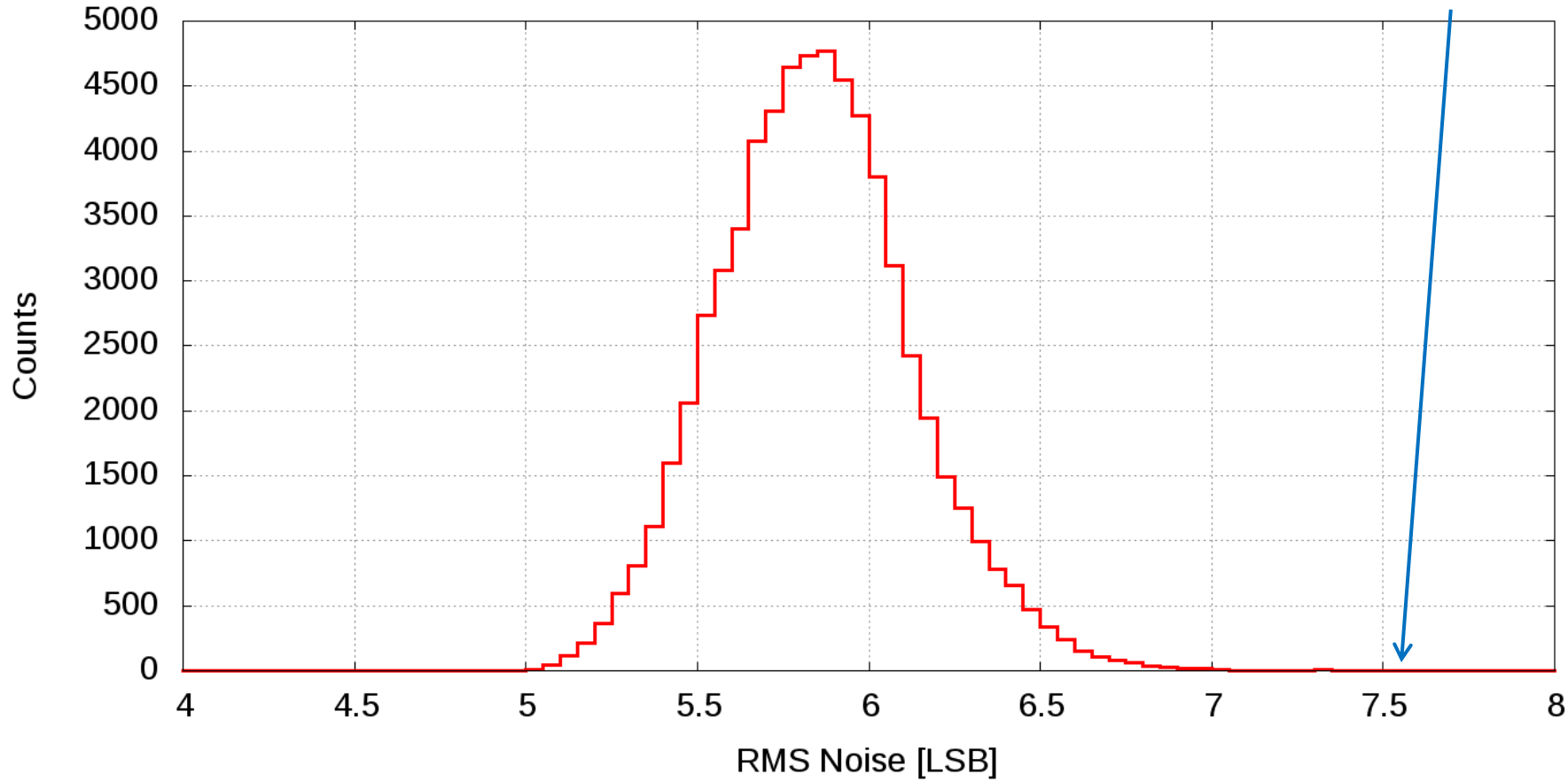


No evident pattern/effect, only a few dead pixels

Noise distribution

Noise: 5.8LSB average, 7.6LSB noisiest pixels
(matching simulation results, no significant digital noise injection)

The noisiest pixel determines the minimum threshold



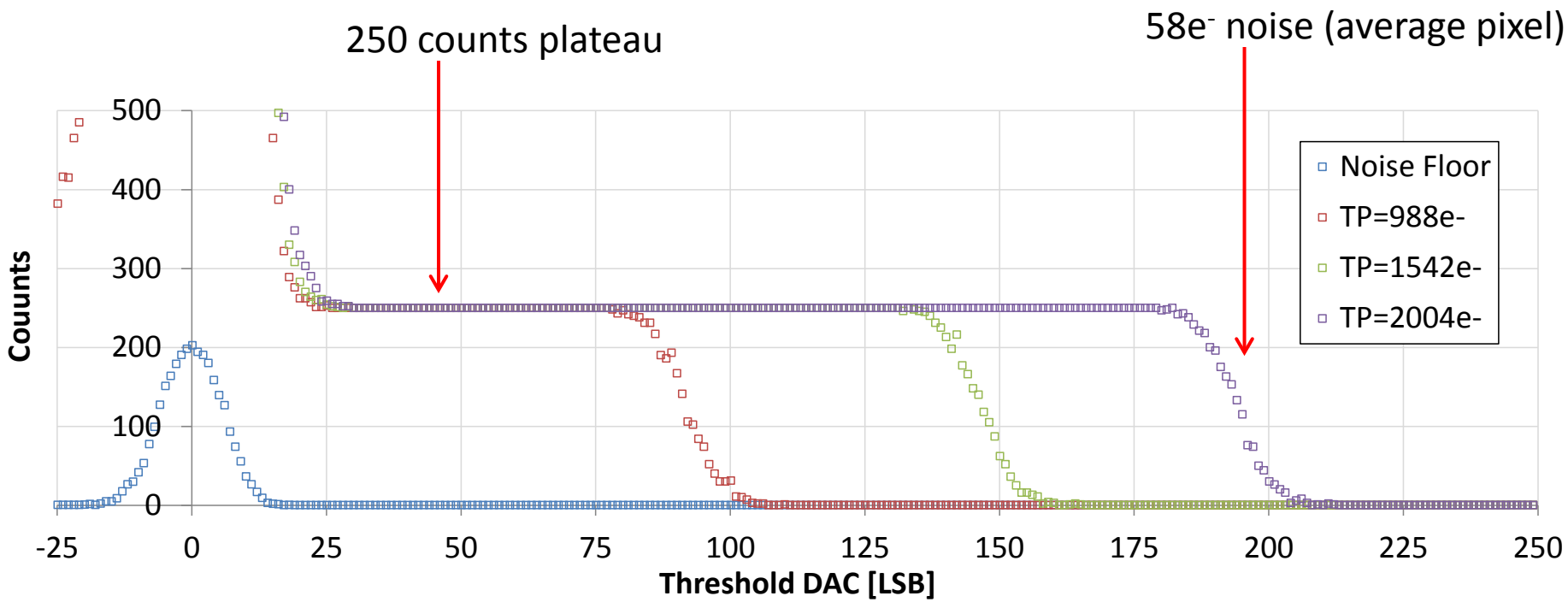
76e$^-$ noise + 29e$^-$ mismatch (after equalization)

➔ 81e$^-$ rms (quadratic sum)

➔ 6σ minimum threshold around 490e$^-$

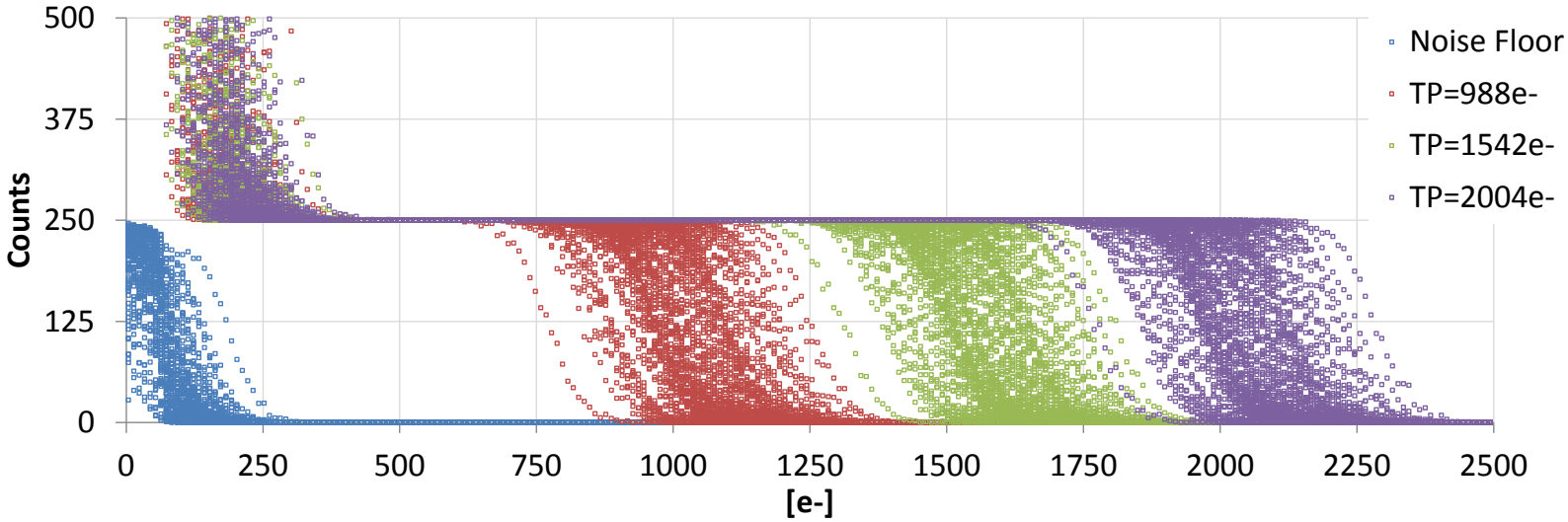
S-curves, using test pulses, 1 pixel

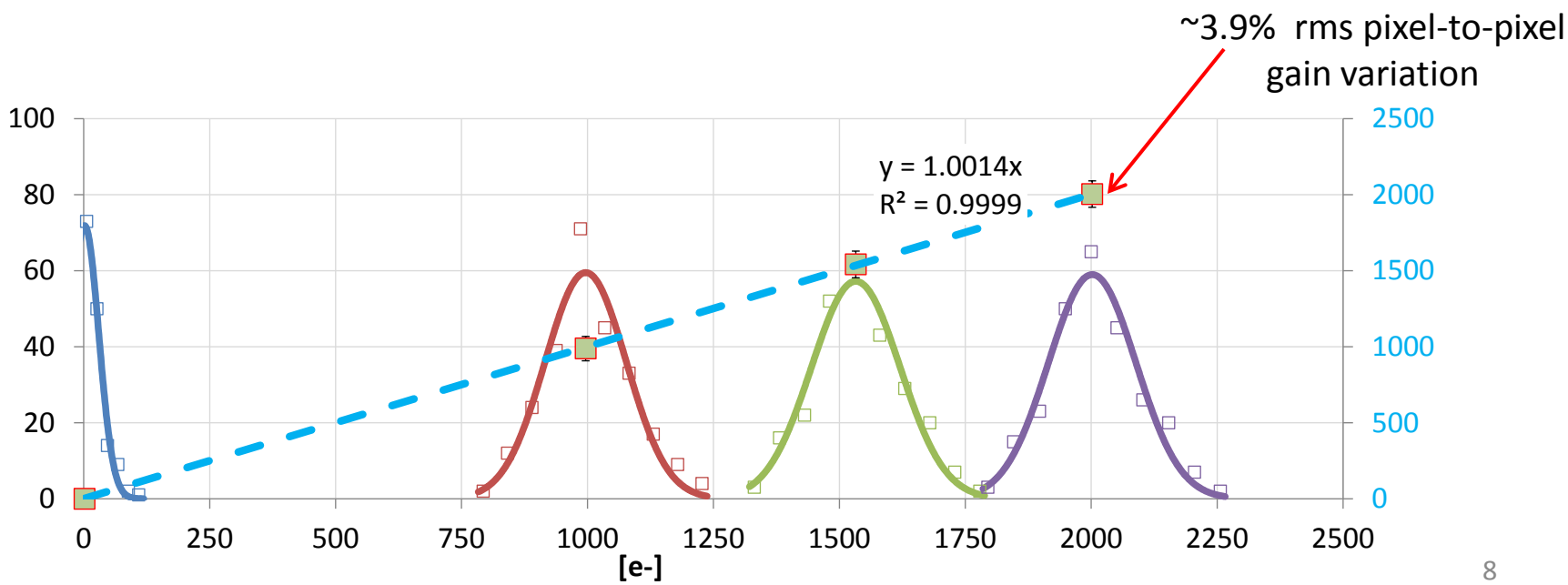
3 trains of positive test pulses (holes) with different amplitudes
250 pulses/train



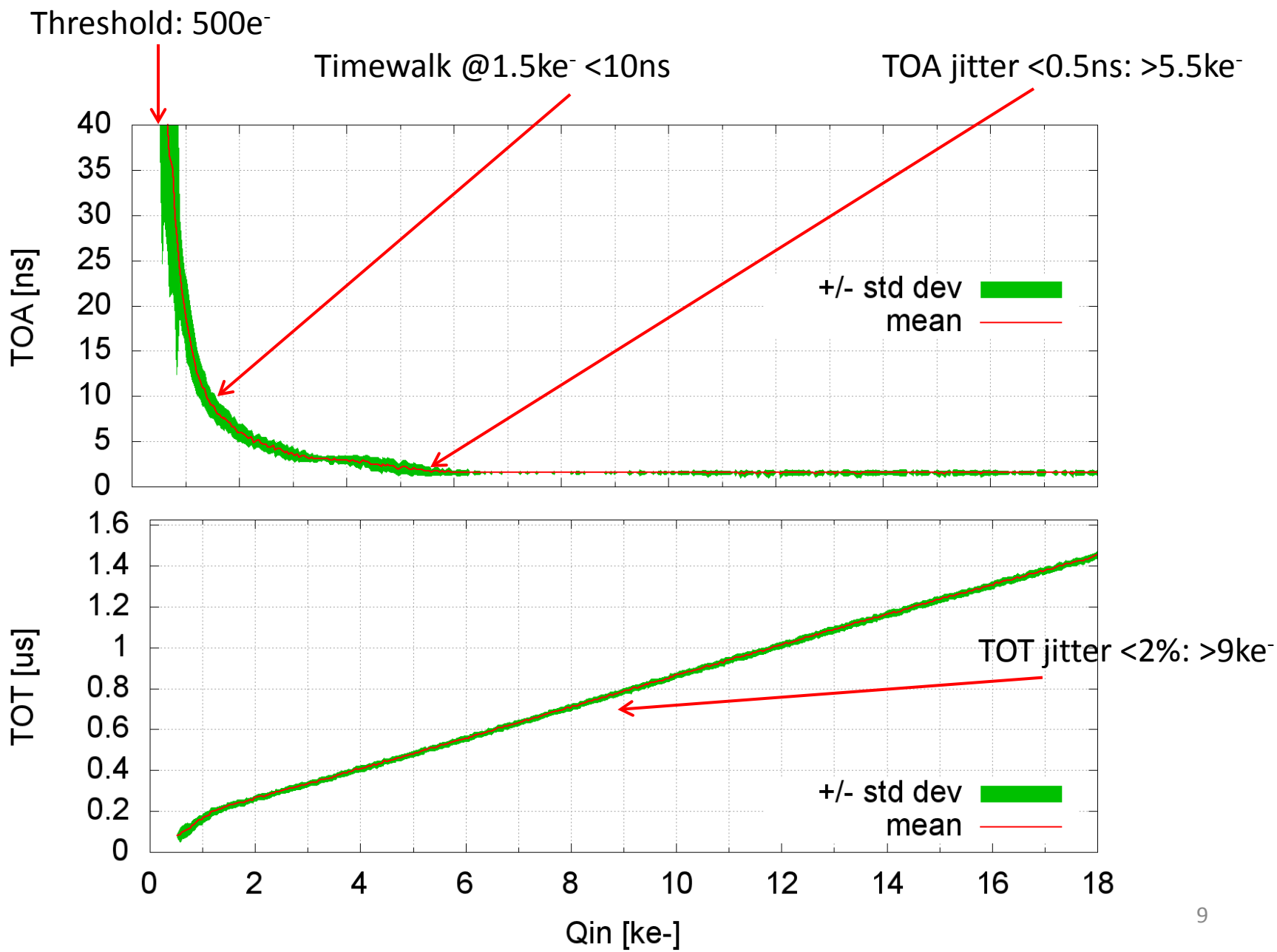
Front-end gain $10e^-$/LSB (or $20e^-$/mV)

S-curves, 256 pixels

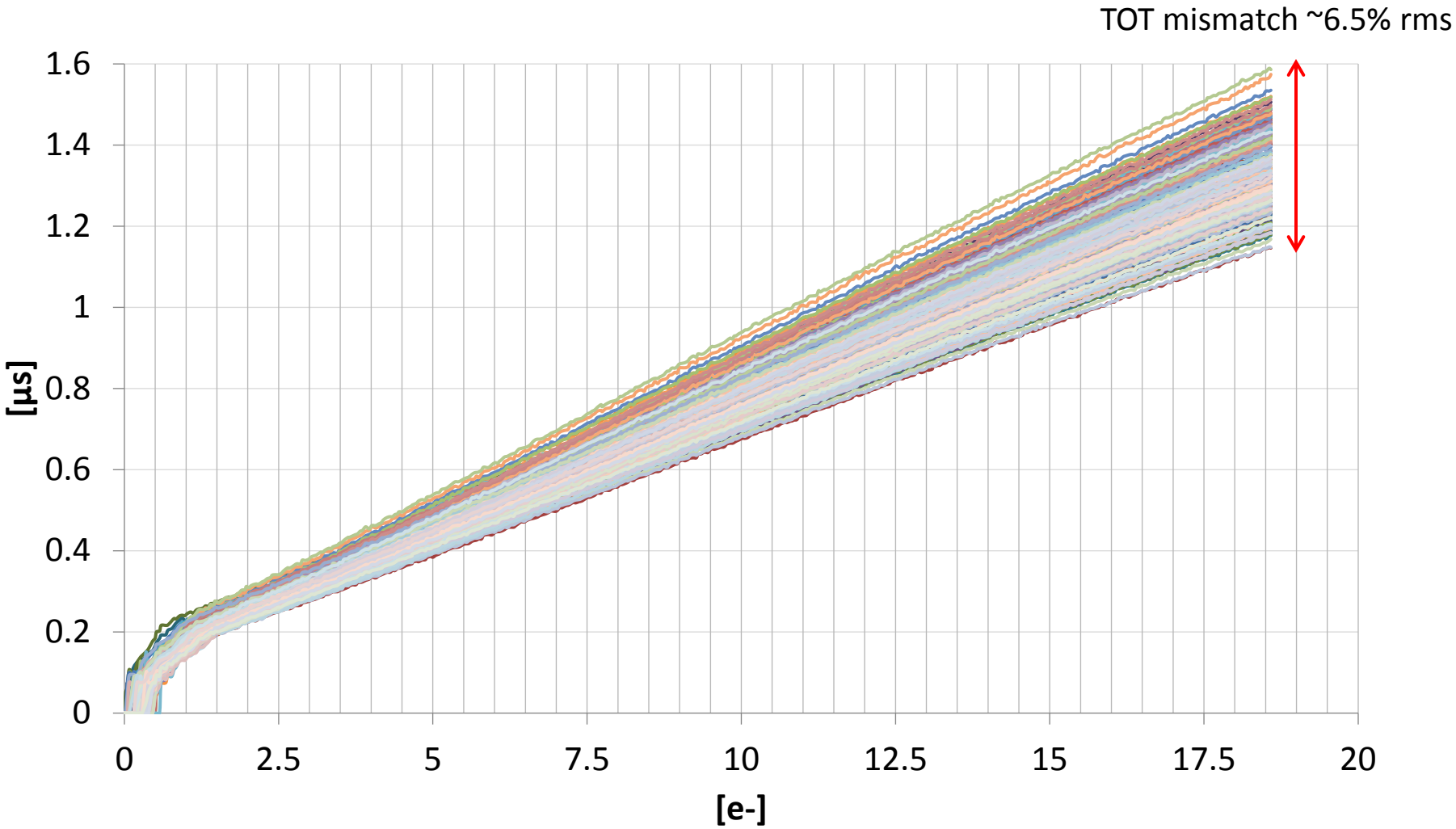




Time-Over-Threshold & Time Of Arrival

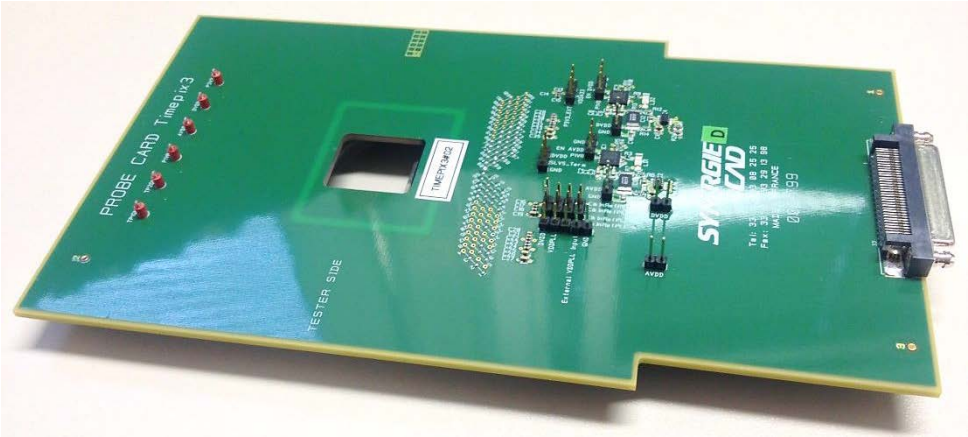


TOT pixel-to-pixel mismatch



Timepix3 CERN PCBs

Timepix3 CERN chip board

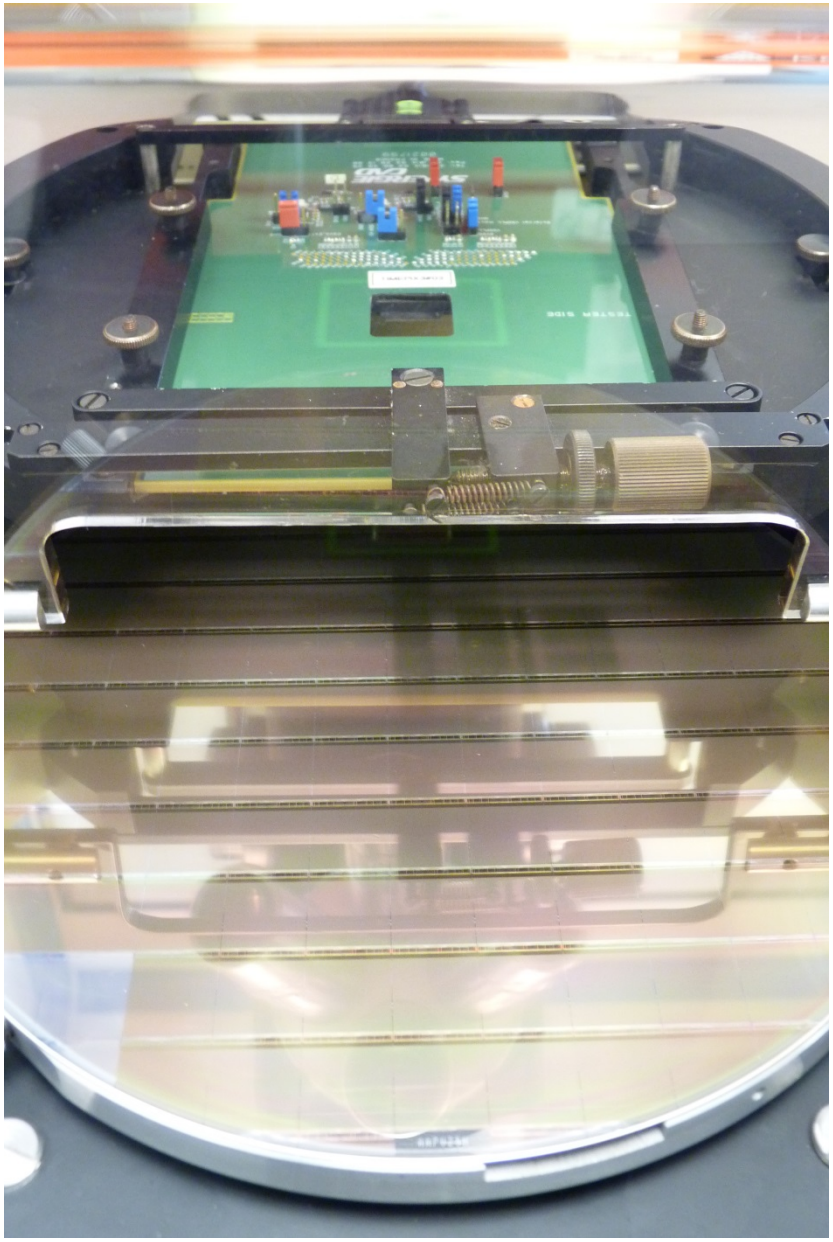


Timepix3 Probe card

Timepix3 translator FMC/VHDCI

Wafer testing

Some small readout bugs to be fixed (missing data packets)
Finalizing wafer probing readout program
11 wafers available (1155 chips)
First wafers to be measured this week

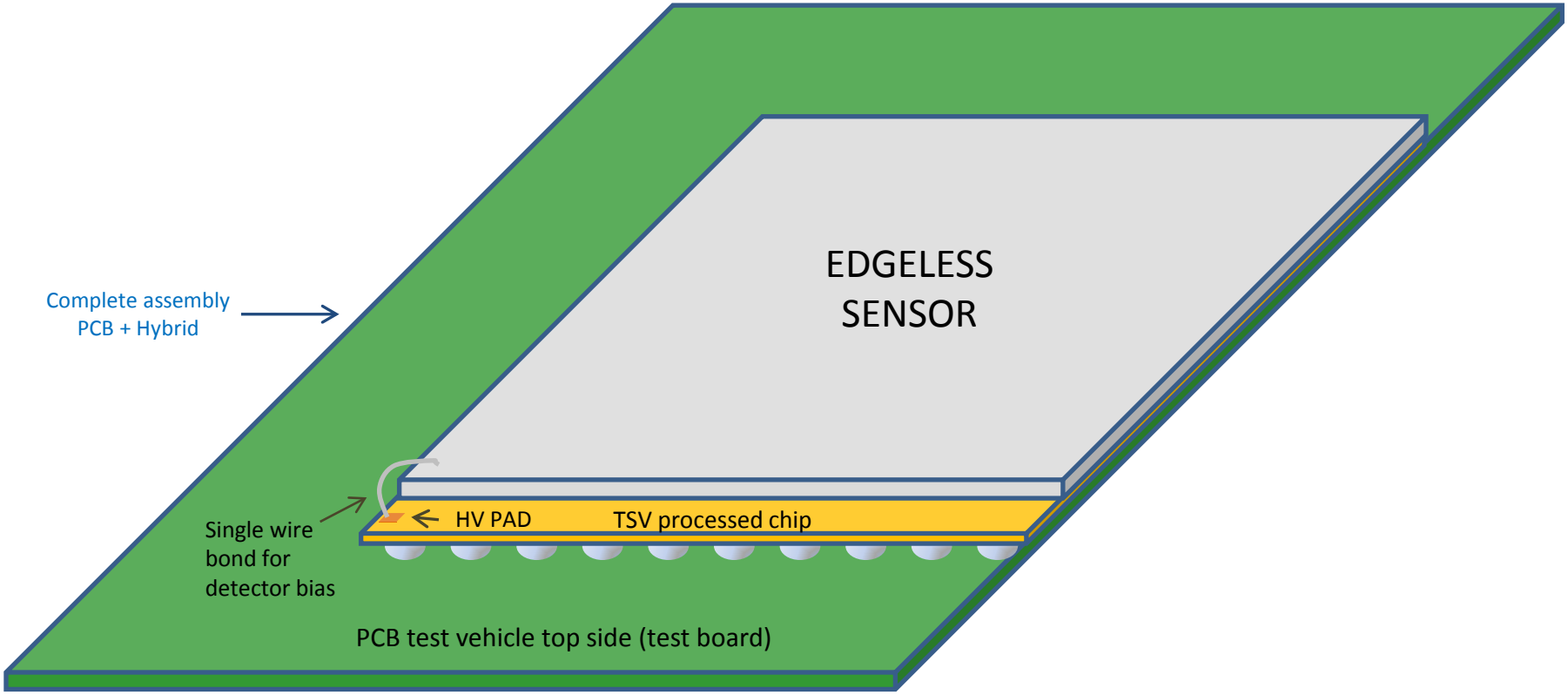


Through-Silicon Vias project

Credit: J Alozy

Goals:

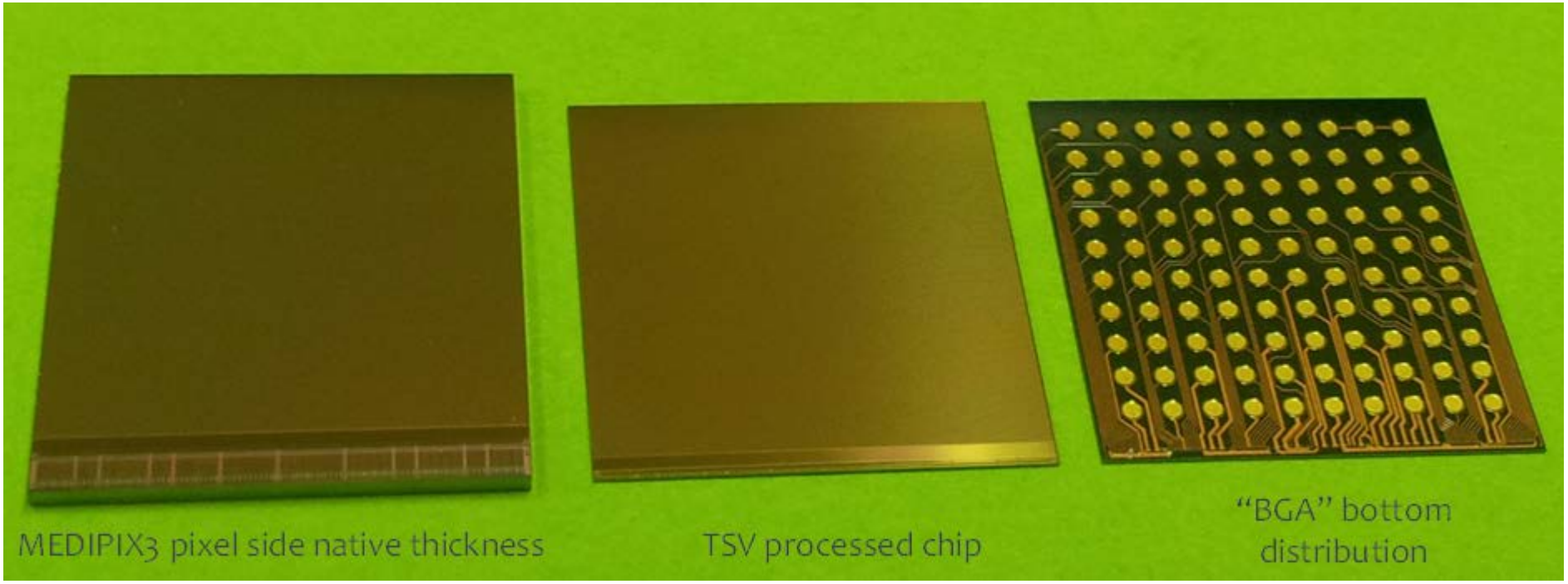
- Produce hybrid pixel detector assemblies which can be tiled on all 4 sides, without losing performance
- Reducing dead area (no wire bonding pad area on chip nor on PCB)
- Thin readout chips for low mass



TSV process

Some Medipix3 chips sent for TSV processing:

1) Thinning to 120um
2) Etching TSVs of diameter 60um
3) Re-Distribution Layer (RDL) applied to the backside of the chip (BGA 100 pins footprint)



Medipix3 / Medipix3RX

First picture taken with Medipix3 assemblies using only TSVs, chip on board (no test socket):

Difficulties with the cleaning process: so far liquid bath (imperfect, leaving traces), now try with vapour cleaning (renting external equipment for CERN assembly workshop)

Good quality of assemblies.

Sensor bias current: tens of uA when high voltage applied through TSV (measurement confirmed with another assembly)
Applying HV with a needle (HV not passing through TSV): only a few uA => To be studied

2 lots of MP3RX wafers undergoing TSV process with 120um thickness. Delivery schedule:
- 3 wafers at the end of February (now in TSV etching phase)
- 3 at the end of March (new UBM mask soon released)

Very similar process, new temporary bonding method

Timepix3 TSV

During 2014: TSV process on 2 wafers of ultra-thin Timepix3
Goal: prove the concept for 50um thickness => different TSV area (diameter 40-50um), geometrical challenges
Ultimate goal: open the road for a 50um-thick readout chip + 50um-thick sensor (CLICpix)

Timepix3: only few wafers available, under test (will take some more time)
$\Rightarrow$ Start with 3 MP3 wafers (same pixel pitch and stress/warpage behaviour)
50um thickness already done with other chips (FEI4) but not standard yet
Study bending of the chips, design new redistribution layer, avoid ball bonds on the corners

Mechanical stress: warpage (mechanical bend of thin chips) -> control and compensation of deformation with a backside compensation layer (materials and techniques under development)

Summary

Timepix3:

- Chip submitted and first wafers received
- All tests performed so far show that the chip is fully functional
- Measurements are in agreement with expectations (noise, mismatch, time resolution)

Plans for 2014:

- Continue testing single chips to achieve a complete characterization
- Test wafers (next weeks)
- Produce assemblies with sensor, possibly before summer

TSV:

- Very encouraging results obtained with Medipix3 chips thinned to 120um
- More tests on chip-on-board integration, temperature behaviour, cleaning methods
- 6 TSV-processed Medipix3RX wafers soon available with a new process and RDL

Plans for 2014:

- More Medipix3RX wafers for ultra-thin processing (aim 50um), in preparation for Timepix3 TSV project

Thanks for your attention!

References:

- T Poikela *et al* "**Digital column readout architectures for hybrid pixel detector readout chips**" *JINST* 9, January 2014
  doi:10.1088/1748-0221/9/01/C01007
- M De Gaspari *et al* "**Design of the analog front-end for the Timepix3 and Smallpix hybrid pixel detectors in 130 nm CMOS technology"** *JINST* 9, January 2014
  doi:10.1088/1748-0221/9/01/C01037

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