TRT ROD Update

Spares

- 8 Spares are mostly working
  - The issue that keeps them from being usable is that typically 1 of the NSEs is not functioning correctly
  - Rest of the board looks good
- Rework on these is finished, awaiting testing
- Bench tests look fine, but need to test data flow, which requires vme system
- VME PS at UBC failed over the summer, replacement sent from Penn was lost in shipping …
- So, progress stuck until we have a working system again
- Plan on testing 3 at CERN in a few weeks as a stop-gap

Firmware updates

- During summer, much of the 100 kHz/23-bit upgrade was completed and tested
- Input deserializer can now handle 23 bit data with the minimum 1 clock between subsequent events

- Validity Mask implemented – user selectable word that is ANDed with the data to implement the mask
- If result is zero, word is set to zero
  - Apply 0xFFFFFFF to not mask any data, so basically this is always “active”
  - Apply desired mask to effect a validity gate, or even more complex pattern
  - At current 80 MHz clock for that section, this works in 1 clock tick
  - Might need to adjust slightly to be a 2 tick process at 100 MHz

Firmware updates

- 100 kHz operation needs test stand access to debug
  - First pass at code runs, but fails after a few dozen events
  - Need working VME crate to look at signals and see what conditions cause the freeze
  - Will work on this at CERN during upcoming trip
  - 100 kHz is awkward
    - DDR memory is running at 2 x 160 MHz
    - SLINK runs at 40 MHz
    - Most things on the board run at a multiple of the base 40 MHz clock – 100 MHz is tricky because it is a non-integer multiple, so the phase relationship between signals is more subtle

Firmware and testing plans

- Hopefully get replacement VME PS to UBC to continue development with students (2) and postdoc there
- In the meantime, will be at CERN in Nov to focus on testing some of the reworked boards and getting a stable 100 kHz design using the test stand in 104
  - Plan to bring a postdoc who is learning VHDL but needs hands-on experience with running and testing the RODs
- Once this is working, do full system tests with Sarah and Ximo to debug at the next level of complexity