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Low Power Robust Design of FinFET-based Circuits using a Technology-Circuit Co-optimization Approach

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Transistor scaling has been the main driving force for the success of the semiconductor industry for the past several decades. However, sustaining the benefits of scaling with conventional bulk MOSFETs has proved to be extremely challenging due to prohibitively large increase in short channel effects and sensitivity to process variations. As a result, alternative technologies with higher scalability are being explored, amongst which FinFETs have emerged as the most promising substitute for the standard transistors. However, FinFETs have their own limitations and design issues like width quantization and higher front end capacitance due to their non-planar structure. Hence, using FinFETs as a drop-in replacement for the bulk MOSFETs is expected to yield sub-optimal designs. In order to harness the full potential of FinFETs, there is a need to explore technology-aware circuit design techniques, which utilize the unique features of FinFETs to achieve superior design solutions. In this talk, I will present several such techniques with a focus on low power robust design of memories and digital logic. I will start my talk by introducing the device structure and characteristics of FinFETs and the circuit implications of making a transition from bulk MOSFETs to FinFETs. I will, then, present technology-circuit co-design techniques based on symmetric and asymmetric spacer optimization, asymmetric source/drain doping, fin orientation and independent gate control of FinFETs. I will highlight the importance of considering device-circuit interactions to achieve higher energy efficiency and stability of FinFET-based memories and logic. I will also briefly discuss the implications of some of the techniques on analog circuit design. Finally, I will present the simulation framework that we have developed for FinFET-based circuits in sub-10nm technologies and discuss its key features.

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