Readout chips for SiPM and fast timing applications: Spiroc, Citiroc, Petiroc, Triroc

ARGONNE, FEE 14

Nathalie Seguin-Moreau on behalf of OMEGA microelectronics group and Weeroc

IN2P3-CNRS, Ecole Polytechnique, Palaiseau (France)

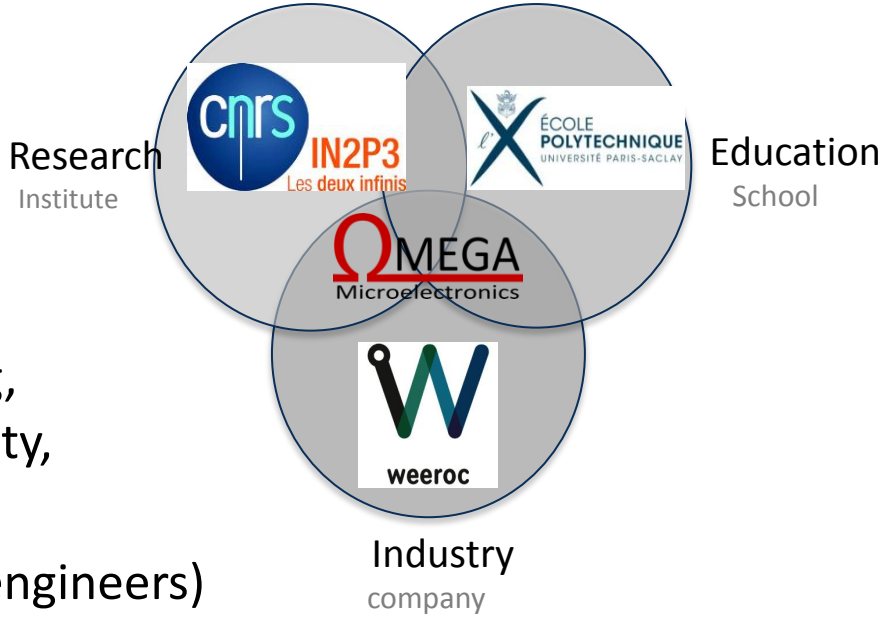
http://omega.in2p3.fr/

http://www.weeroc.com/

Organization for Micro-Electronics desiGn and Applications

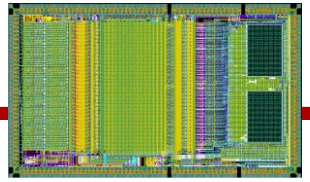
OMEGA and Weeroc

- **OMEGA:** was a microelectronics group of LAL ORSAY, became an independent lab (IN2P3/CNRS/Ecole Polytechnique) in June 2013. Located in Palaiseau, directed by Christophe de La Taille
- OMEGA addresses academic microelectronics requests for IN2P3/CNRS labs and also for external research labs



- **Weeroc** is a spin-off company from Omega
- CEO: Julien Fleury
- Weeroc addresses industrial needs for microelectronics in Spatial, medical imaging, scientific instrumentation, Homeland security, nuclear industry …
- Weeroc and OMEGA (13 microelectronics engineers) provide :
  - on-the-shelf FE ASIC (the ROC chip family)
  - customer-specific ASICs
  - Services, Audit, Expertise
- **Designs in SiGe 0.35µm AMS tech.**

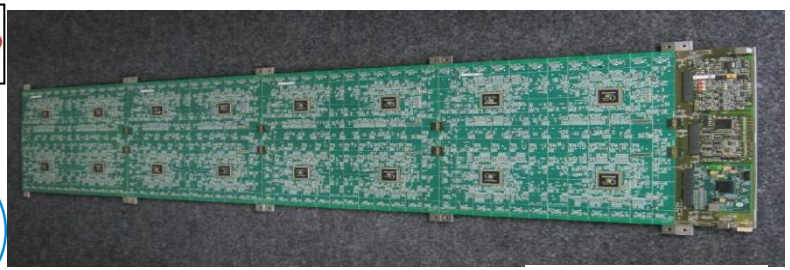
SPIROC



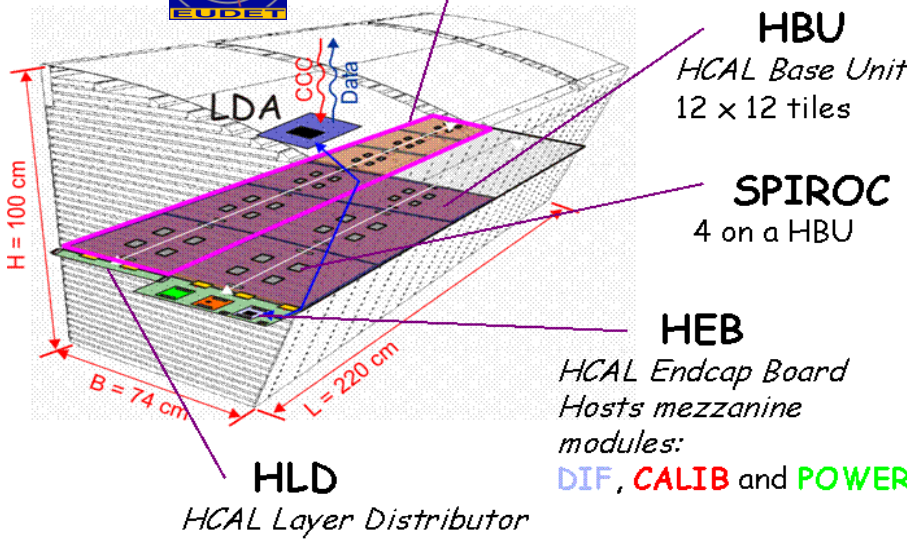
Omega

- Silicon Photomultiplier Integrated Readout Chip to read out the analog hadronic calorimeter for CALICE (ILC) , first version designed in 2006 in 0.35m SiGe AMS
- Large detector with 8 millions channels =>Chip embedded in detector + LOW POWER
- **36-Channel ASIC**
- **Auto-trigger on MIP or on single photo-electron**
  - Auto-Trigger on 1/3 pe (50fC)
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits, 1 pe to 2000 pe**
  - pe/noise ratio : ~11
- **Time measurement :**
  - 12-bit Bunch Crossing ID (coarse time)
  - 12-bit step~1 ns TDC->TAC (fine time)
- Analog memory for time and charge measurement : depth = 16
- 4kbytes internal memory and daisy chain readout
- **Low consumption : ~25 µW/ch @0.5%duty cycle in power pulsing mode**

4 HBU: 576 channels



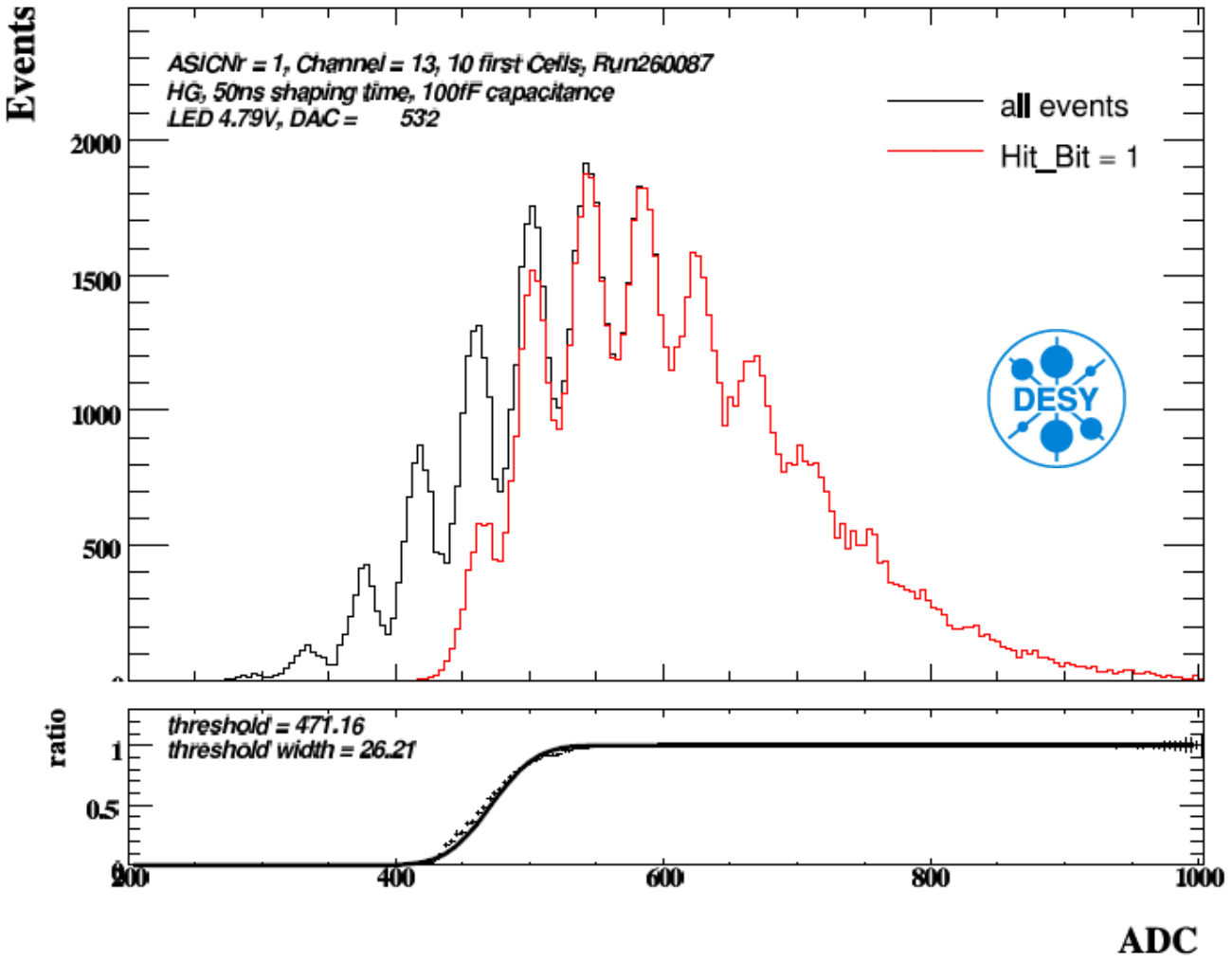
(0.36m)² Tiles + SiPM + SPIROC (144ch)



SPIROC2 PERFORMANCE

Omega

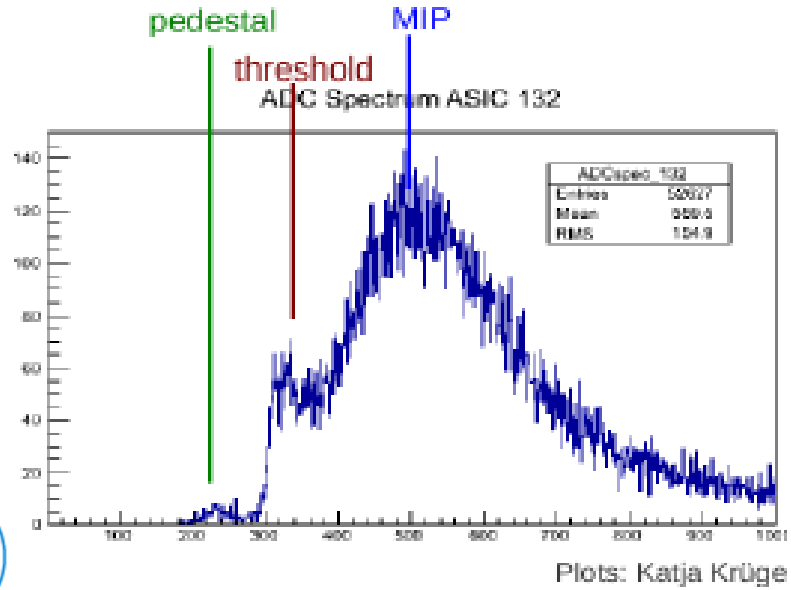
SiPM SPECTRUM with Autotrigger



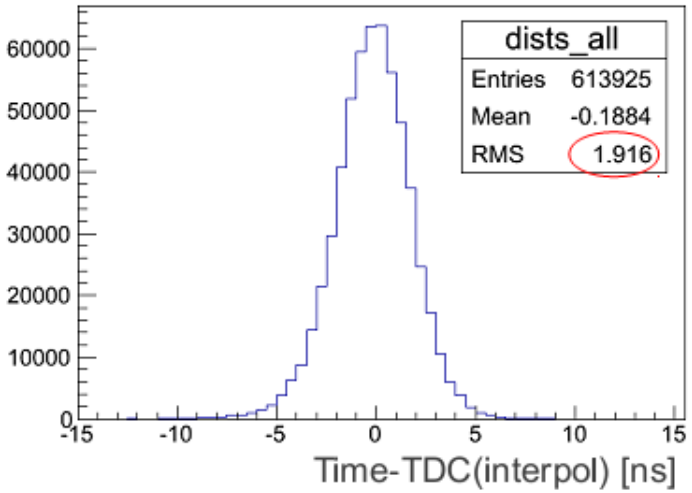
SPIROC2: TESTBEAM

- 576 channel AHCAL layer prototype and multi layer prototype **successfully tested at CERN and at DESY** in 2012 and 2013

- First tests of TDC ramps in SPIROC2b show promising results
  - ✓ Several corrections needed: memory cell and channel wis offsets correction, chip wise ramp corrections
  - ✓ Electronics resolution ~ 2 ns, allows neutron identification



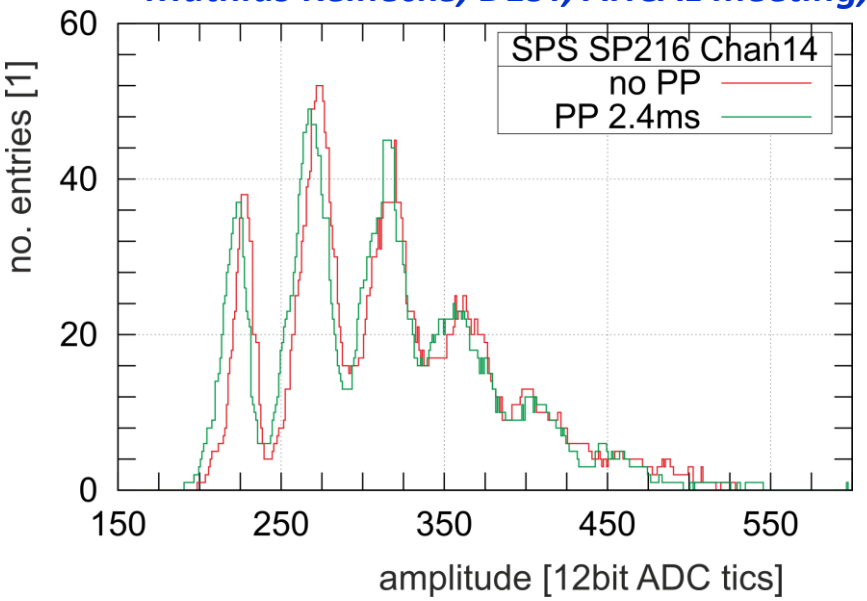
@DESY, HBU

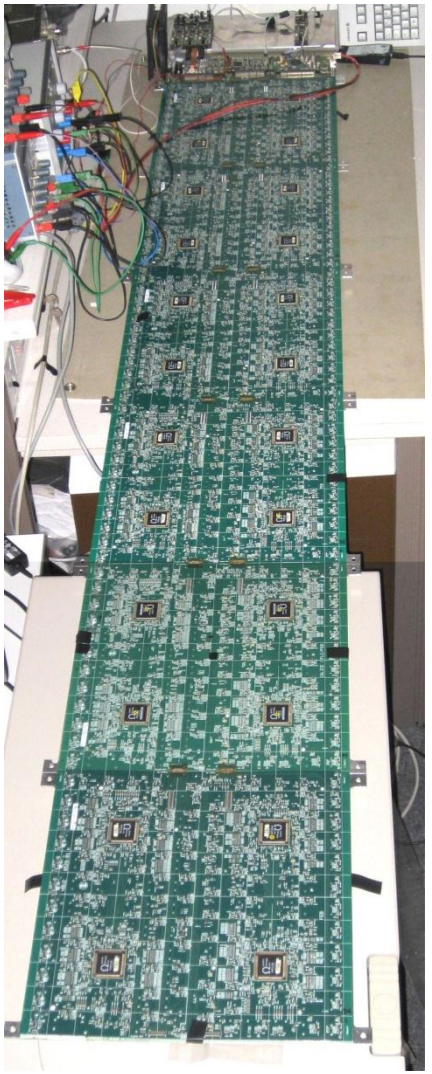


SPIROC2 POWER PULSING TEST

- ILC requirement: 25µW/channel @0.5 %duty cycle => 5mW/ch or 1.5mA/ch @100% duty cycle
- Slab with 24 SPIROC2 chips (864 channels)
- With 6mF: ~2ms switch-on time needed (~2% on-time). Excellent agreement w/wo power pulsing (only small pedestal shift).

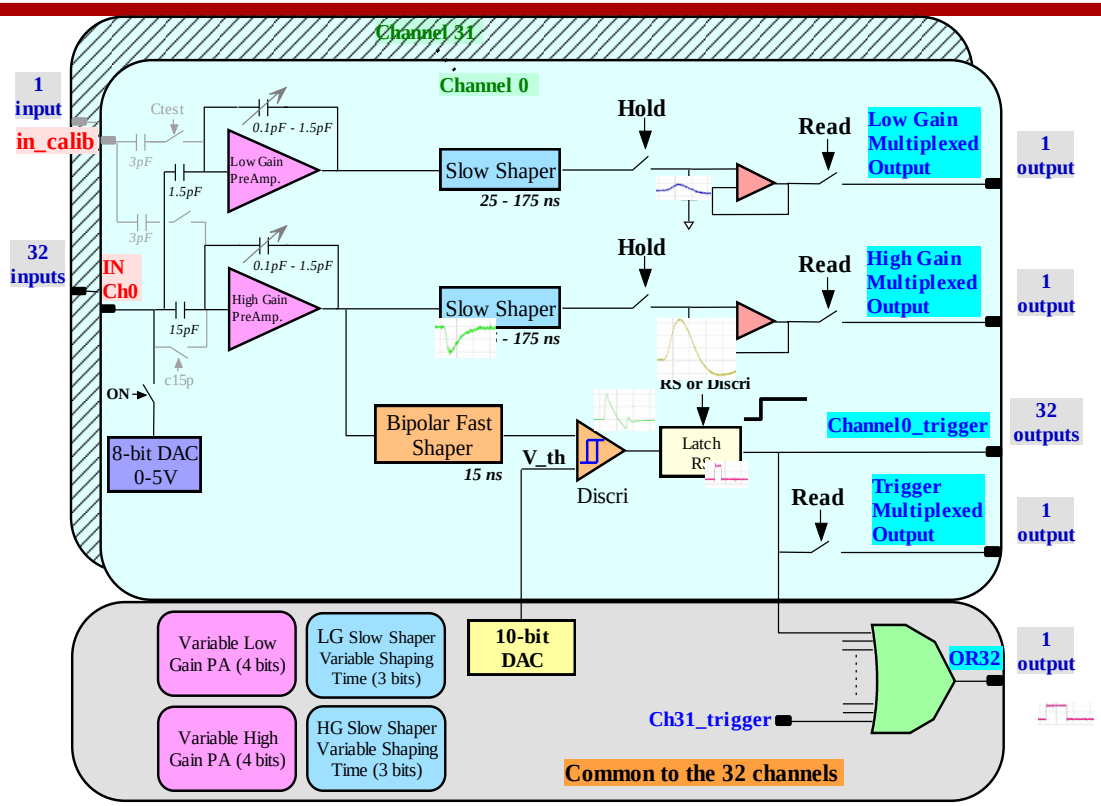
Mathias Reinecke, DESY, AHCAL meeting, 2013, December 13th





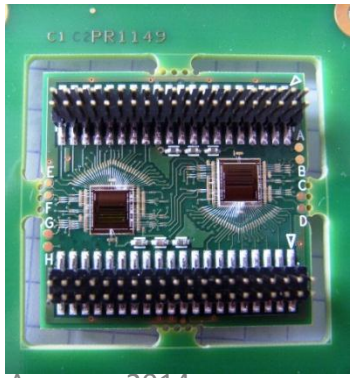
- Power Pulsing works for the full extension setup!
- Trade-off between switch-on time and blocking capacitors needed.

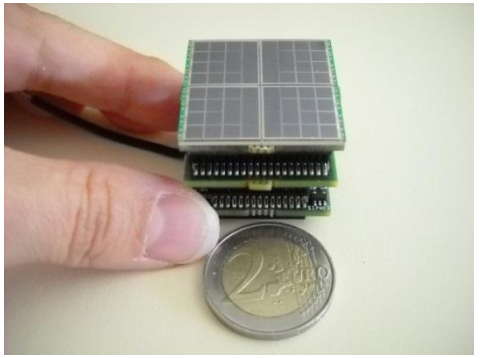
EASIROC



- 32-channel front-end readout (analogue part of SPIROC)
  - 2 multiplexed analog outputs (high gain, low gain) [tri state outputs]
- Trigger output
  - 32 Trigger outputs
  - OR32 output
  - Trigger multiplexed output (latch included) [Tri state output]
- Low power : 4.84 mW/channel, 155 mW/chip

SipMed, IMNC, LAL, OMEGA





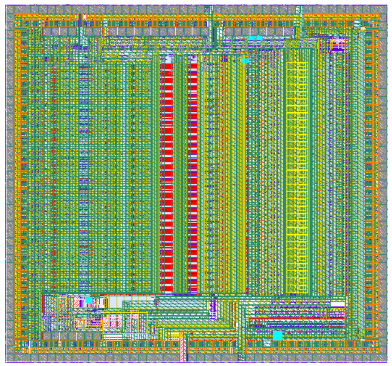
Many applications:

- Astrophysics (CTA Palermo),
- Nuclear physics (KEK, Tohoku),
- PET (Roma, Pisa, Valencia),
- Vulcanology (Napoli, IPN Lyon)

JPARC

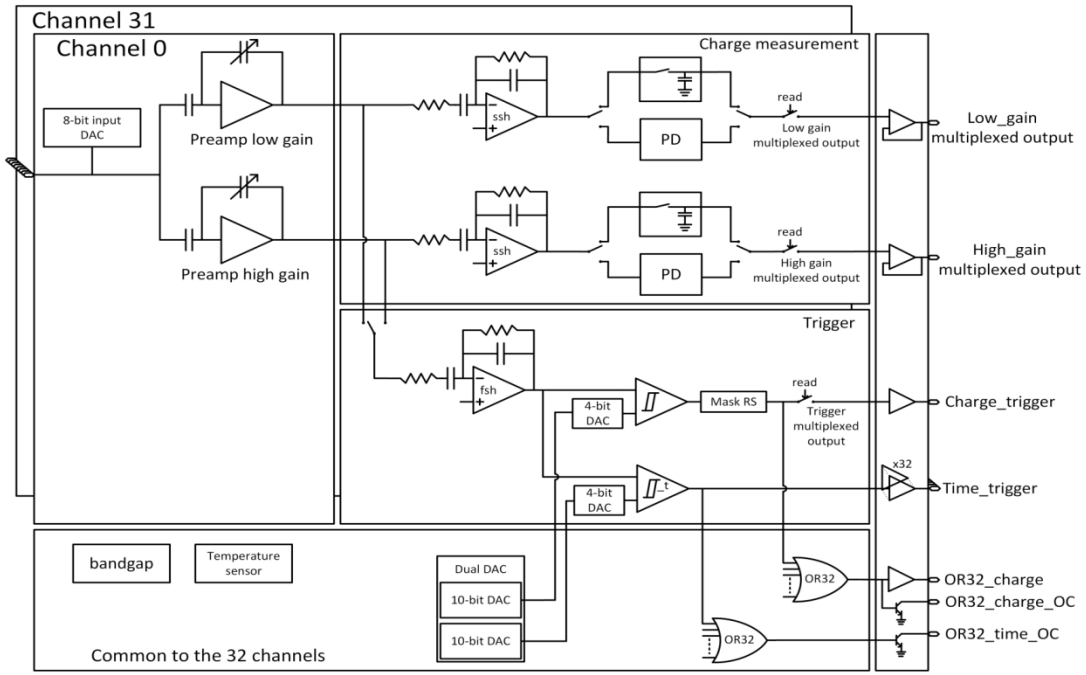
CITIROC

- **Similar to Easiroc (same pinout)**
- **General ASIC:**
  - ✓ Analogue front end ASIC to readout SIPM (positive signal). No ADC, no TDC
  - ✓ 32 channels, charge and trigger ouputs
  - ✓ Power pulsed, each stage can be forced ON/OFF (versatility)

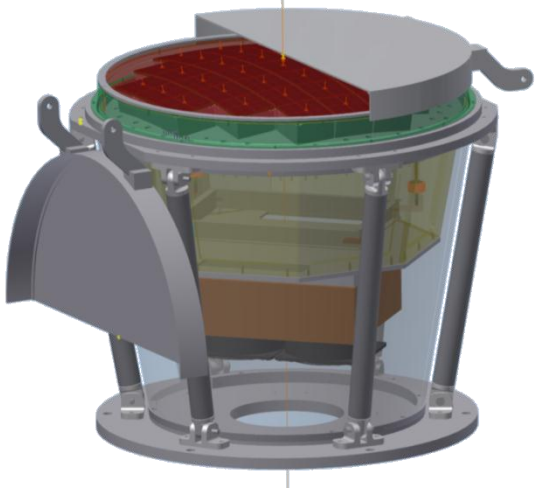


weeroc

- **Front End**
  - ✓ **Trigger path**
    - Fast shaper connected to either low or high gain preamp
    - Two discriminators: one for the timing, one for event validation on energy
  - ✓ **Energy measurement**
    - 2 voltage preamplifiers (1:10 ratio) followed by shaper
    - Analogue memory: track and hold or peak detector
    - Analogue multiplexer

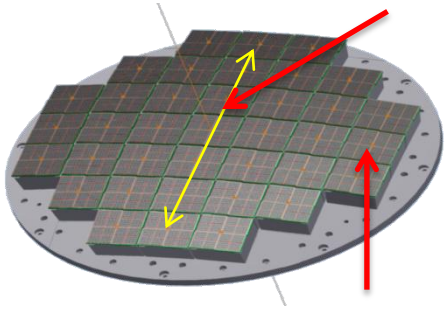


PDM Electronics



FOV = 9.6°

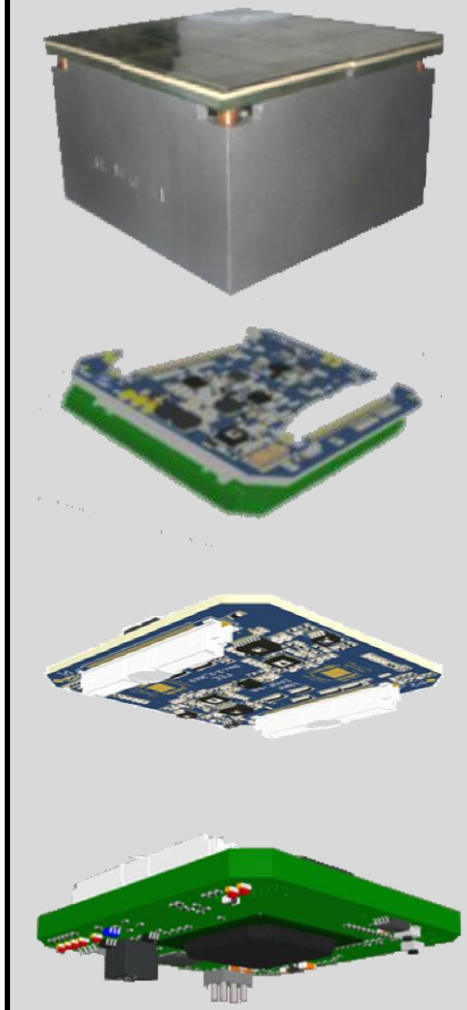
Ø = 350mm

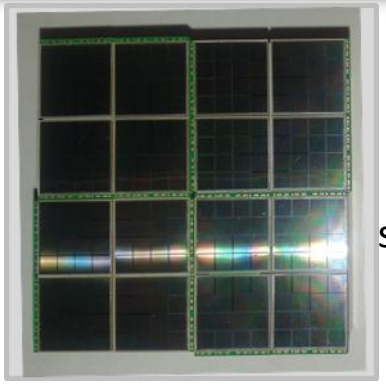


Photon Detection Module (PDM)

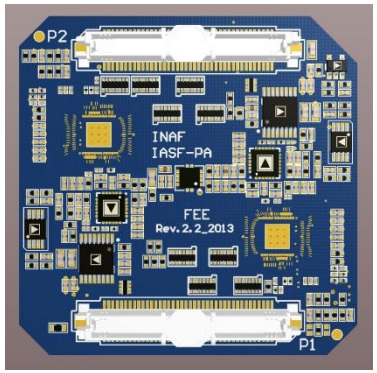
Pixel = 0.17° → 6.2 x 6.2 mm

ASSEMBLING





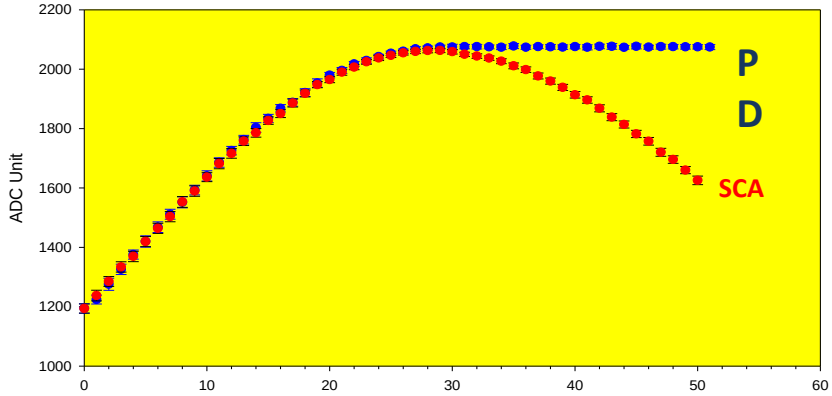
SiPM board
(9 +1 temperature sensors embedded



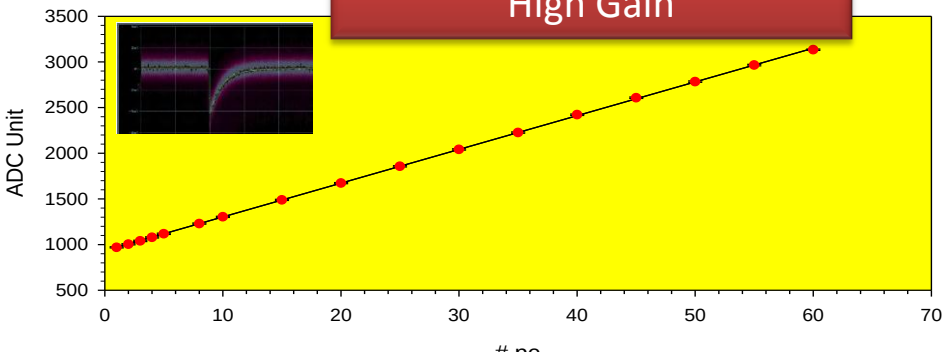
Front-End board
(2 CITIROC ASIC)

PDM FPGA Board
(XILINX ARTIX 7)

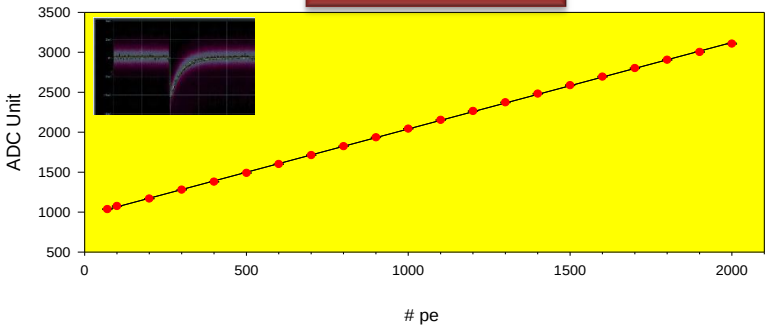
CITIROC: Peak detector

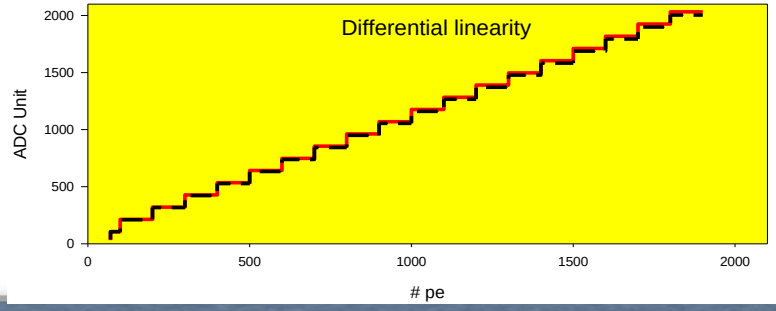


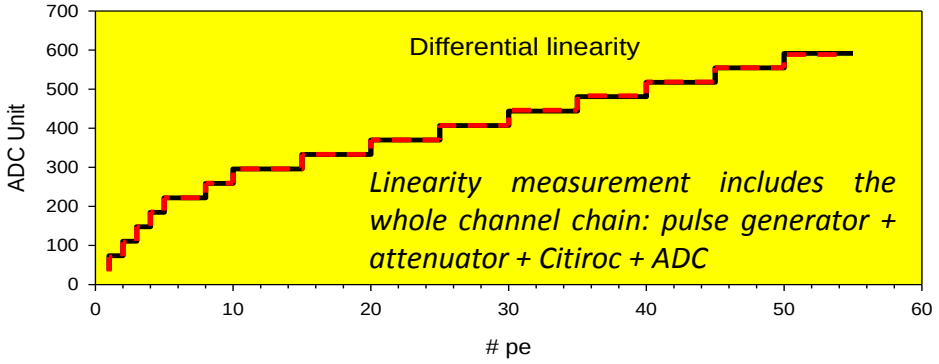
Peak Det. Linearity
High Gain



Low Gain

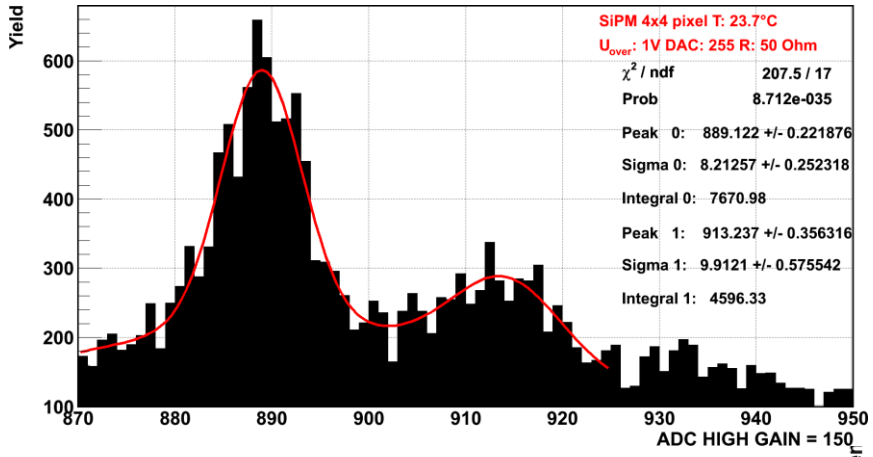


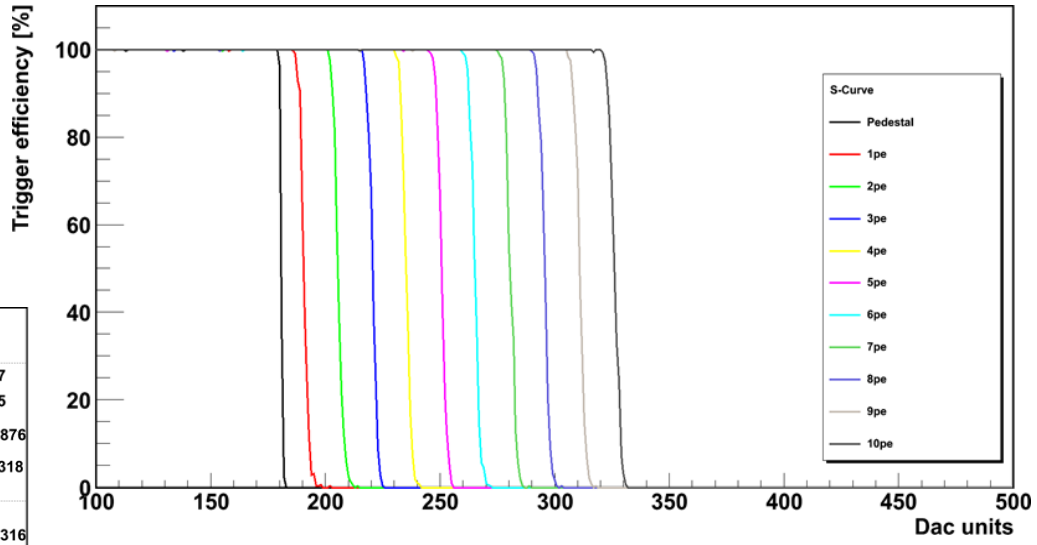


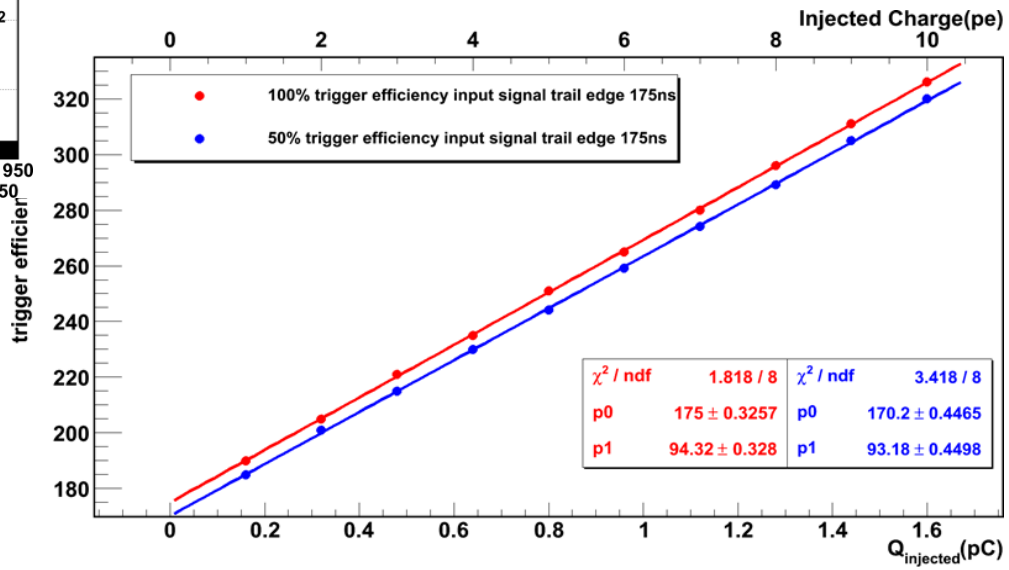


CITIROC: Trigger Linearity

Gain premplifier =4*25fF ≈ 150 nom.
Shaping Time = 50ns
Steps of 1,2,3,4,5,6,7,8,9,10 pe







SiPM 4 pixel High Gain =150
Shaping Time = 50ns
delay time = 38 x 2.5 ns
Temp = 23.7 °C U_{over} = 1V
Resistance = 50 Ohm
Threshold = 922 DAC ~50% of 1 plateau

SiGe GHz Front End

- R&D of 10GHz GBWP preamps for applications where fast timing or high timing resolution is needed (Time Of Flight PET MRI, preclinical, particle physics…)
- 3 architectures in 0.35µm SiGe technology integrated and tested

1 pe-=160fC

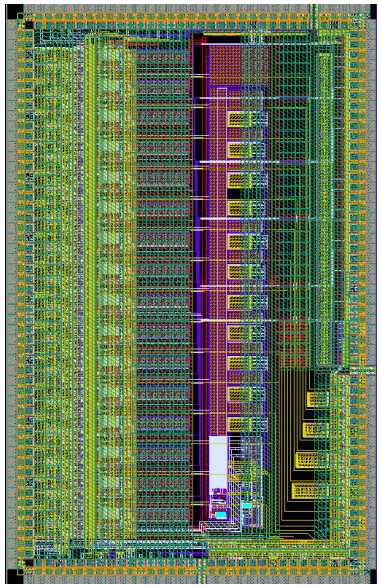
Testboard #3	**RF (Common Emitter)**	**Common Base**	**Super Common Base**
With 100pf/50 Ohm injector (SiPM emulation)		Vb_cb : 400 #DAC	Vb_scb : 1023 #DAC
Noise floor (pedestal)	185-187 #DAC / 1.196V	216-224 #DAC / 1.259V	340-342 #DAC / 1.514V
Signal value @ 10pe	235 #DAC / 1.300V	137 #DAC / 1.085V	115 #DAC / 1.038V
Signal amplitude @ 10pe (signal minus pedestal)	50 #DAC / 110mV	83 #DAC / 174mV	226 #DAC / 476mV
Gain (mV/pe)	**10.4mV/pe (5 #DAC/pe)**	**17.4mV (8.3 #DAC)**	**47.6mV/pe (22.6 #DAC/pe)**
Jitter - threshold 1 pe @10pe	**13ps RMS**	**6ps RMS**	**8ps RMS**
Jitter - threshold 3 pe @10pe	**8ps RMS**	**6ps RMS**	**8ps RMS**
With 100nF DC block (for voltage gain & BW meas.)	**18mV injection**	**18mV injection**	**7mV injection**
Signal Value	267 #DAC / 1.371V	41 #DAC / 0.884V	192 #DAC / 1.2V
Signal amplitude (signal minus pedestal)	81 #DAC / 175mV	179 #DAC / 375mV	150 #DAC / 320mV
Voltage gain (before 50 ohm bridge => factor of 0 .5)	**4.86 V/V**	**10.4 V/V**	**22.5 V/V**
Bandwidth, after discriminator (Δt 10% T50% meas.)	**Δt : 150ps / 660MHz**	**Δt : 360ps / 280MHz**	**Δt : 400ps / 250MHz**

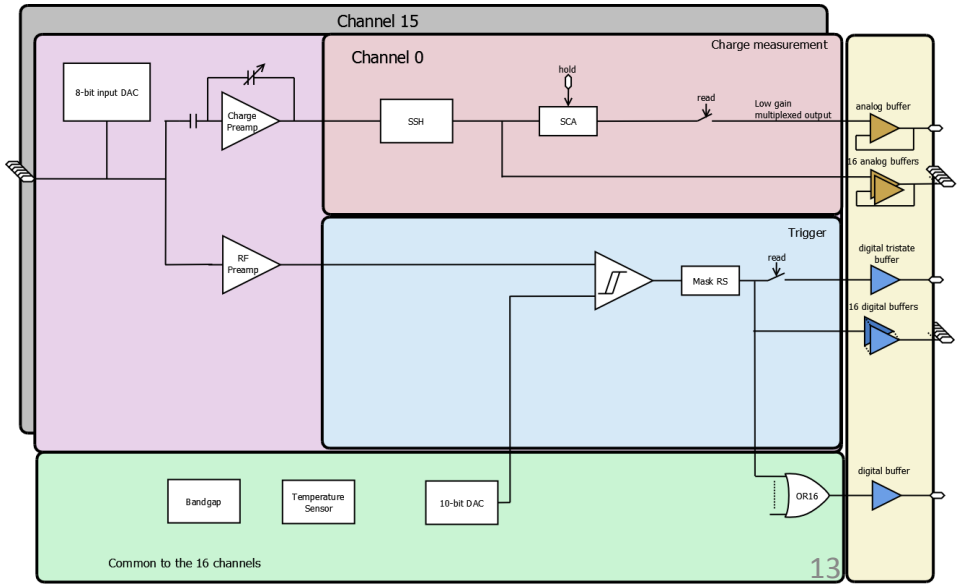
=> Design of PETIROC1: 16 channels with RF amplifier

PETIROC1

- Analog readout chip
  - 16 channels prototyping ASIC
  - 16 input DAC for SiPM HV tuning, 16 discriminator outputs, 16 charge outputs, MUX charge output

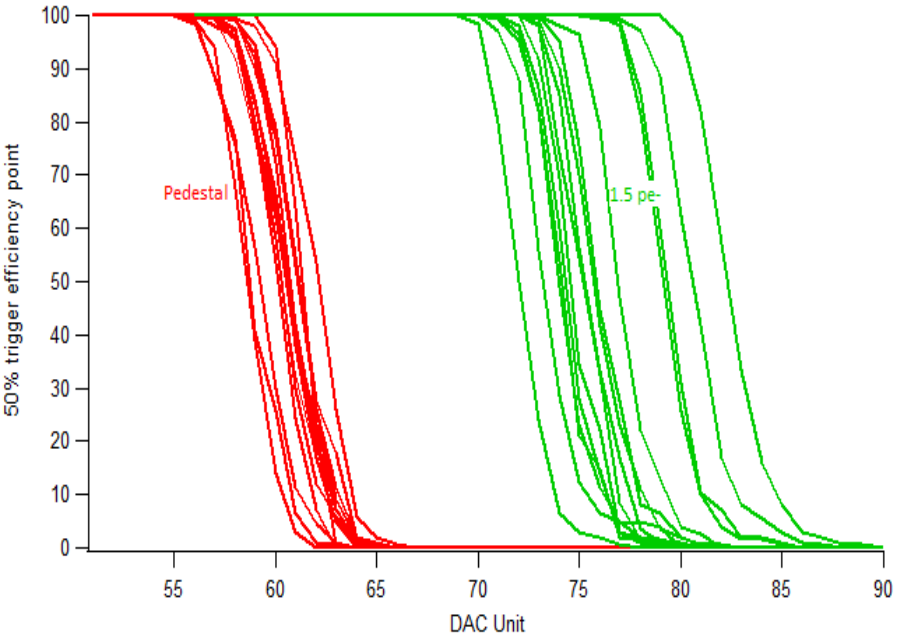
- Fast timing front-end
  - **10GHz GBWP common emitter SiGe** , DC coupled to detector
  - **Fast SiGe discriminator**
  - **Low power: 3.5 mW/ch**
  - Low noise amp+shaper for charge measurement
    - Adjustable peaking time (25ns, 50ns, 75ns, 100ns)
    - Low gain for high swing : 360uV/pe

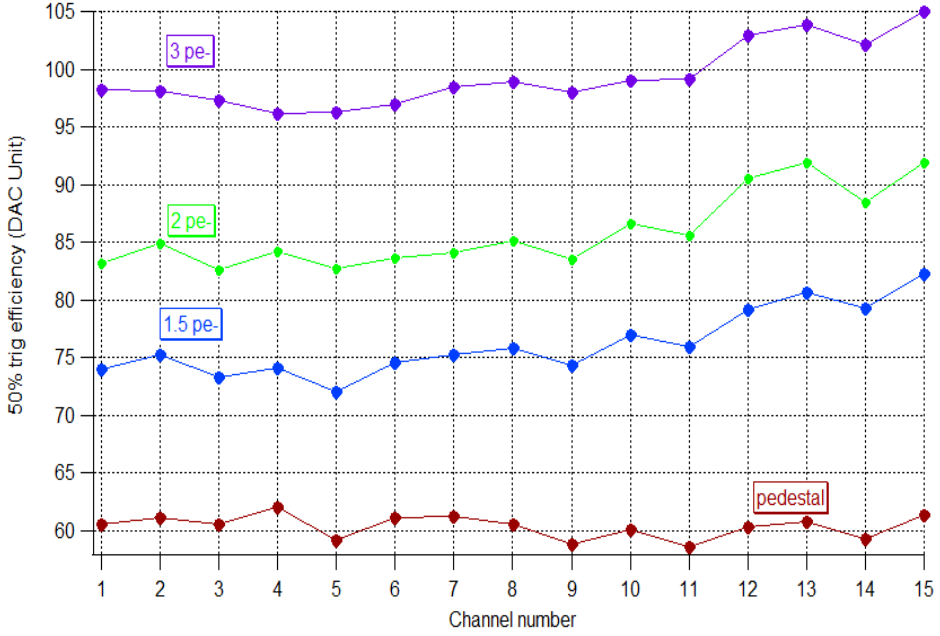




PETIROC1: S curves

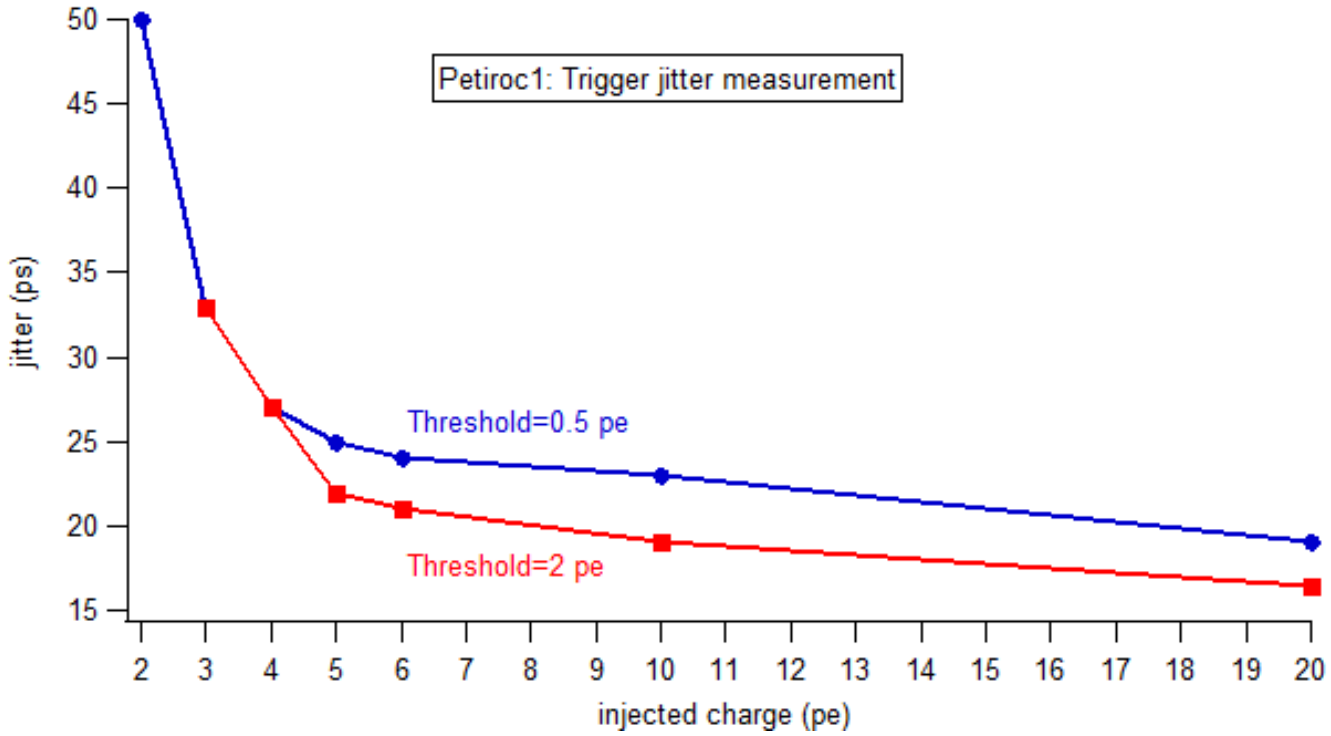
- S curve : trigger efficiency versus threshold
  - For every channel of Petiroc
  - Measured for pedestal and 1.5pe injection
- 50% trigger efficiency
  - For every channel of Petiroc
  - Pedestal, 1.5pe, 2pe and 3pe





PETIROC1: Time measurement

- Jitter vs threshold & injection
- Jitter improve with signal
- Very close to testbench time resolution
- Jitter below 20ps → lower than SiPM time resolution



0.5pe trigger threshold

Injection (pe)	Jitter (ps)
2	50
3	33
4	27
5	25
6	24
10	23
20	19

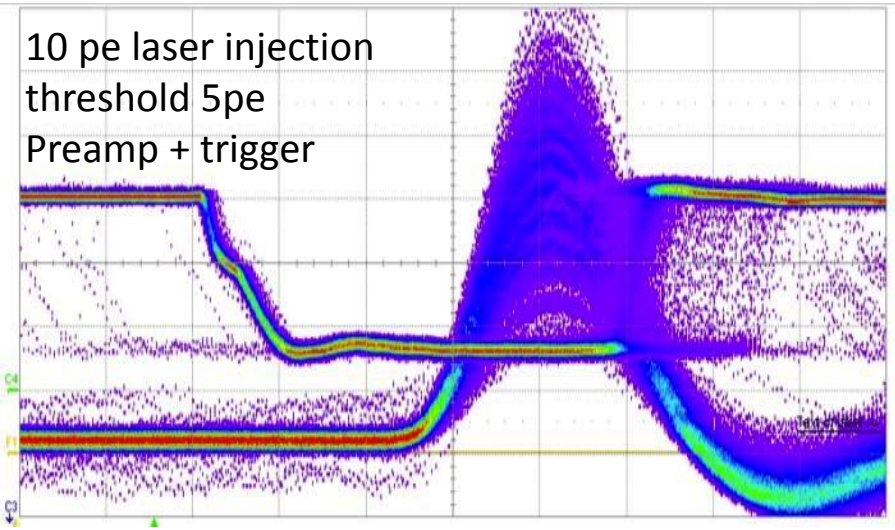
2pe trigger threshold

Injection (pe)	Jitter (ps)
3	33
4	27
5	22
6	21
10	19
20	16.5

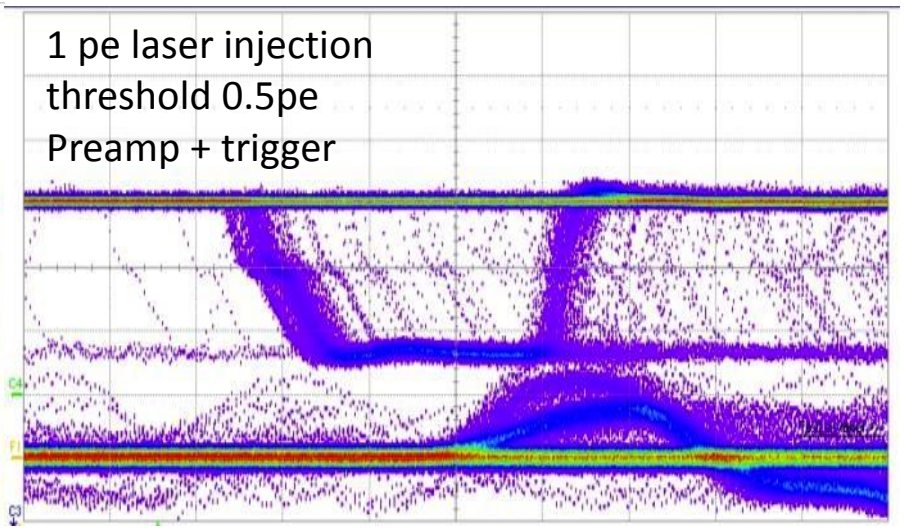
PETIROC1: Triggers on first pe

- 1x1mm SiPM Hamamatsu
- Laser for low light injection
  - 405nm
  - Jitter : 28 ps FWMH
- Low trigger mandatory for good timing resolution
- Petiroc can trigger on first photoelectron
- Petiroc is low noise : single photon identification

Thanks to
David Brasse – IPHC – IN2P3
Jacques Wurtz– IPHC – IN2P3



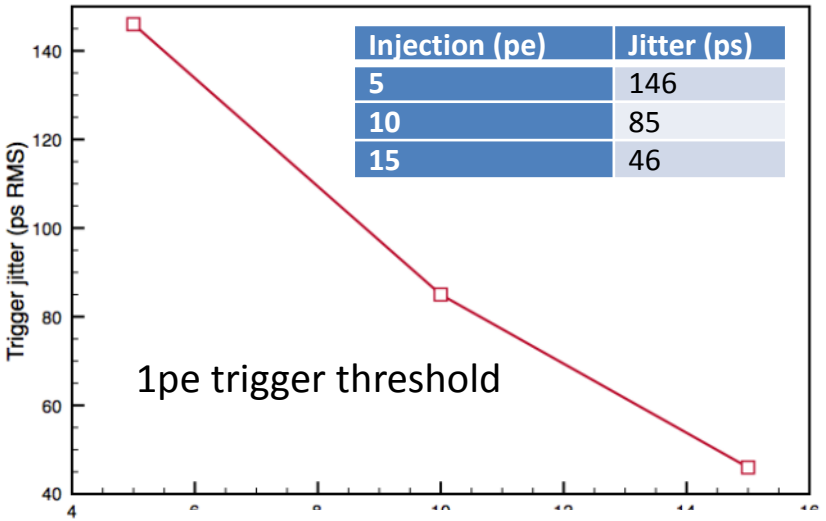
2 ns/div



2 ns/div

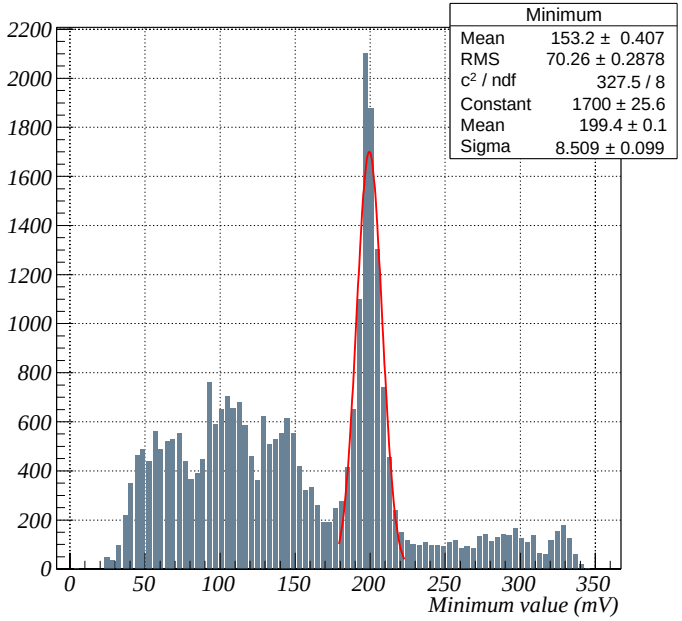
Time and Charge measurements with SiPM

- Jitter vs injection
  - Laser illumination of 1x1mm SiPM
  - 5 →15 pe, threshold 1pe
  - Jitter improves with signal, down to 50ps



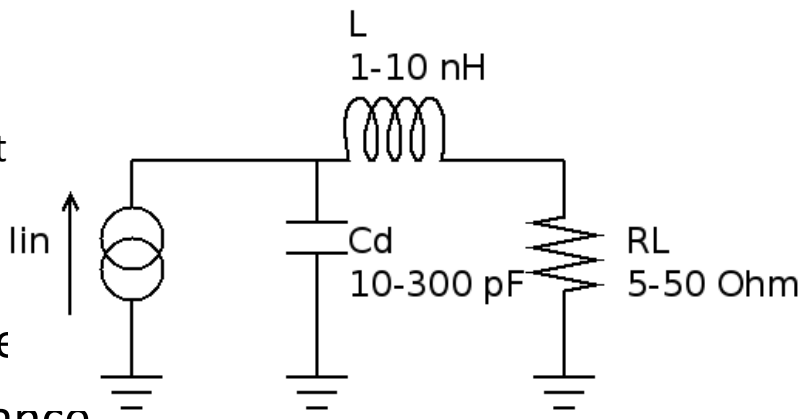
Injection (pe)	Jitter (ps)
5	146
10	85
15	46

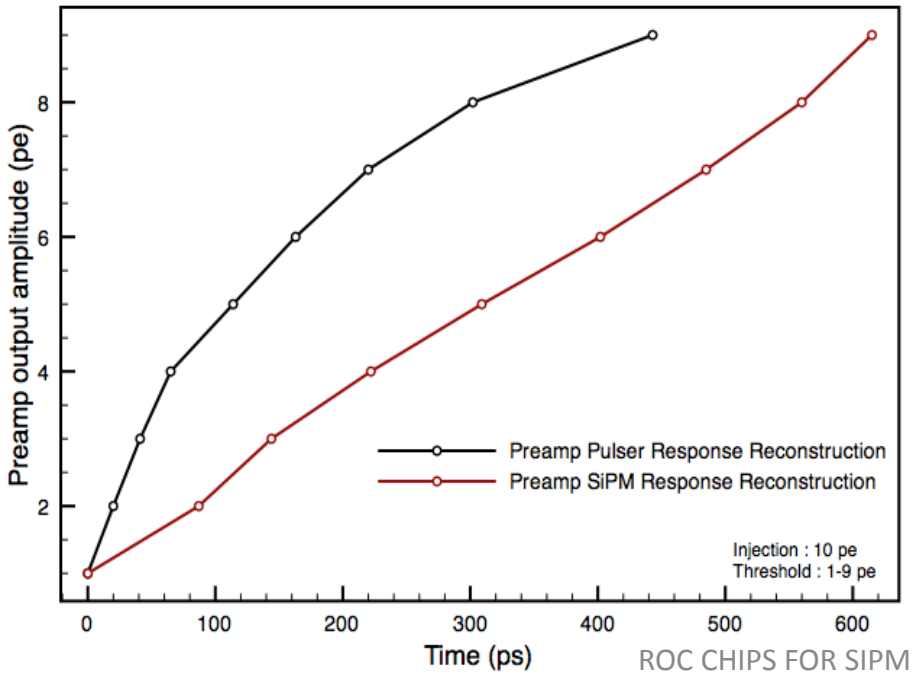
- Energy resolution
  - Raw data, no correction for non linearities
  - Using 3x3x5mm LYSO:Ce crystal & 3x3mm Ketek SiPM
  - Na22 source
  - Petiroc self-triggered (threshold 5pe)
  - Energy resolution: 9.5% FWMH

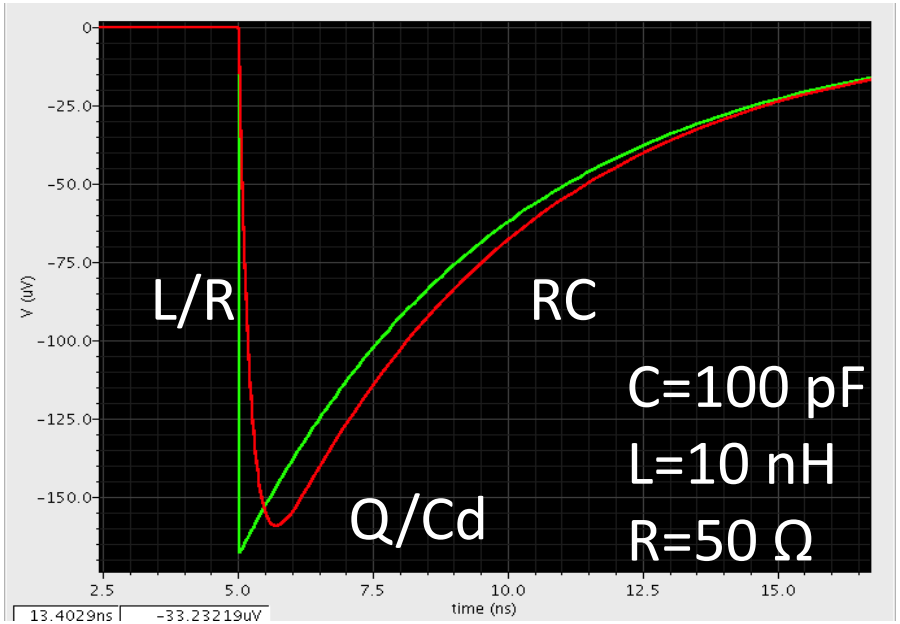


PETIROC1: BW

- Pulser vs SiPM comparison
- SiPM is significantly slower than Petiroc
  - Pulser with 100pF injection capacitance, 10pe inject
  - SiPM illuminated with laser pulse, 10pe measured
  - Threshold from 1pe to 9pe
- Petiroc bandwidth meas. : 877MHz with pulse
- With SiPm: limitation due to the stray inductance

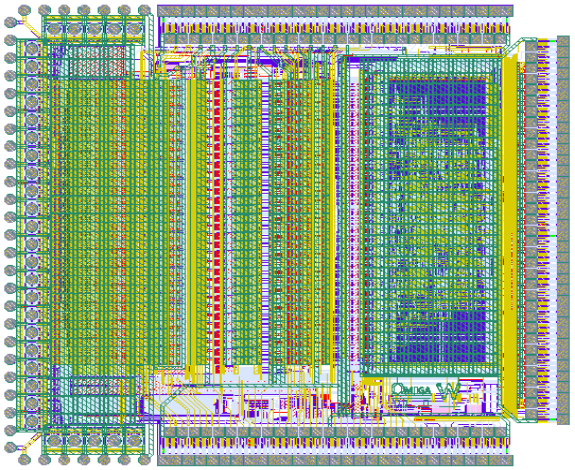




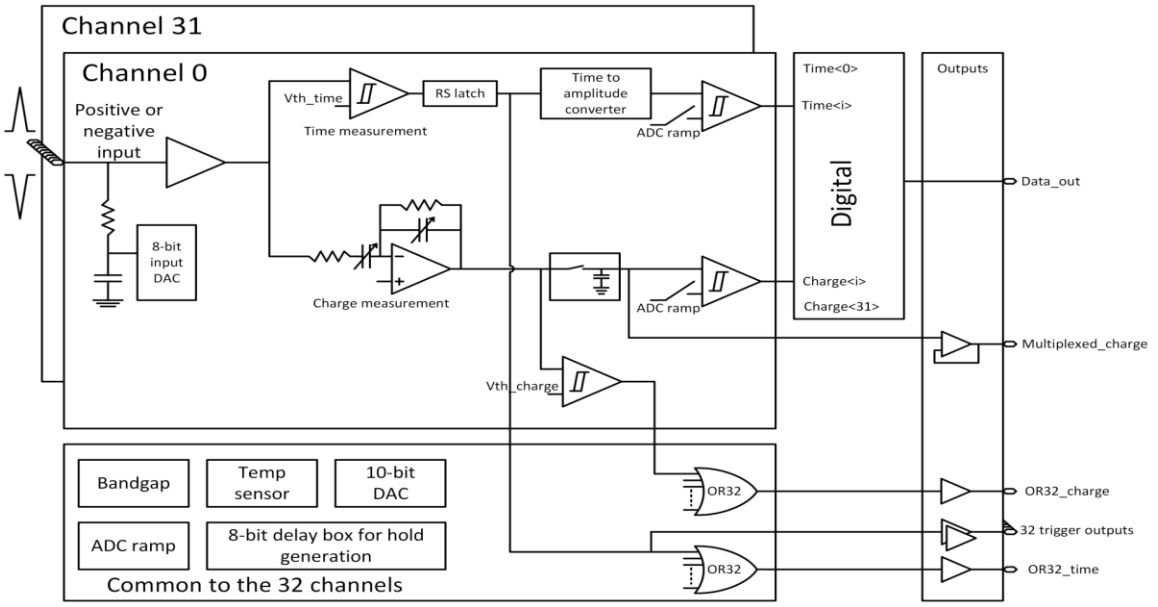


PETIROC2

- Time of Flight read-out chip with embedded TDC (25 ps bin) and ADC
- Dynamic range: 160 fC up to 400 pC
- 32 channels (negative input)
  - 32 trigger outputs
  - NOR32_chrage
  - NOR32 time
  - Charge measurement over 10 bits
  - Time measurement over 10 bits
  - One multiplexed charge output
- Common trigger threshold adjustment and 6bit-dac/channel for individual adjustment
- Variable shaping time of the charge shaper
- 32 8bit-input dac for SiPM HV adjustment
- Power consumption 6 mW/ch
- Front-end
  - common emitter SiGe fast amplifier, DC coupled to detector
  - Fast SiGe discriminator

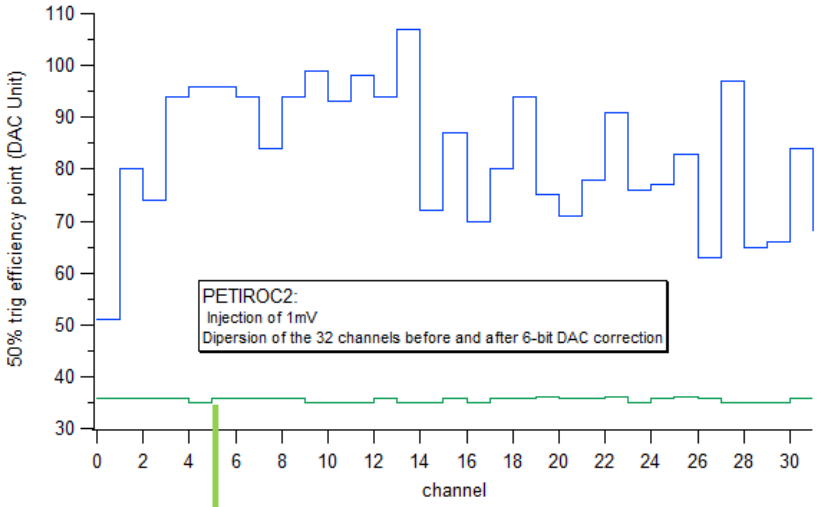


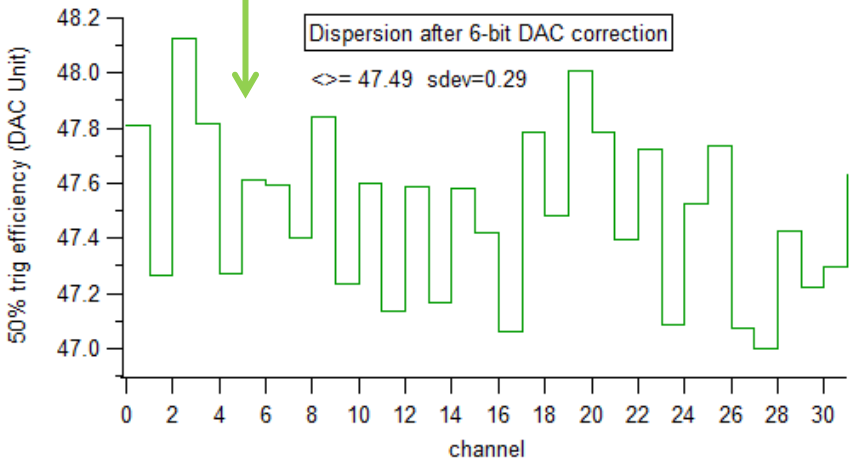
weeroc

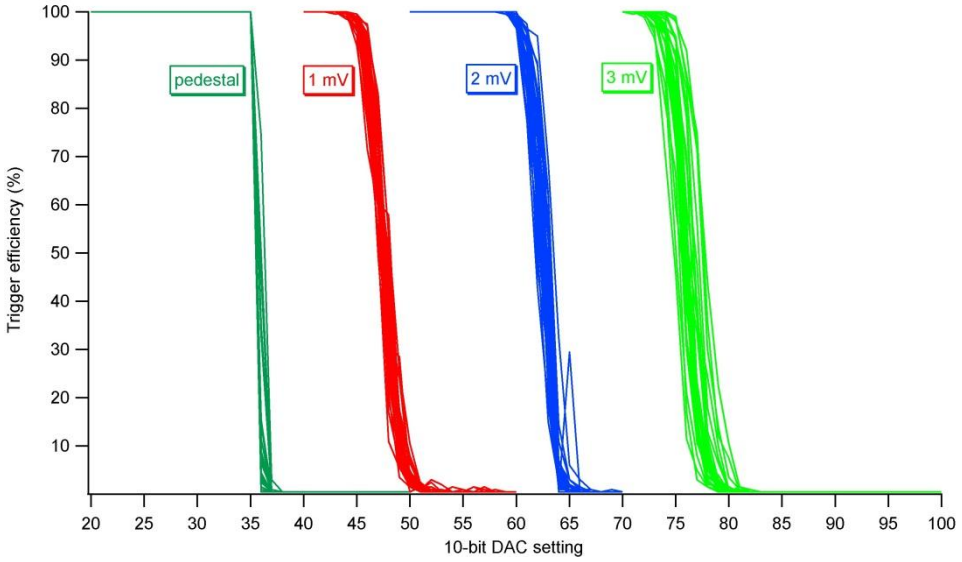


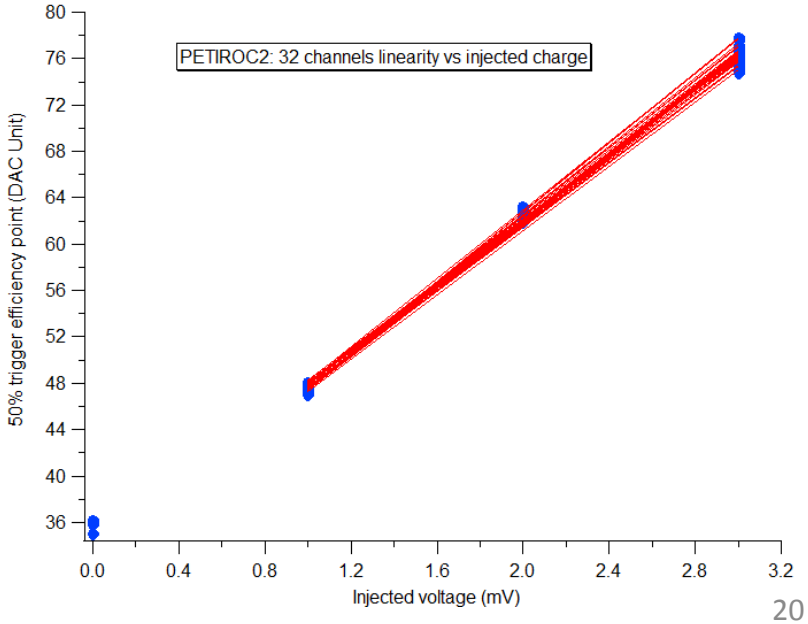
PETIROC2: Scurve measurement

- Trigger efficiency measurements:



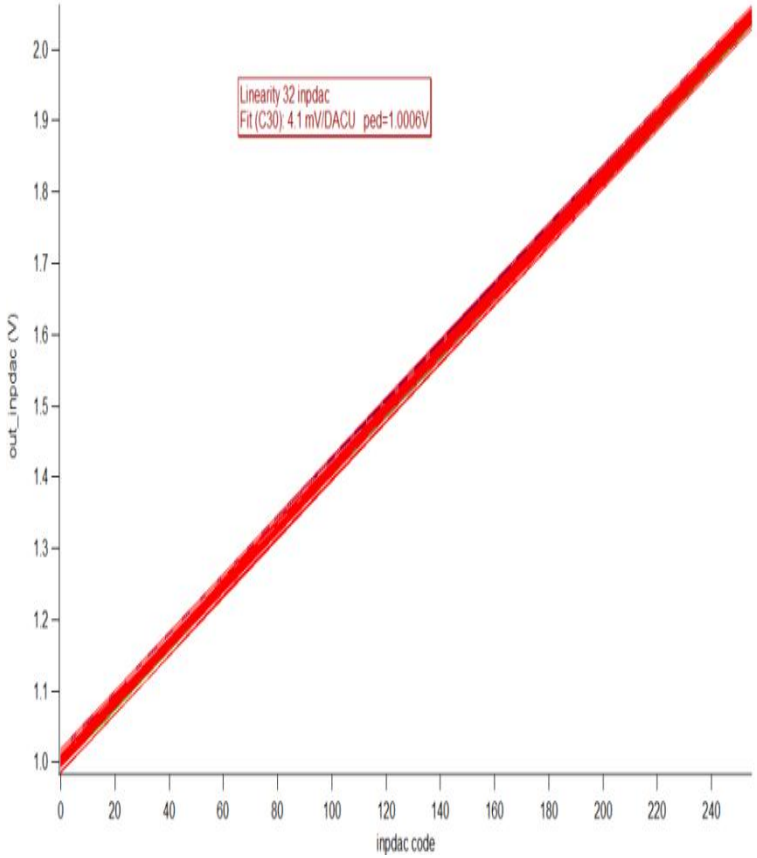




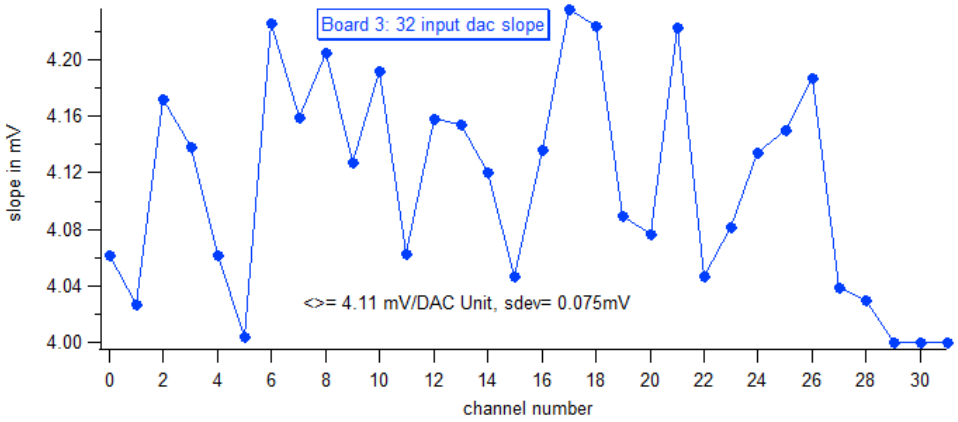


PETIROC2: Input DAC uniformity

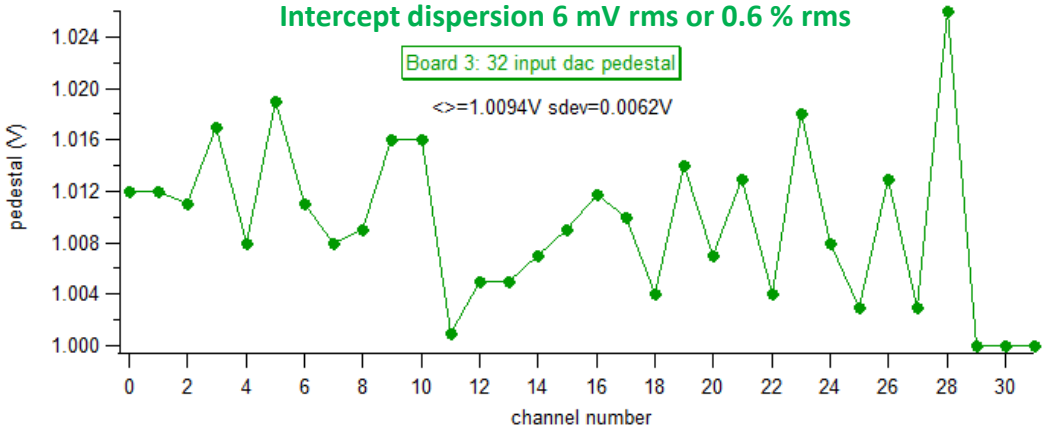
- Linearity and dispersion of the 32 8-bit input DAC



Slope dispersion 75 uV rms or 2% rms

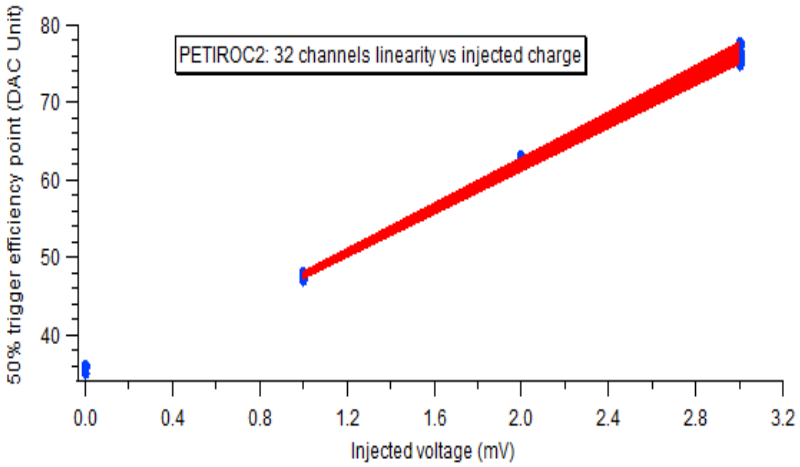


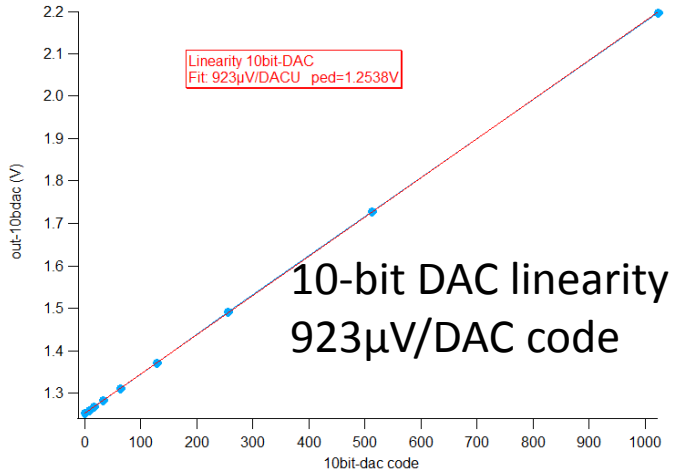
Intercept dispersion 6 mV rms or 0.6 % rms



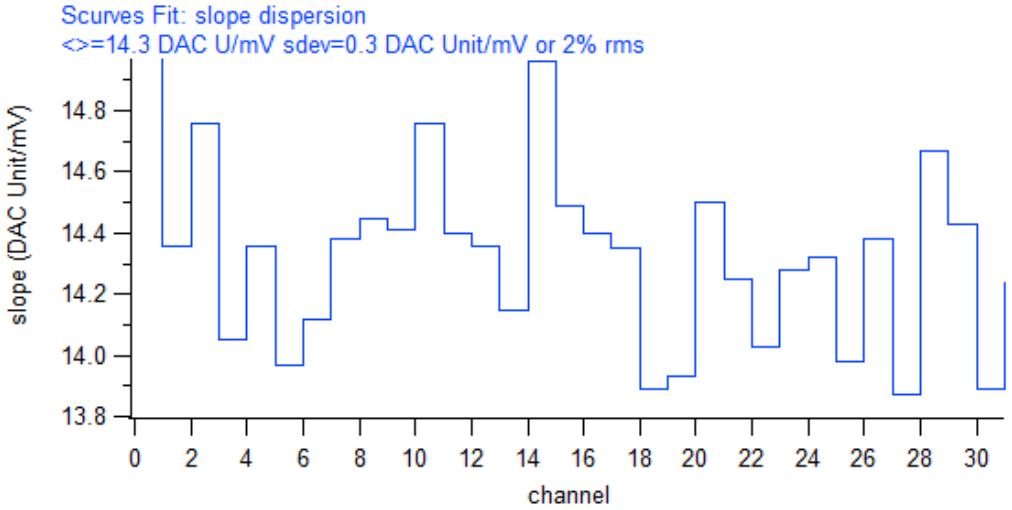
PETIROC2: efficiency uniformity

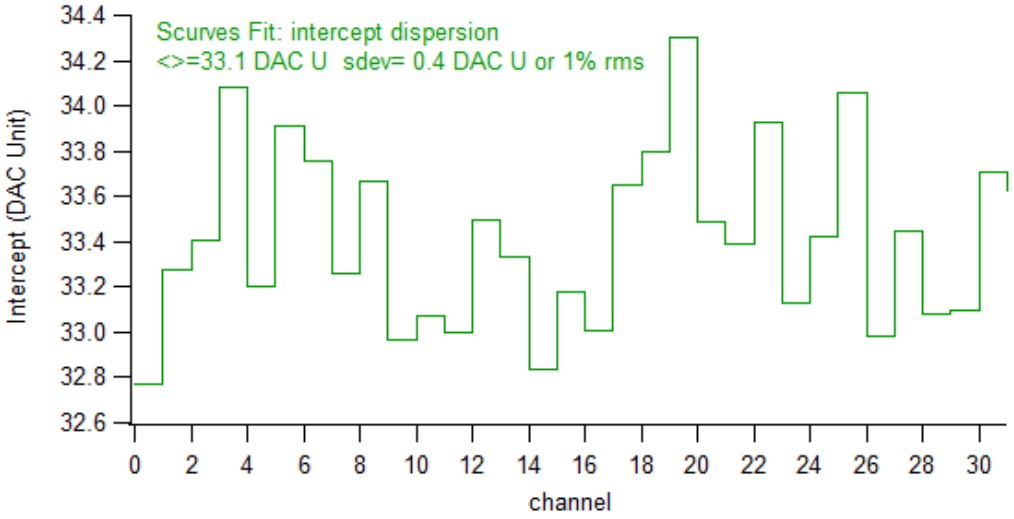
- Trigger efficiency measurements: Linearity
- One 10-bit DAC Unit= 923 µV





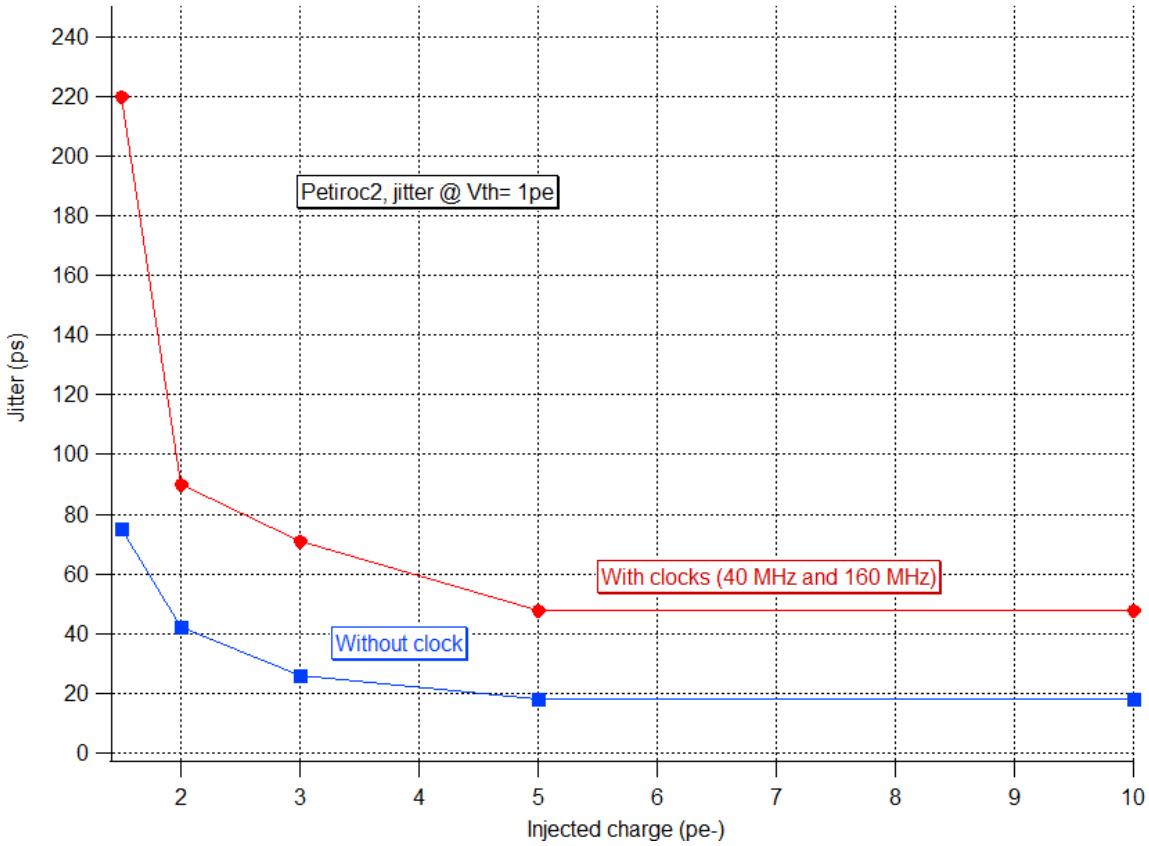
10-bit DAC linearity
923µV/DAC code





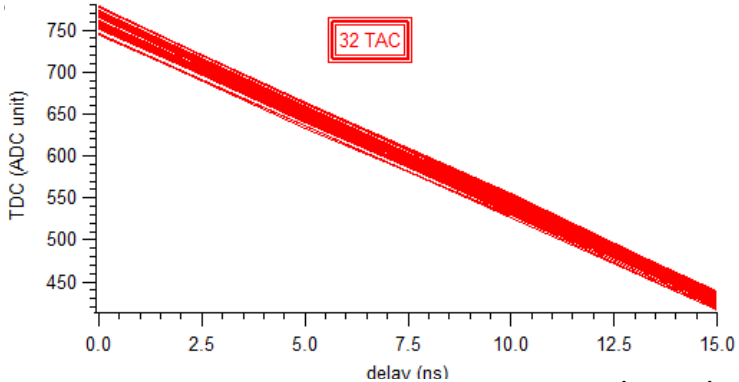
PETIROC2: Time measurement

- Jitter vs threshold & injection
- Jitter improves with signal
- Clock couplings (understood)
- Jitter below 20ps

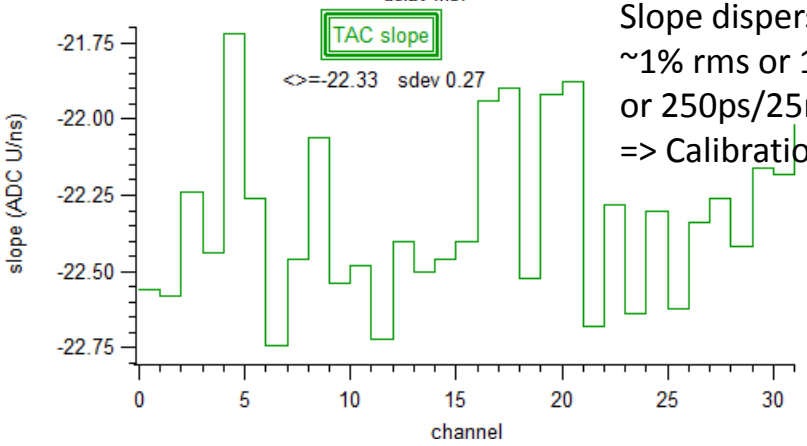


PETIROC2: TAC measurement

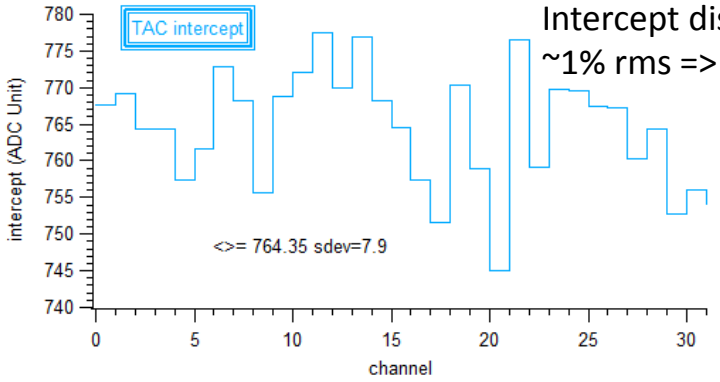
Omega



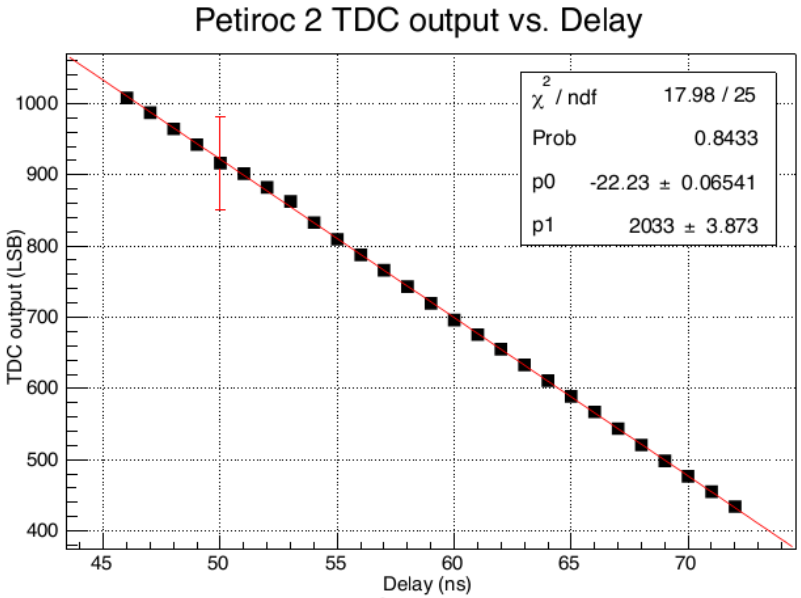
weeroc

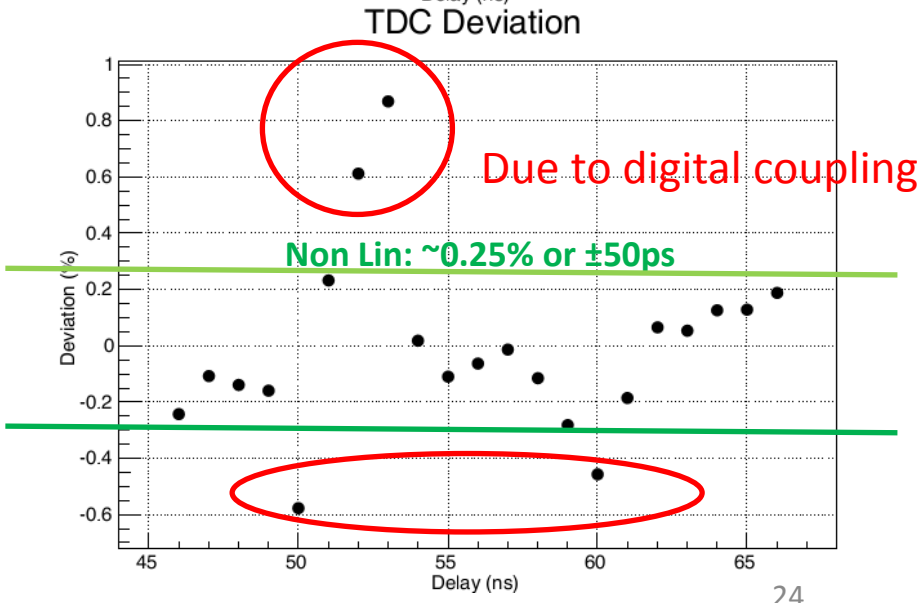


Slope dispersion:
~1% rms or 10ps/1ns
or 250ps/25ns
=> Calibration

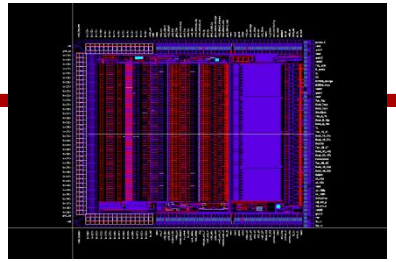


Intercept dispersion:
~1% rms => Calibration

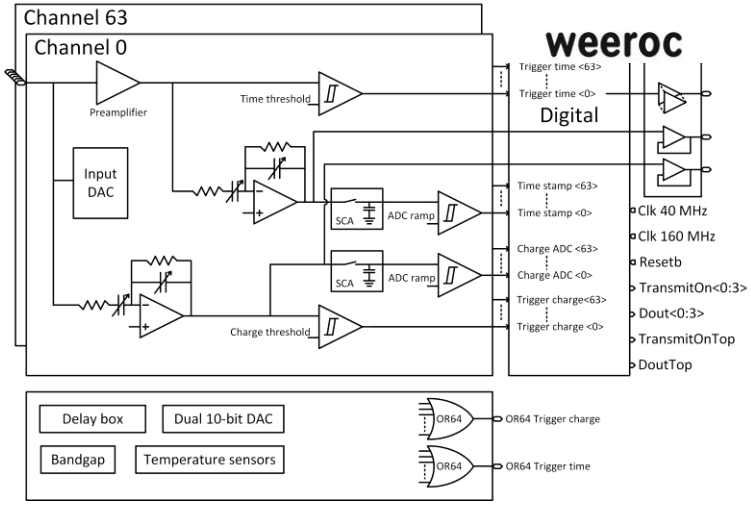


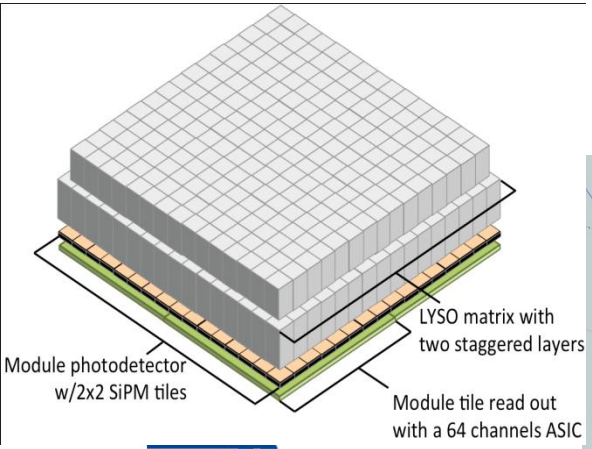


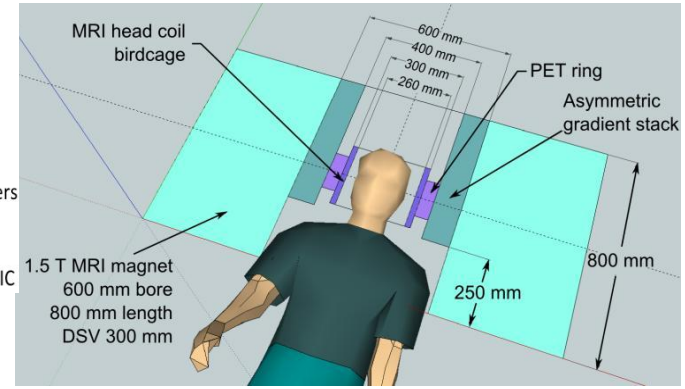
TRIROC description

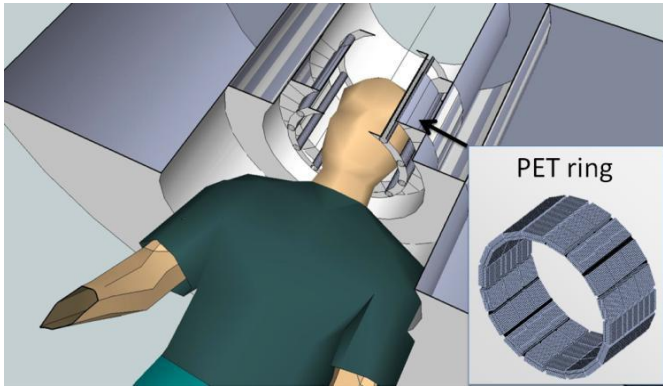


- Full system-on-chip :
  - On-chip zero suppress, self trigger, Time and energy conversion
- 64-channel SiPM readout : positive & negative polarity inputs
- Input DAC for SiPM gain non-uniformity correction
- Time Stamp and ADC charge outputs
- 64-channel trigger outputs
- Power Pulsing : Analog, ADC & Digital
- Event rate : 30k events/s, limited by digital processing









The research leading to these results has received funding from the European Union Seventh Programme under grant agreement n° 602621

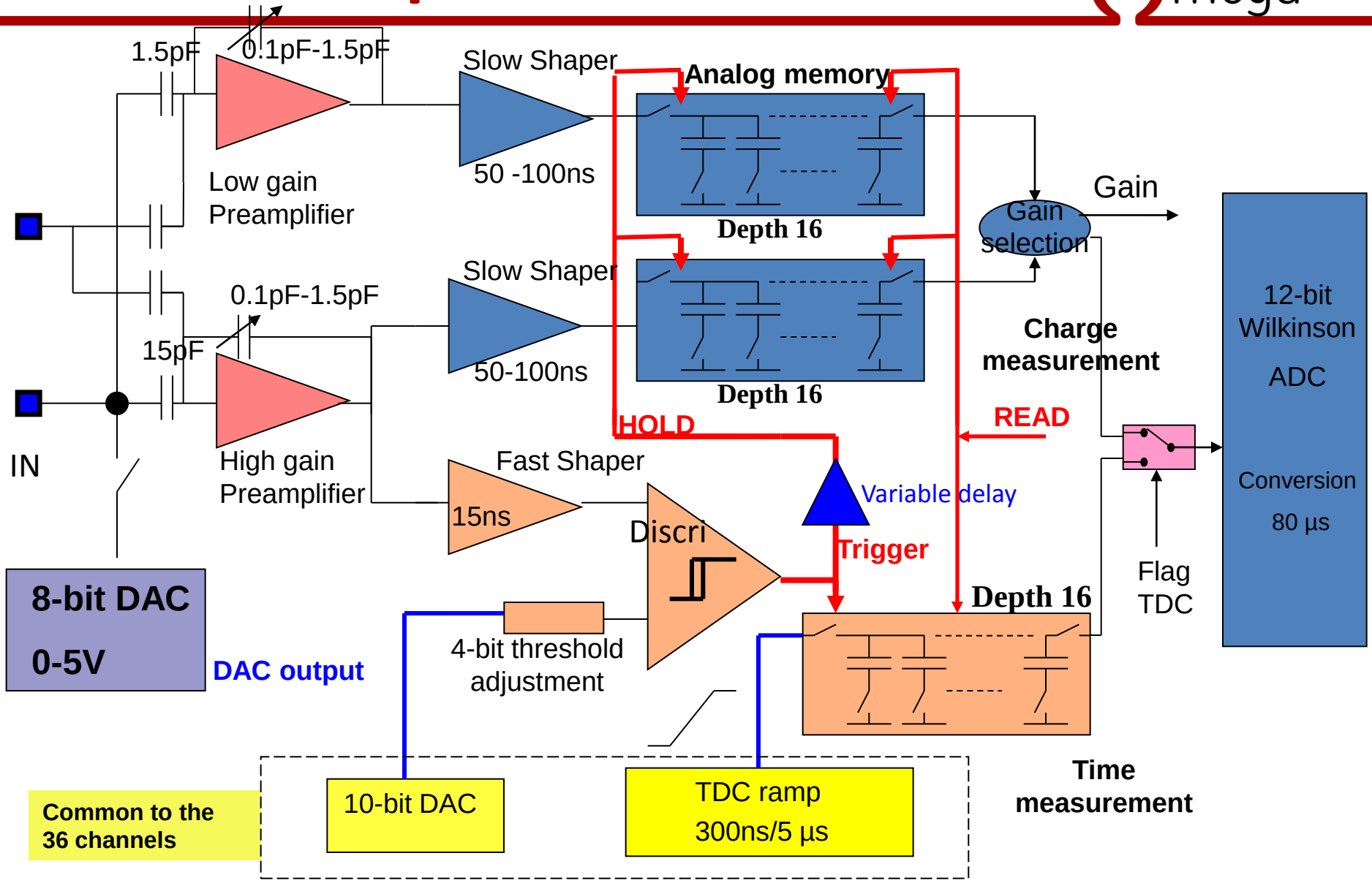
SUMMARY

- SPIROC, EASIROC: produced in large quantity, used by many groups, many applications
- CITIROC, PETIROC, TRIROC more recent chips, higher speed for charge and time measurements (<100ps), low power
- Engineering run (0.35µm SiGe AMS) foreseen at the end of this year http://omega.in2p3.fr/
- Move to SiGe 130nm or 180nm in AIDA2 to further improve the digital part http://www.weeroc.com/

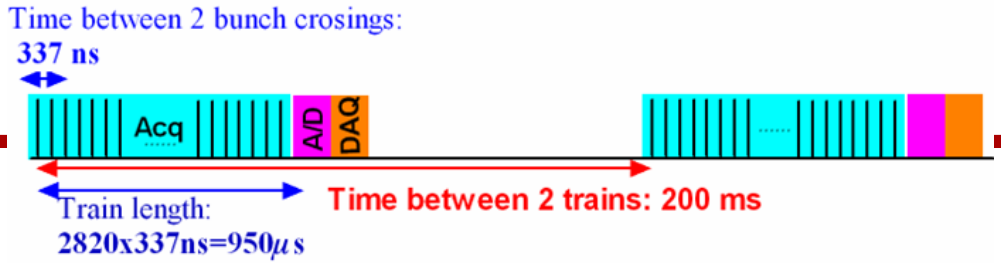
Chip	Detector	Ch	Polarity	Dyn Range	Specificities
MAROC	PM	64	<0	5 fC - 5 pC	64 trig outputs, internal 8/10/12-bit ADC (for charge measurment)
SPACIROC	PM	64	<0	2 pC- 220 pC	Fast photon counting (50MHz)
PARISROC	PM	16	<0	50 fC - 100 pC	Internal TDC (<1ns), 16 trig outputs
HARDROC	RPC	64	<0	2 fC - 10 pC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
MICROROC	µMEGAS/GEM	64	<0	0.2 fC - 500 fC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
SKIROC	Si pin diodes	64	>0	0.3 f C - 10 pC	Internal 12-bit ADC for charge measurement
SPIROC	SiPM	36	>0	10 fC - 300 pC	36 HV SiPM tuning (8 bits), Internal 12-bit ADC for charge and time measurement
EASIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
CITIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
PETIROC	SiPM	32	<0	100fC – 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)
TRIROC	SiPM	64	Both	100 fC- 300 pC	64 HV SiPM tuning (8 bits), 64 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)

BACKUP SLIDES

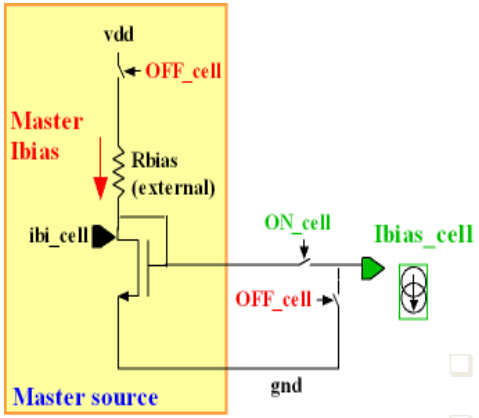
SPIROC2 simplified schematics



POWER PULSING



- **Requirement:**
  - **25 µW/ch with 0.5% duty cycle**
  - **500 µA for the entire chip**



- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **SK2 power consumption measurement:**
  - 123 mA x 3.3V ≈ 400 mW => **6 mW/ch**

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ANR
CALIIMAX-HEP

- **4 Power pulsing lines** : analog, conversion, dac, digital
- Each chip can be forced **on/off by slow control**

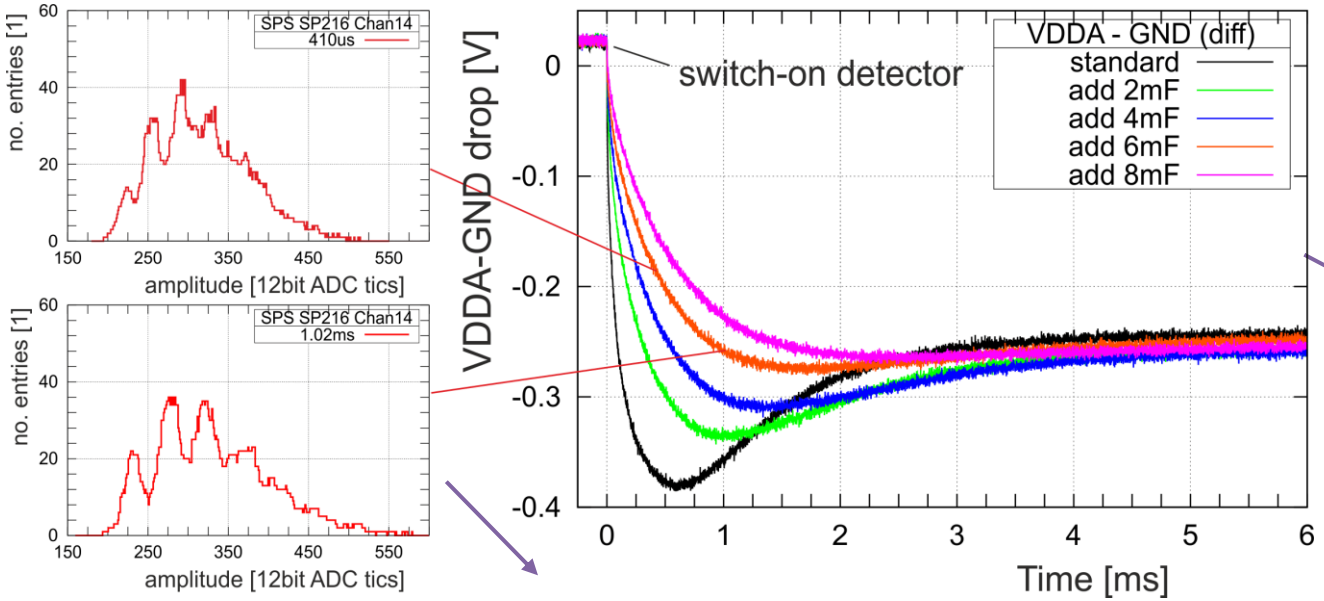
MEASUREMENTS		
Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

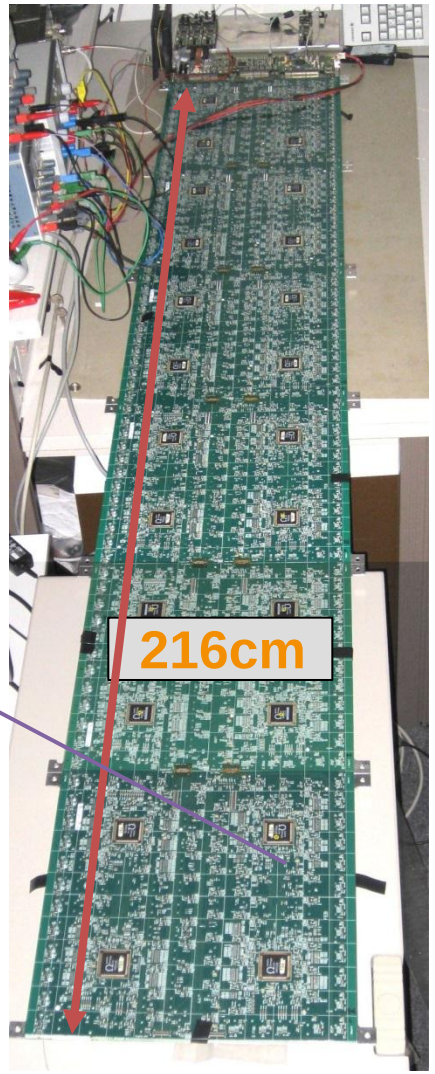
Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 µW/ch

SPIROC2 POWER PULSING

Mathias Reinecke, DESY, AHCAL meeting, 2013, December 13th

- Switched Current: 2.75A (analog supply voltage VDDA).
- Voltage drop across 216cm (dominated by flexleads):
  - 0.18V on VDDA (19mΩ per HBU2+flexlead)
  - 0.04V on GND (4mΩ per HBU2+flexlead)
- Studies ongoing, e.g. additional block capacitors:

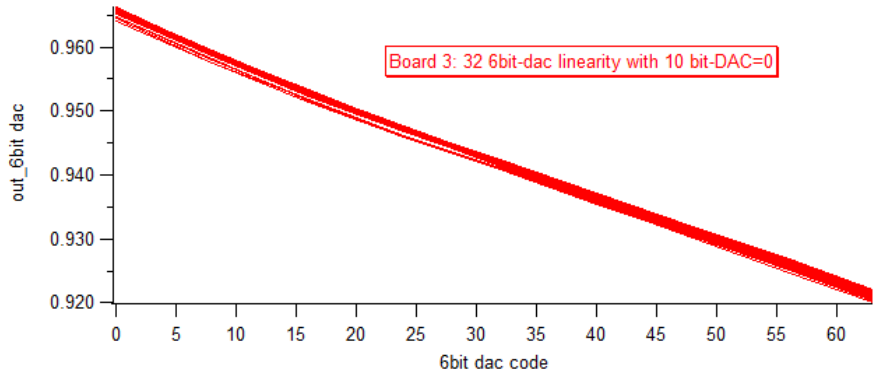


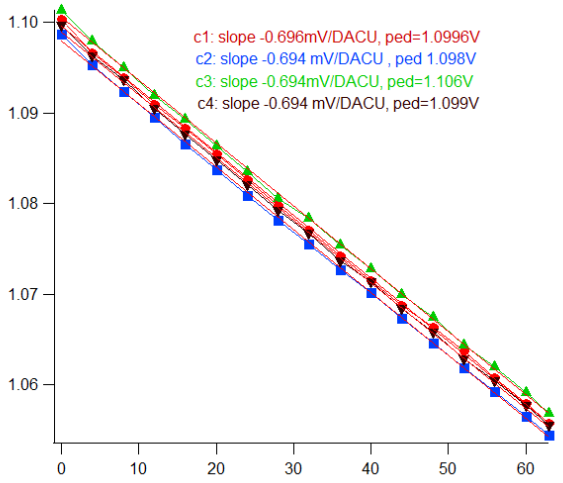


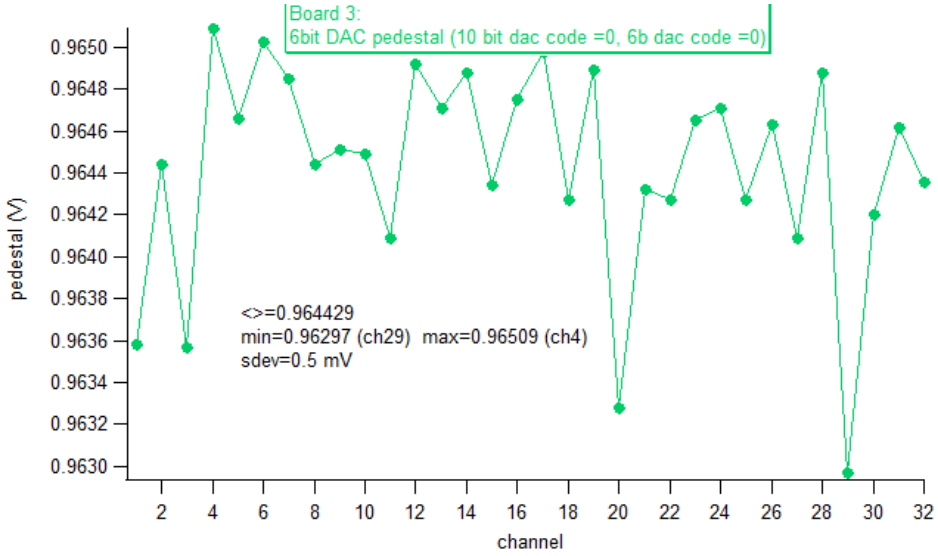
- Switch-on time T_on too small: Low gain and high noise!

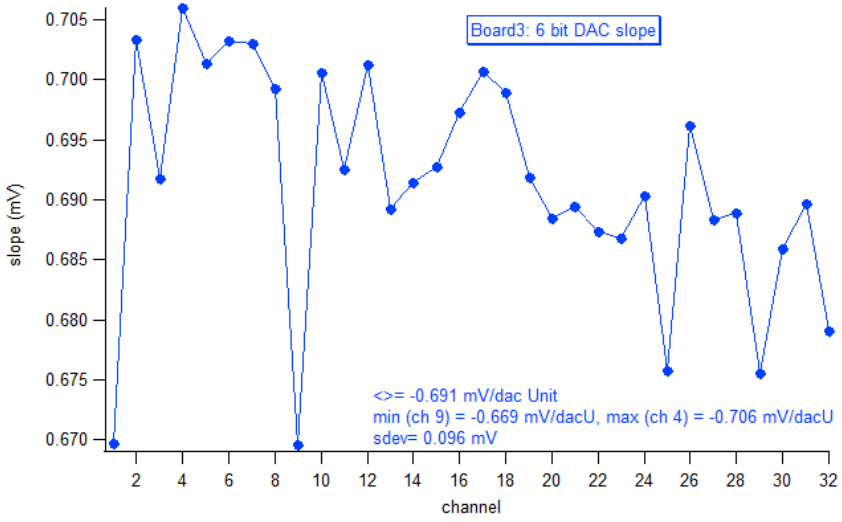
PETIROC2: uniformity measurements

- 6 bit dac/channel to adjust the threshold









PETIROC1: Charge measurement

- Measurement up to 3000pe (10^6 SiPM gain)
- Linearity of :
  - 1% (2000pe)
  - 2% (2500pe)
  - 4% (3000pe)
- Good uniformity in the gain (0.6% RMS)
- Noise floor: 1.5pe RMS

→ dynamic range : 2000