The TDCpix ASIC: High Rate Readout of Hybrid Pixels with Timing Resolution better than 200 ps

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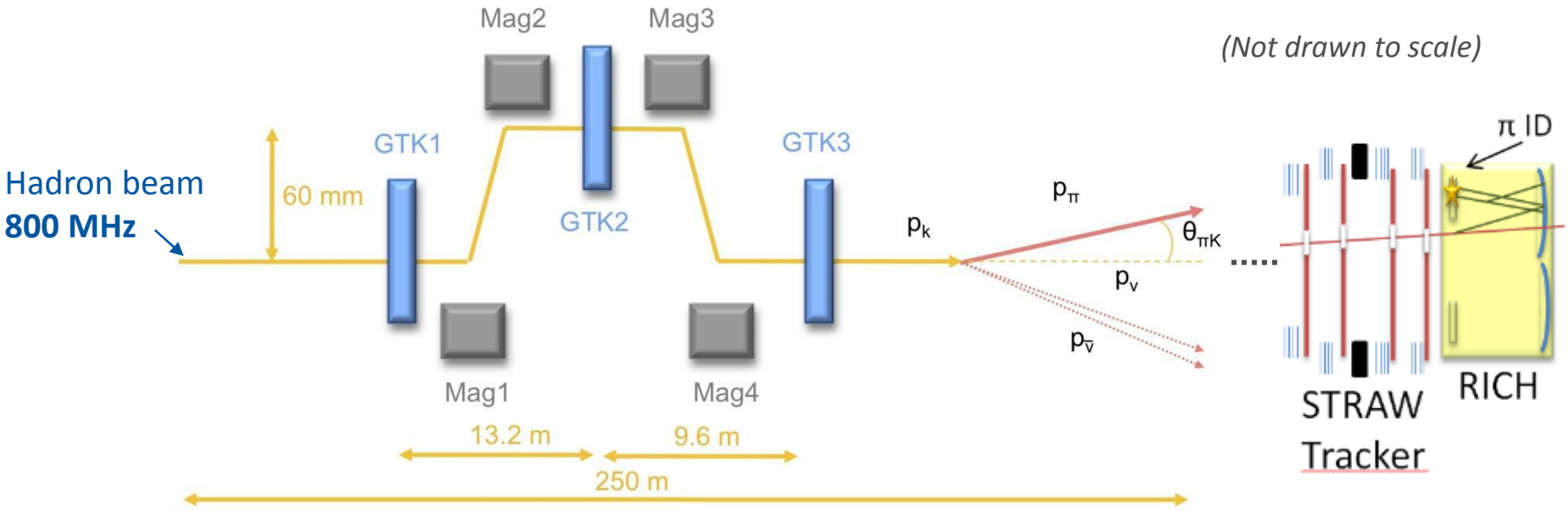
On behalf of the NA62 Gigatracker project

Outline

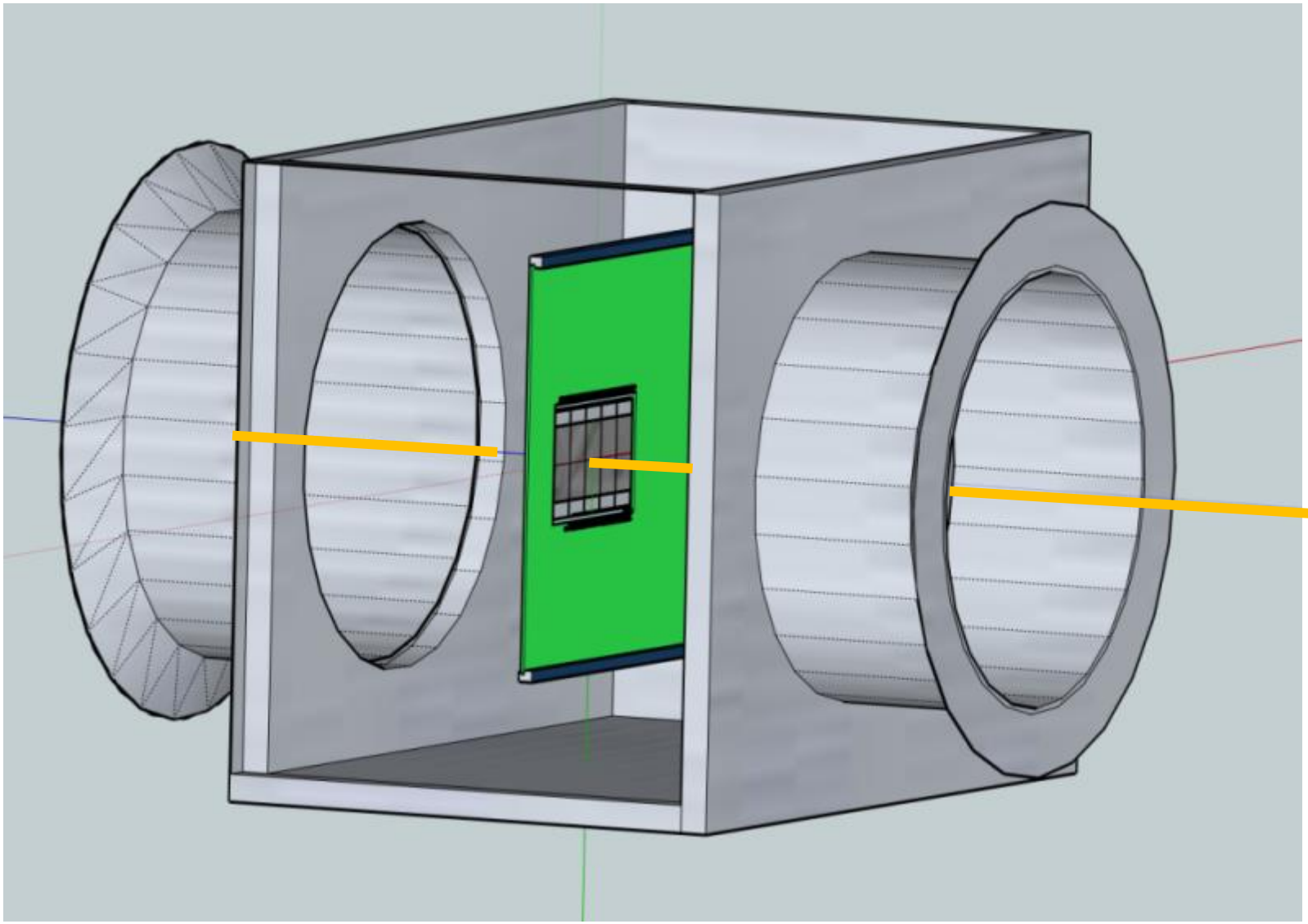
1. Target application: NA62 Gigatracker
2. TDCpix ASIC overview and capabilities
3. First tests and characterization

NA62 Gigatracker

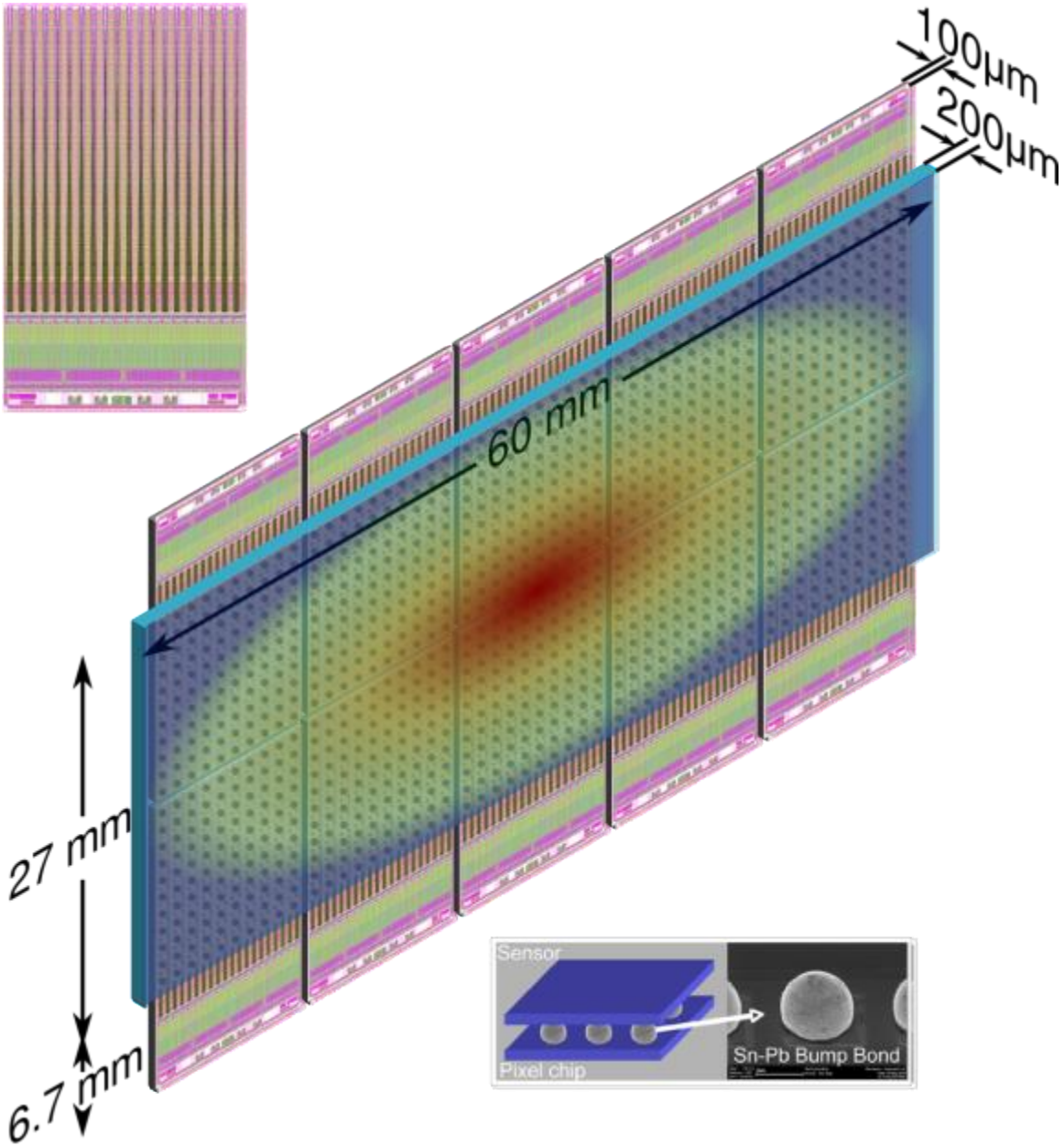


- NA62: Direct measurement of rare decay $K^+ \to p^+ n\bar{n}$
  - In flight decay of Kaons from high intensity beam
- Giagatracker
  - Measure momentum
  - **Time stamp with 200 ps resolution** (per station)

Gigatracker station

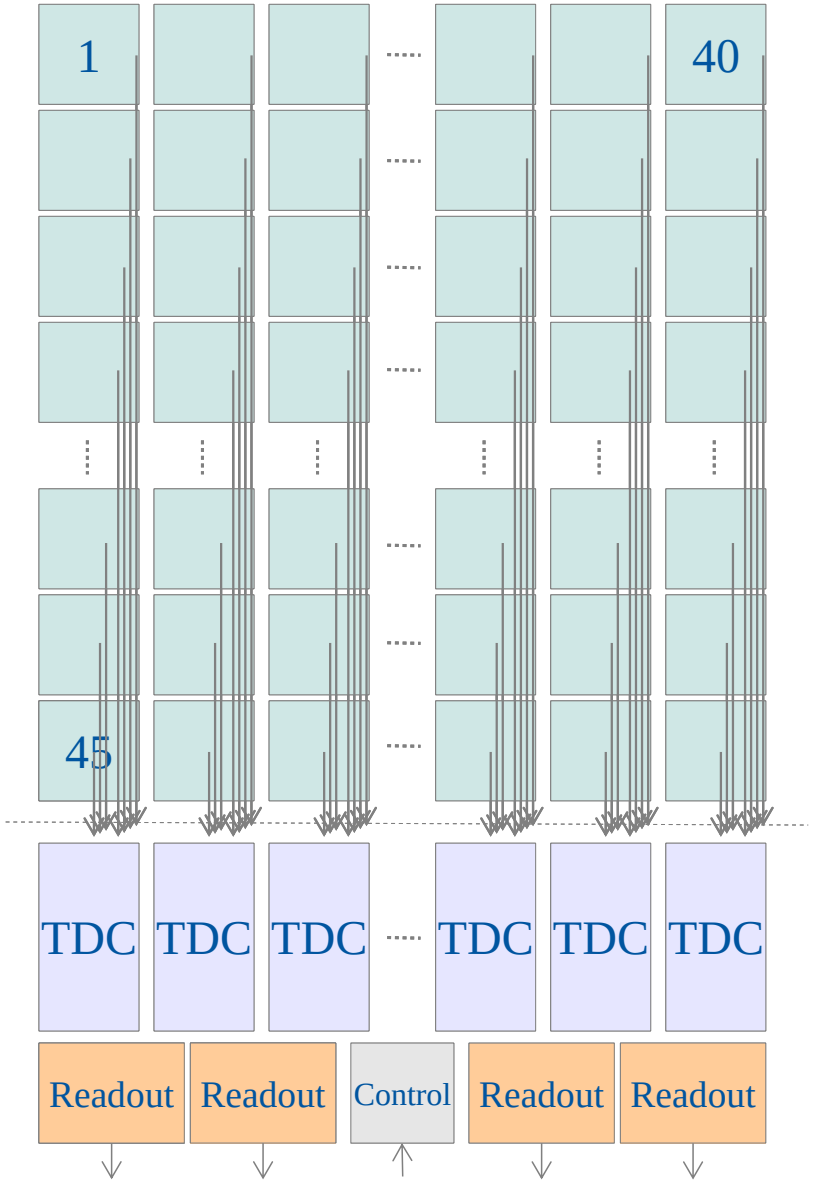


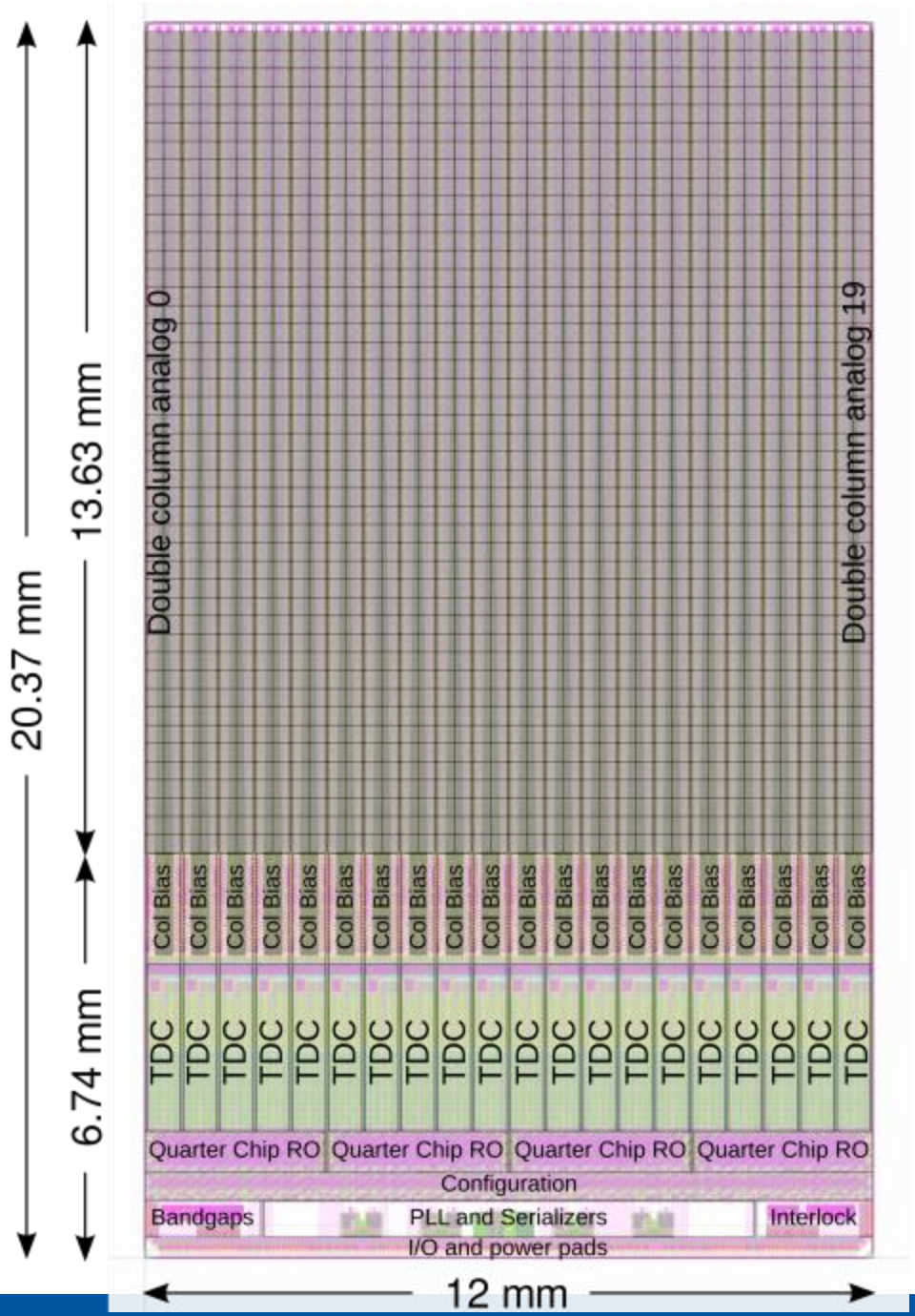
TDCpix



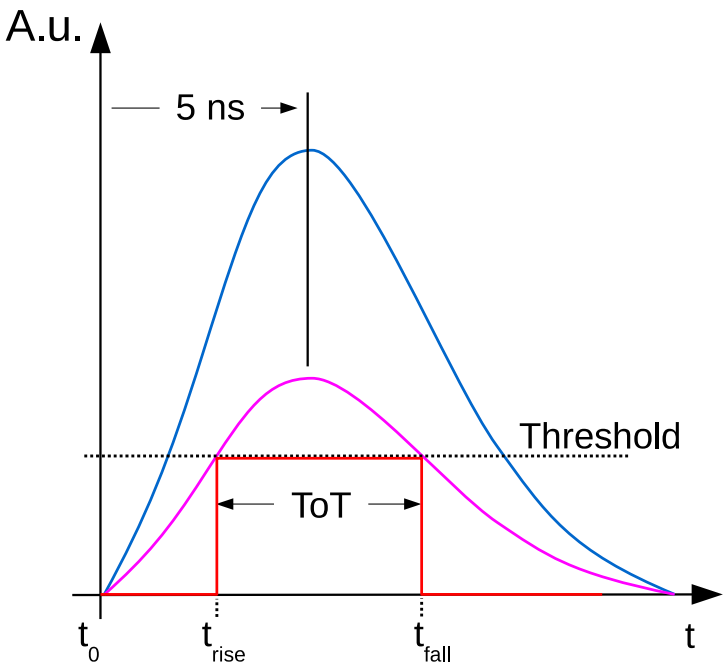
TDCpix overview

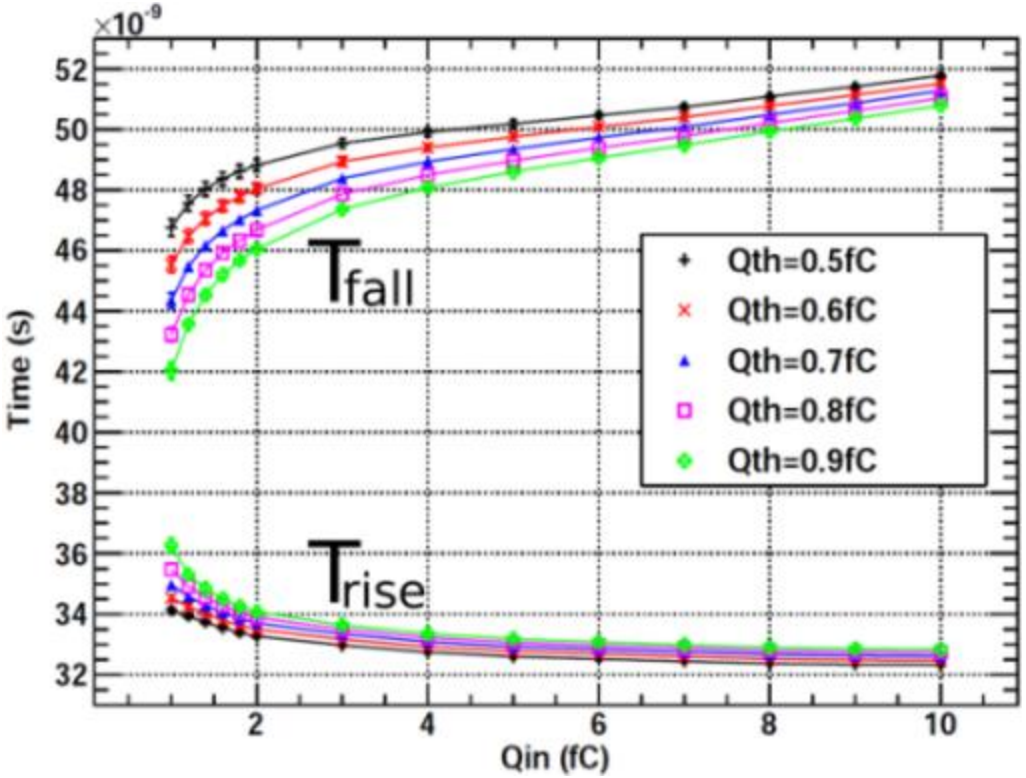
- 1800 channels
  - 45 × 40 pixels of 300 × 300 µm^2
- Hit rate 0.8 MHz/mm^2
  - 130 MHits/s per chip
- TDCs with Time Over Threshold
- No digital activity in the matrix
  - Discriminated pulses transmitted differentially to periphery
- CMOS 130 nm



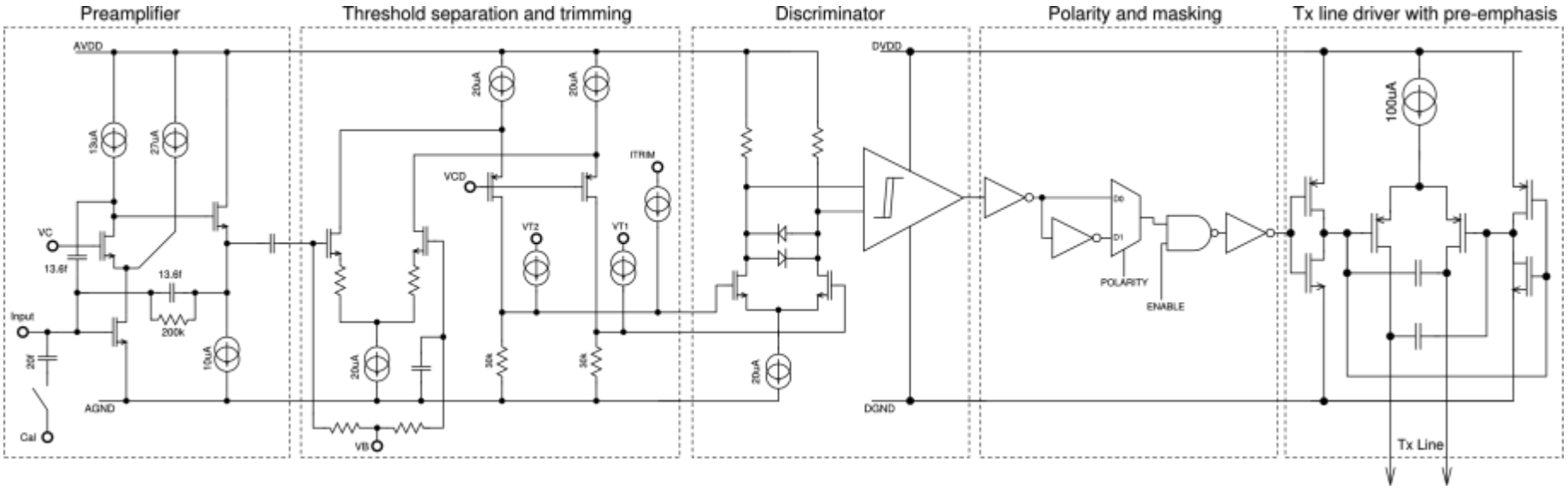

20.37 mm
13.63 mm
6.74 mm
Double column analog 0
Double column analog 19
Col Bias
TDC
Quarter Chip RO
Configuration
Bandgaps
PLL and Serializers
Interlock
I/O and power pads
12 mm

Time walk and Time Over Threshold



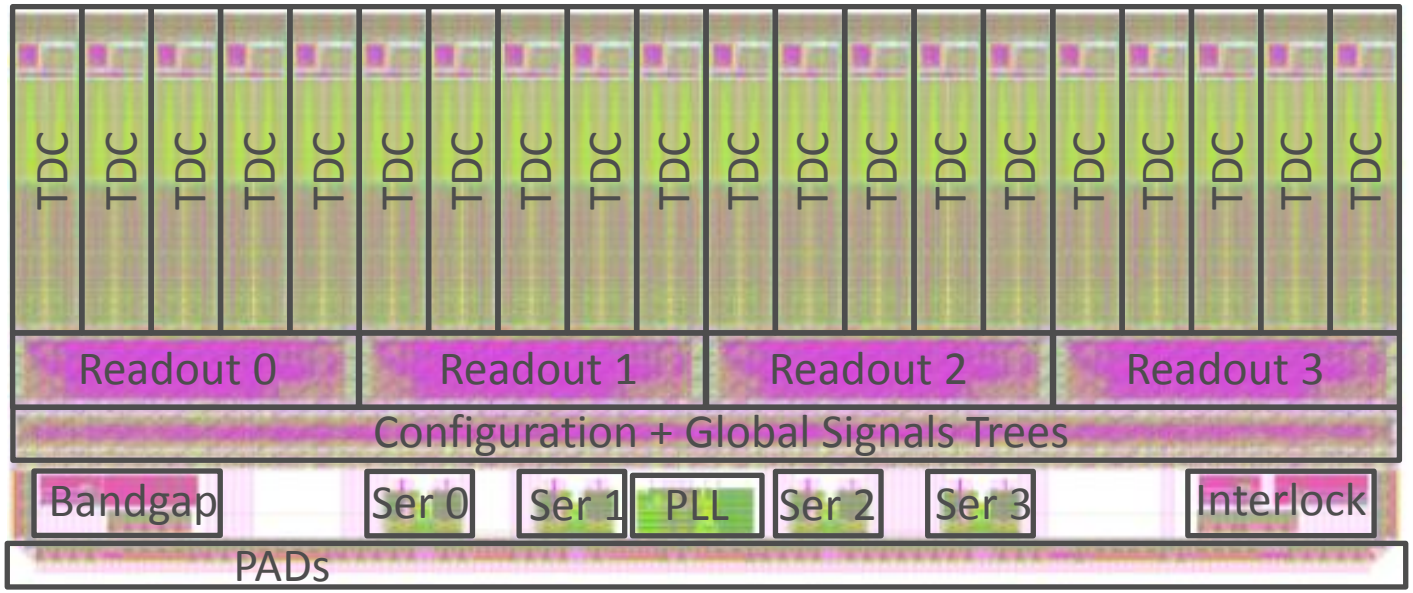


Pixel cell



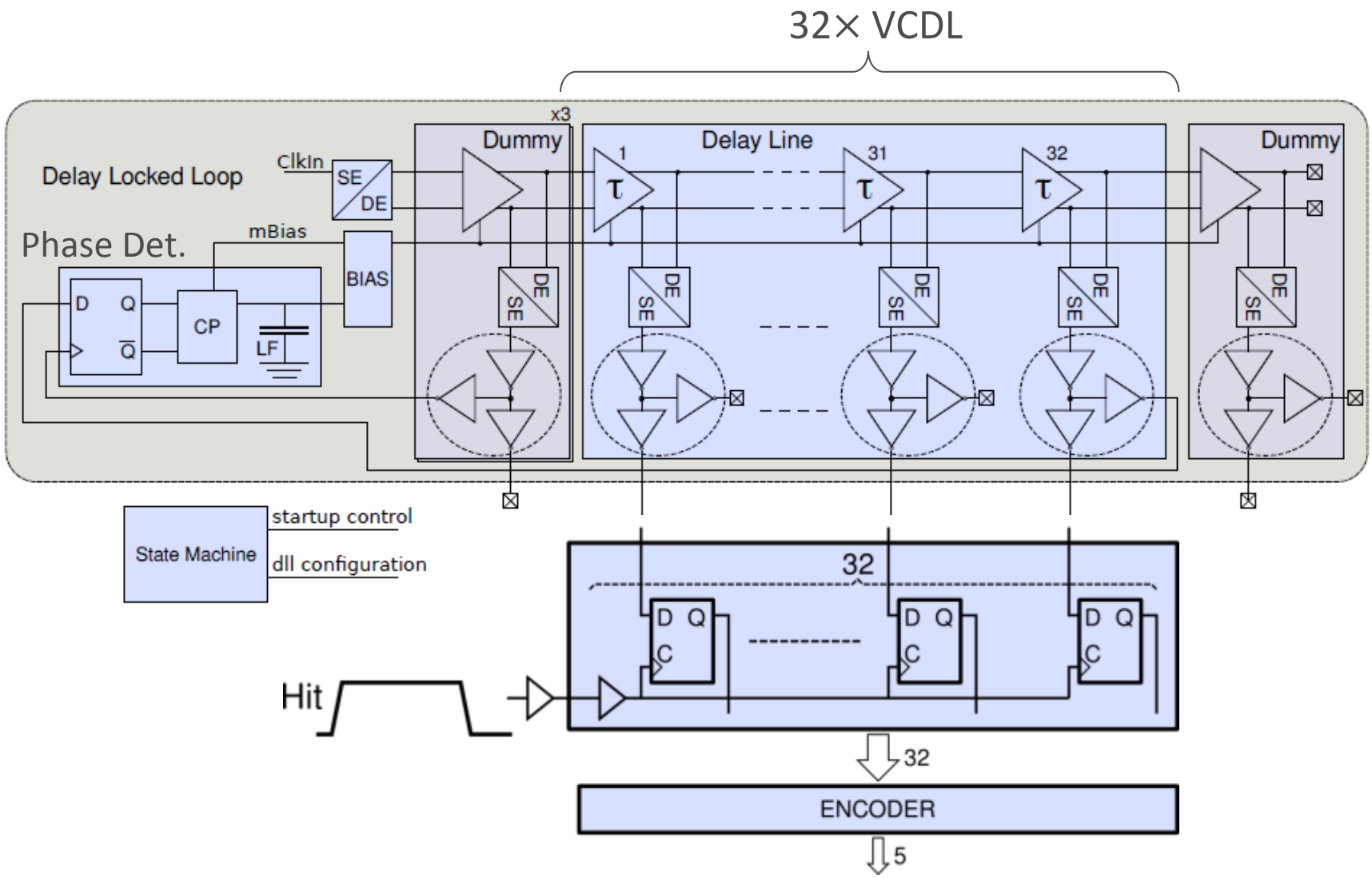
Dynamic Range	0.5-10 fC (3100-62500 e)
Dual polarity	YES
Gain	65 mV/fC (Typ)
Peaking time	5 ns
Current	140 µA (FE) + 160 µA (Discriminator, TX driver)
Input noise (C_{in} 250 fF)	2.6 mV (250 e)

Periphery



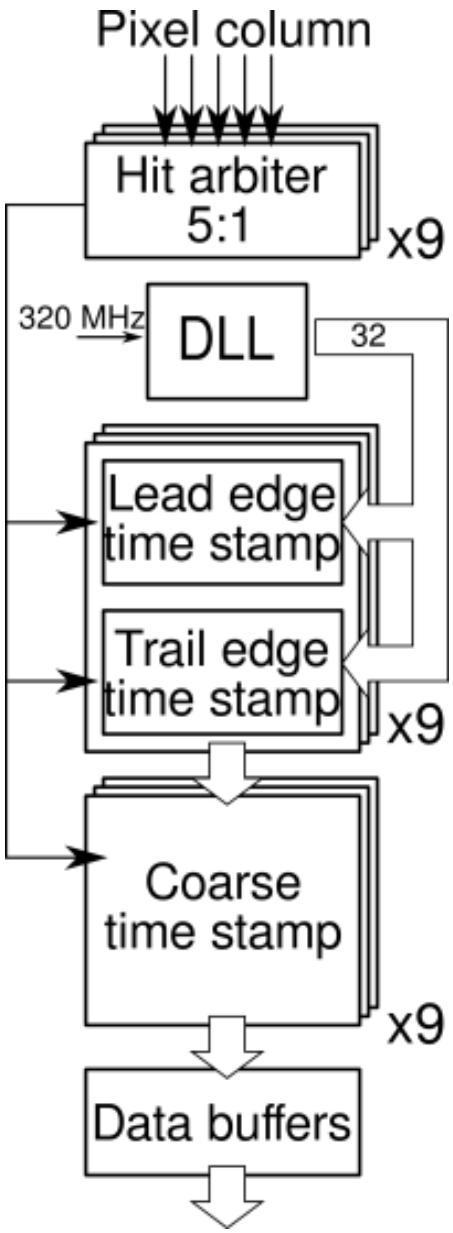
- TDCs
- 4 Readout Units
  - Data driven readout (trigger-less)
- Two bandgap references, temperature interlock

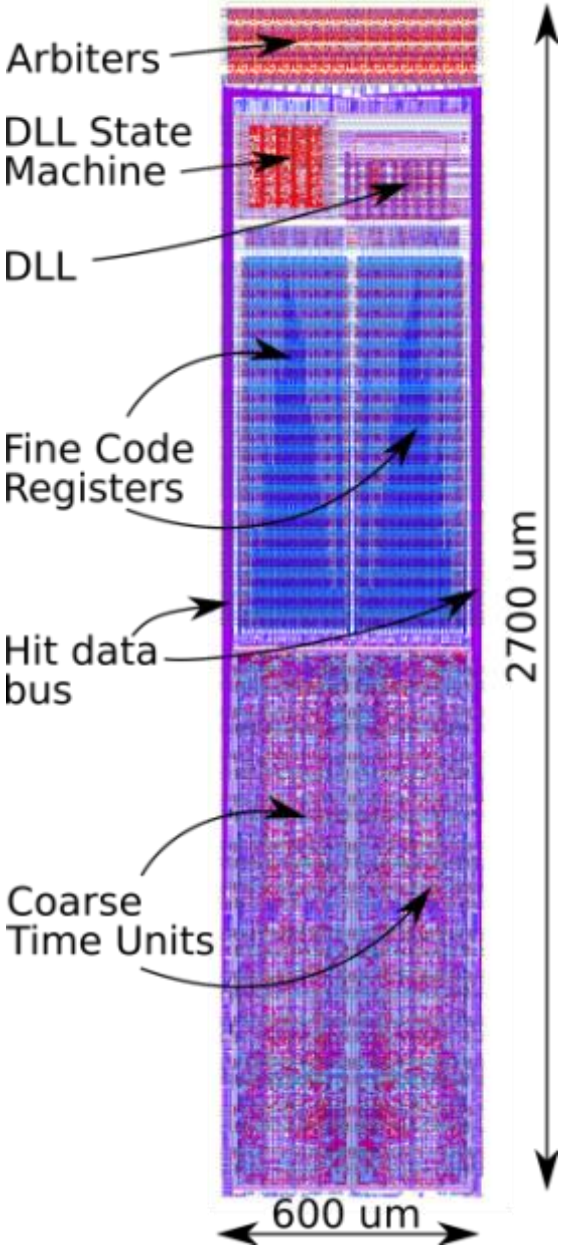
TDC based on Delay Locked Loop



TDC

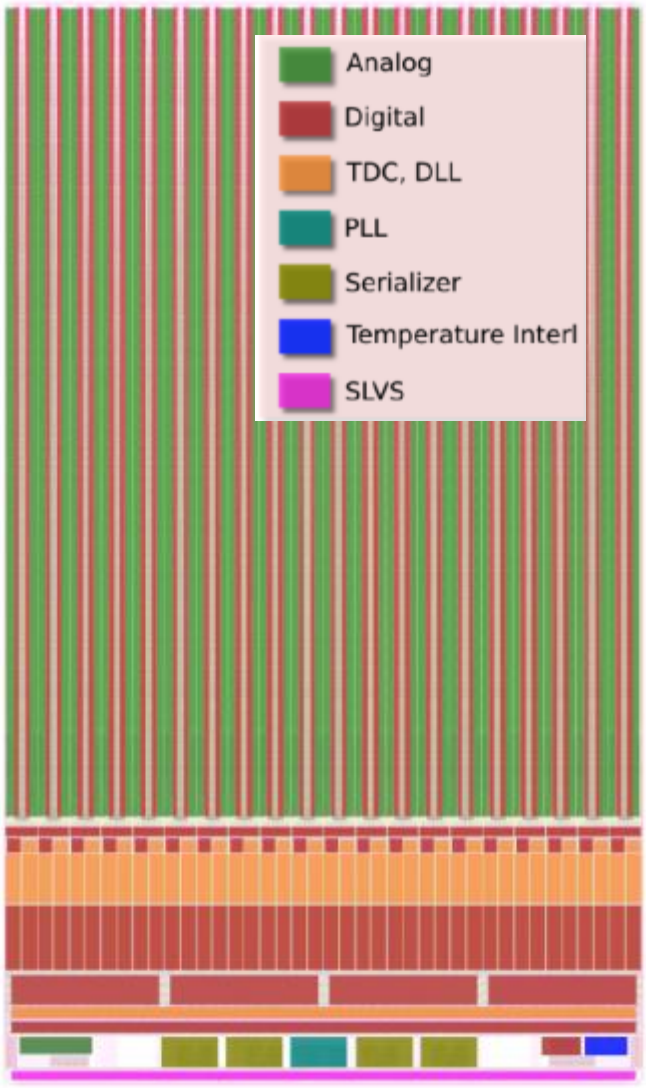
- 9 channels per column
  - 5 pixels each
    - Collision detection
  - Dual edge stamping
    - Time Over Threshold
- Delay Locked Loop
  - 320 MHz reference
    - 32 bins of 97.7 ps
  - Shared between two TDCs





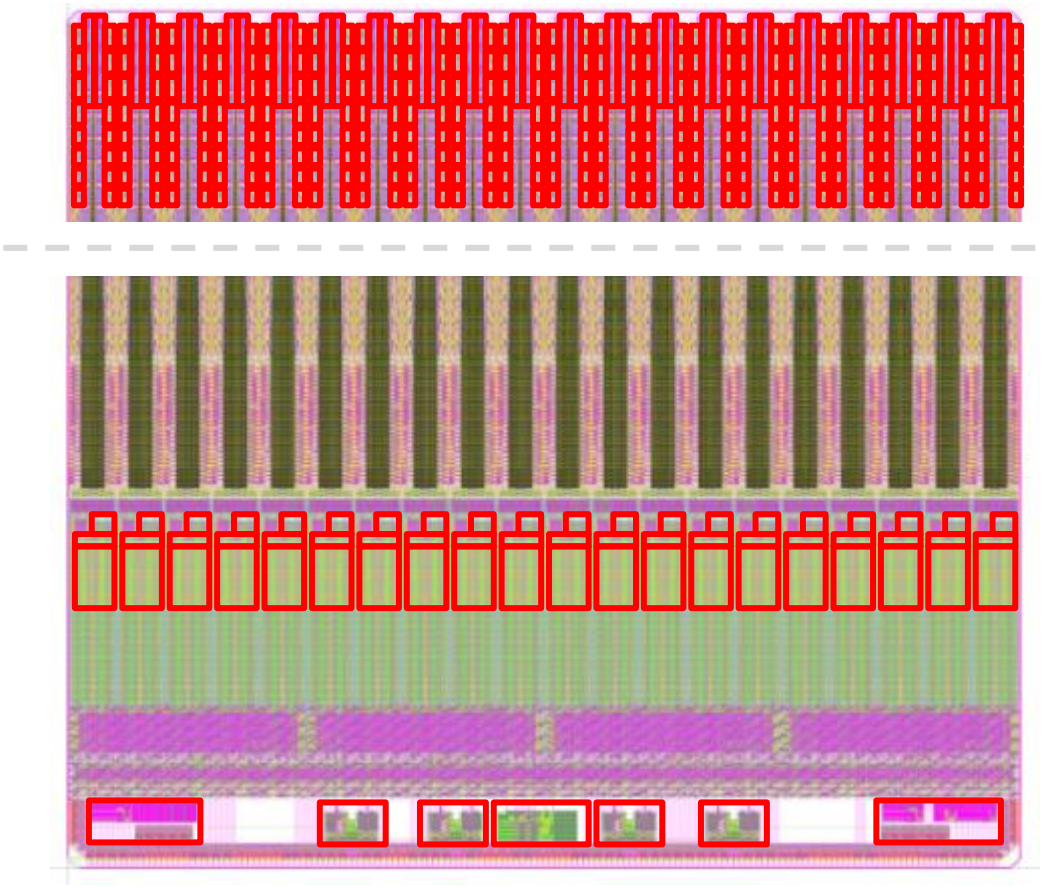
Power

- 1.2 V supplies
- Pixels
  - 650 mW (450 mW/cm^2)
- Periphery
  - 2000 mW (2500 mW/cm^2)



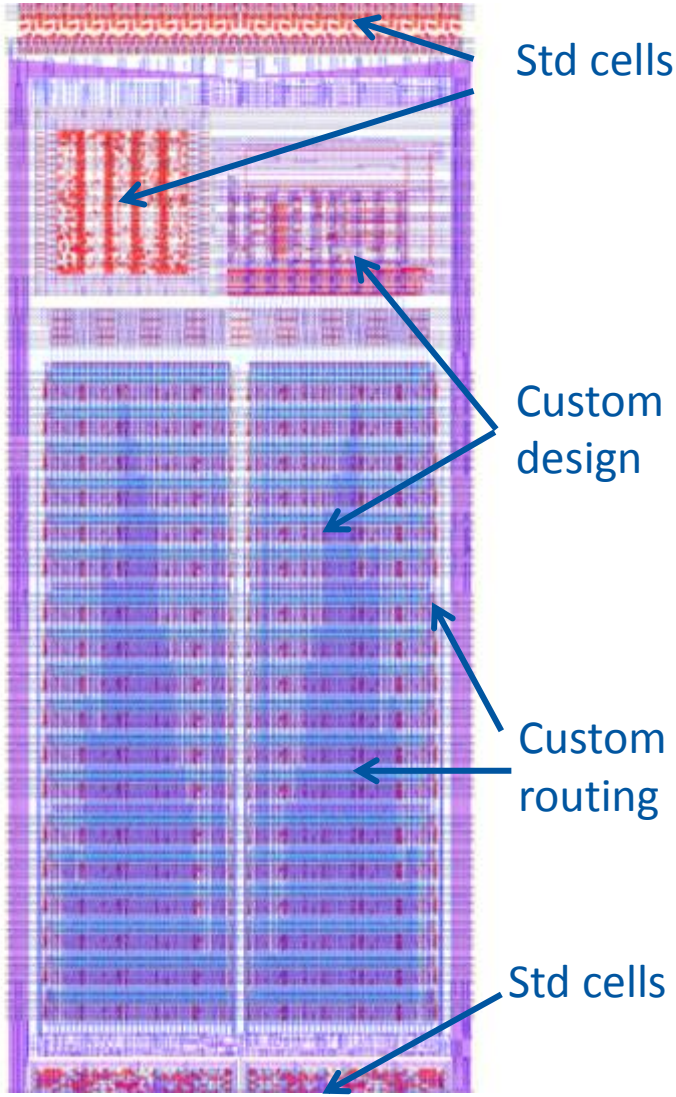
Noise and signal integrity

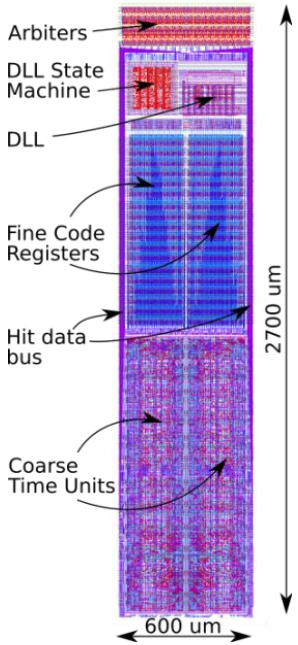
- No switching in matrix
- Triple-wells
- Substrate isolation
- Shielded routing



Congestion and TDC uniformity

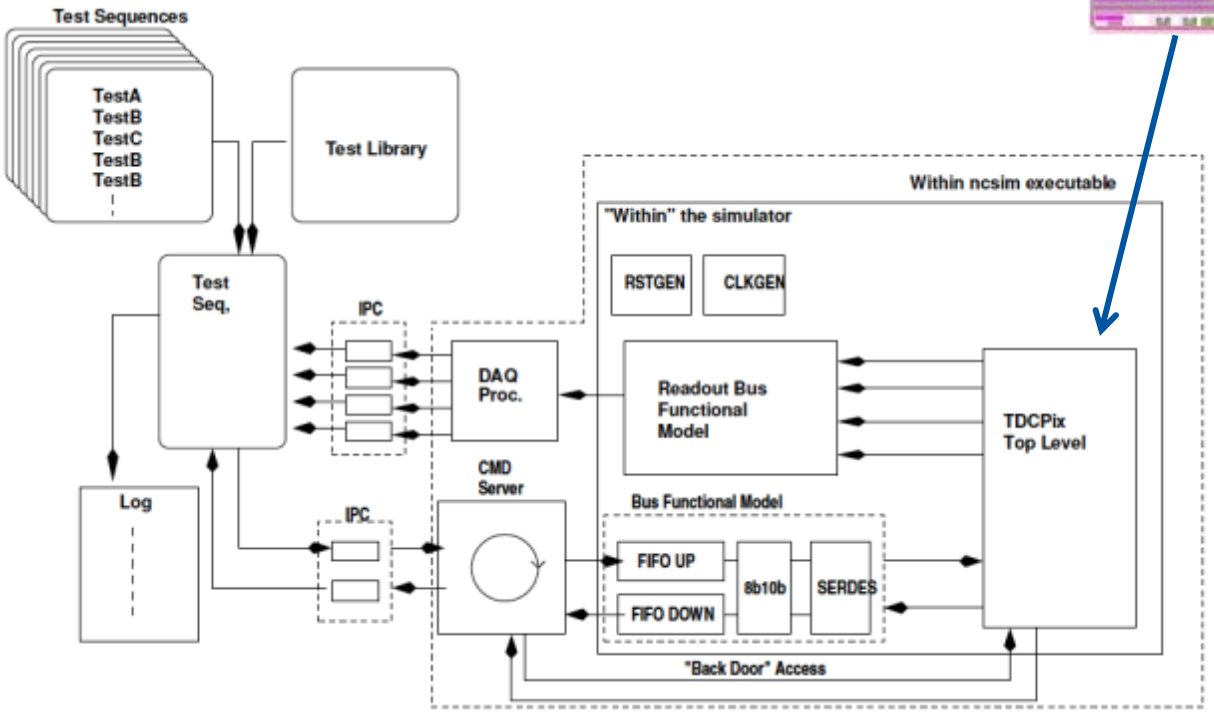
- Congestion
  - Careful floor planning
- Uniformity of TDC channels
  - Custom design, placement, routing



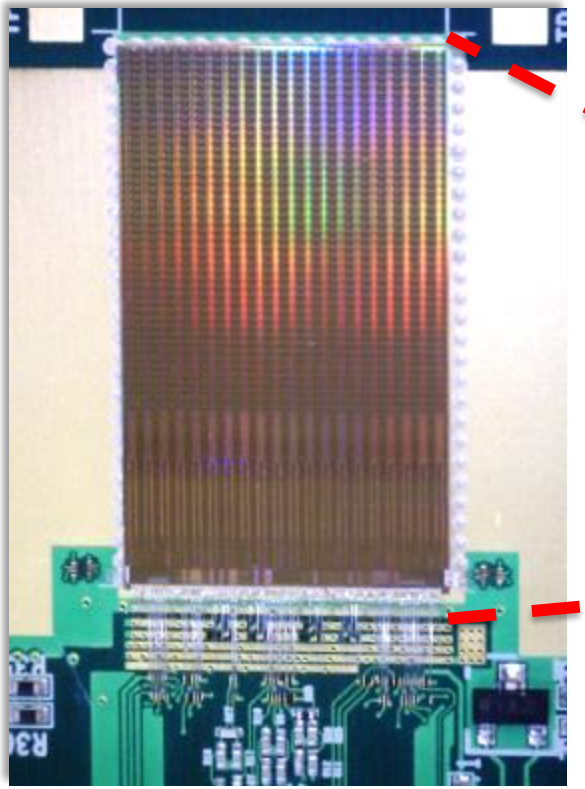


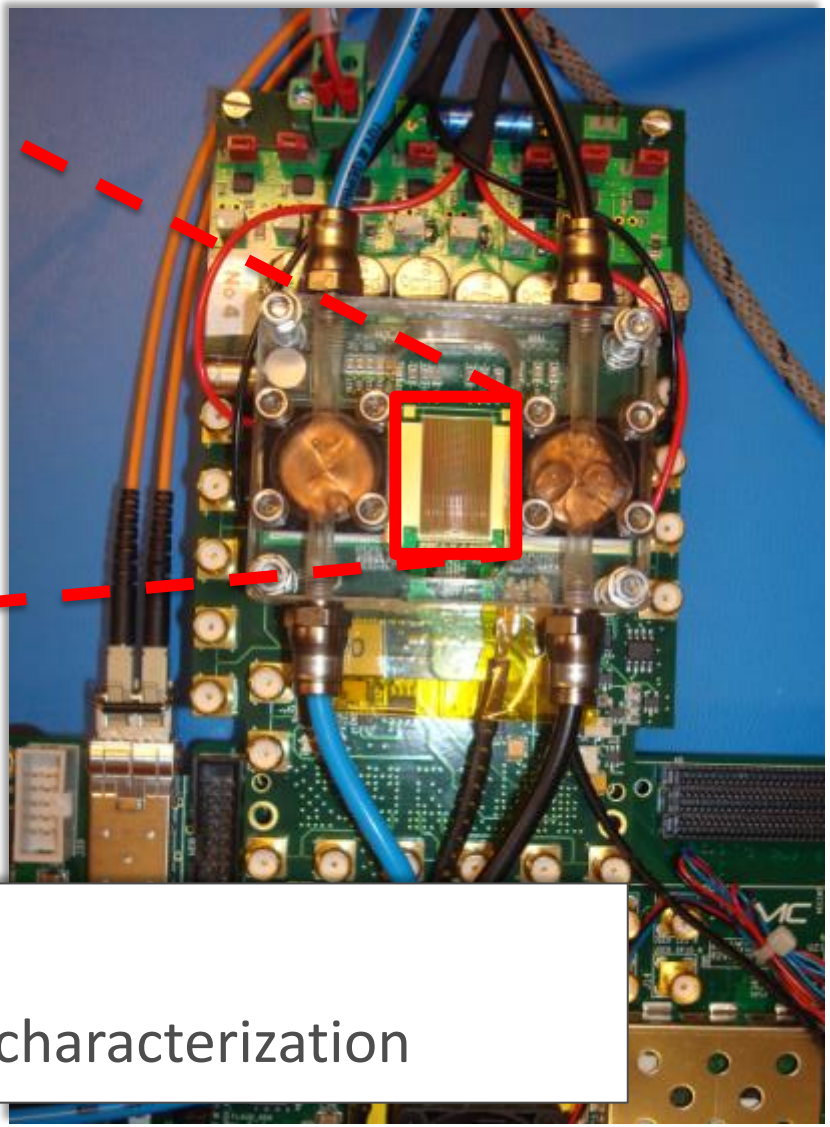
Sign-off verification

- Full chip simulations
  - Complex and large design
- Physical verification



Laboratory tests





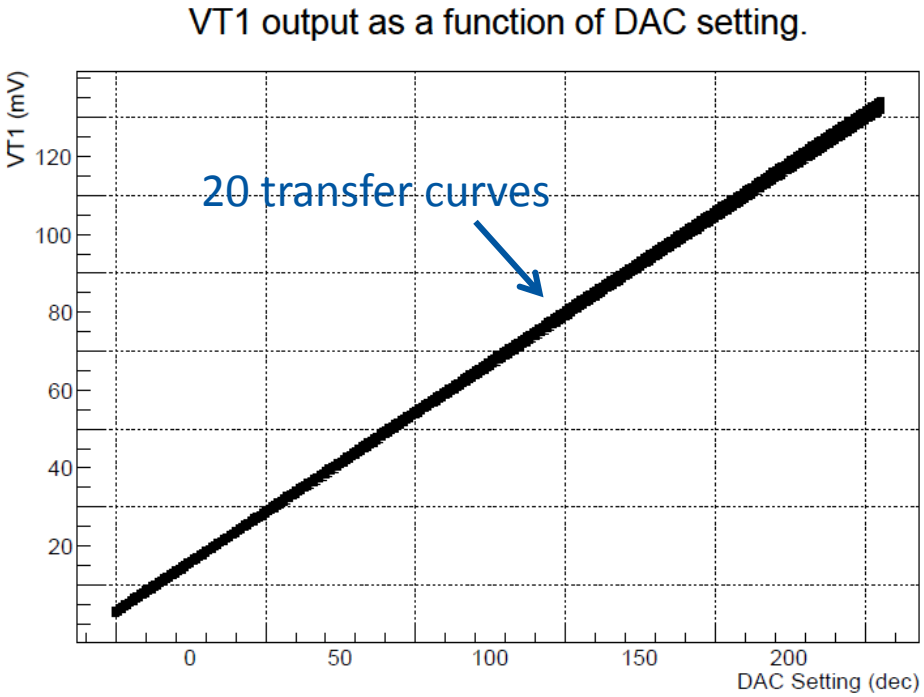
- 5 chips bonded for tests
- 1 chip under systematic characterization

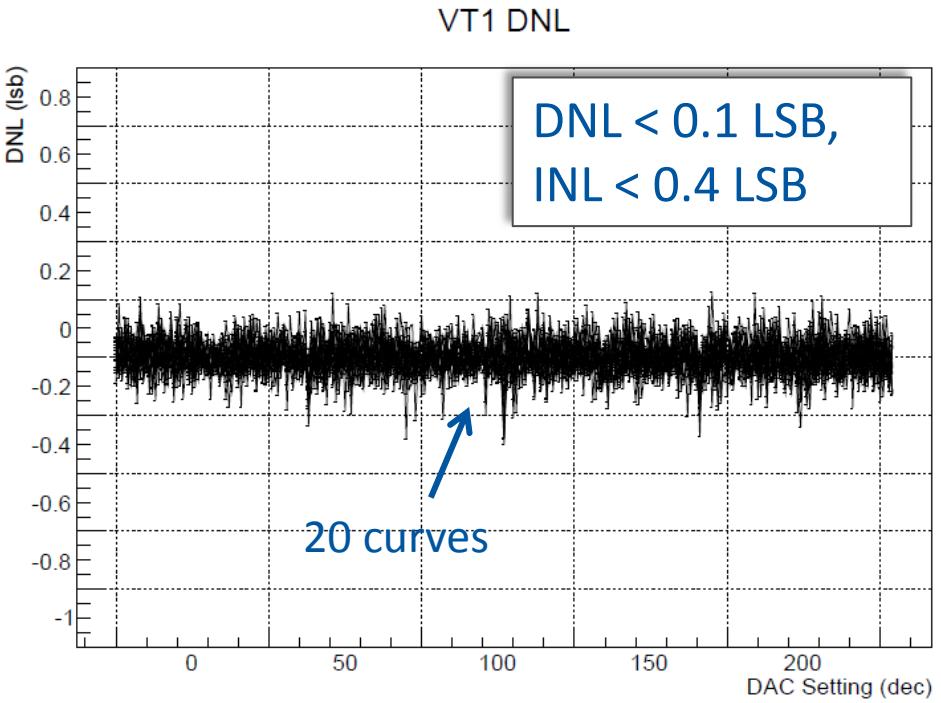
Functionalities

Block	Status	Remarks
Configuration circuits	**WORKING**	In all 5 chips
PLL	**WORKING**	3.2 GHz
Serializers	**WORKING**	3.2 Gb/s
Bandgaps	**WORKING**	
Temperature Interlock	**WORKING**	
Column bias DACs	**WORKING**	**200** DACs
In-pixel threshold trimming	**WORKING**	**1800** DACs

DACs

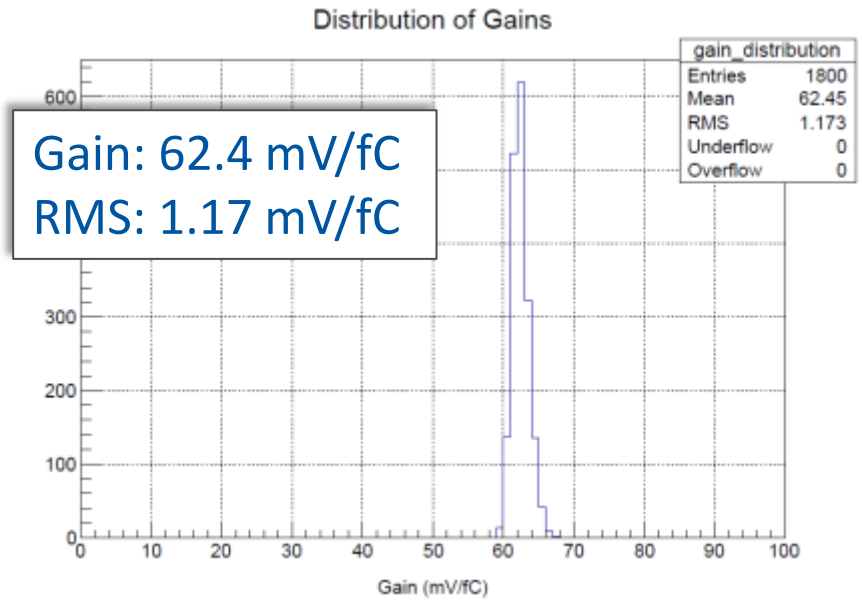
- 200 DACs
  - 10*20 Column pair bias blocks

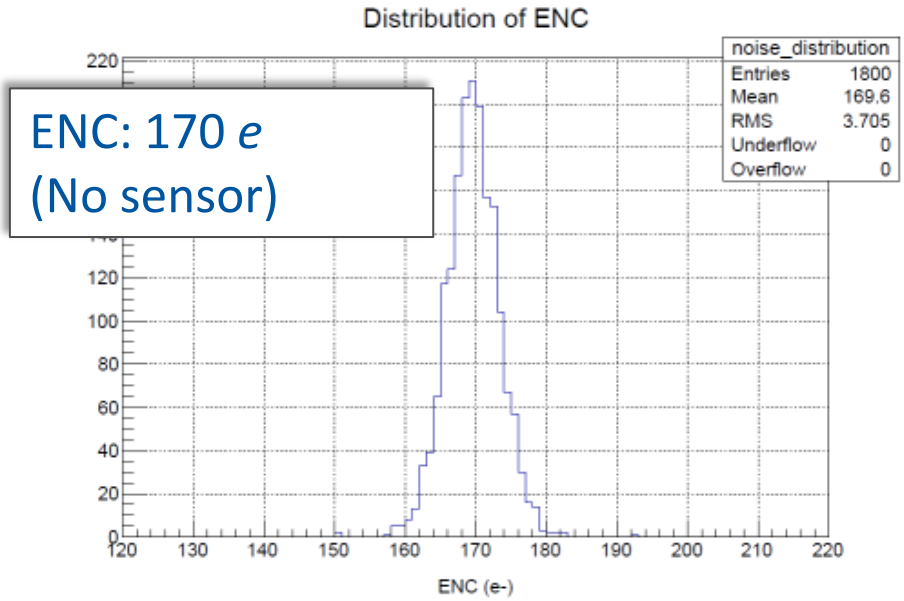




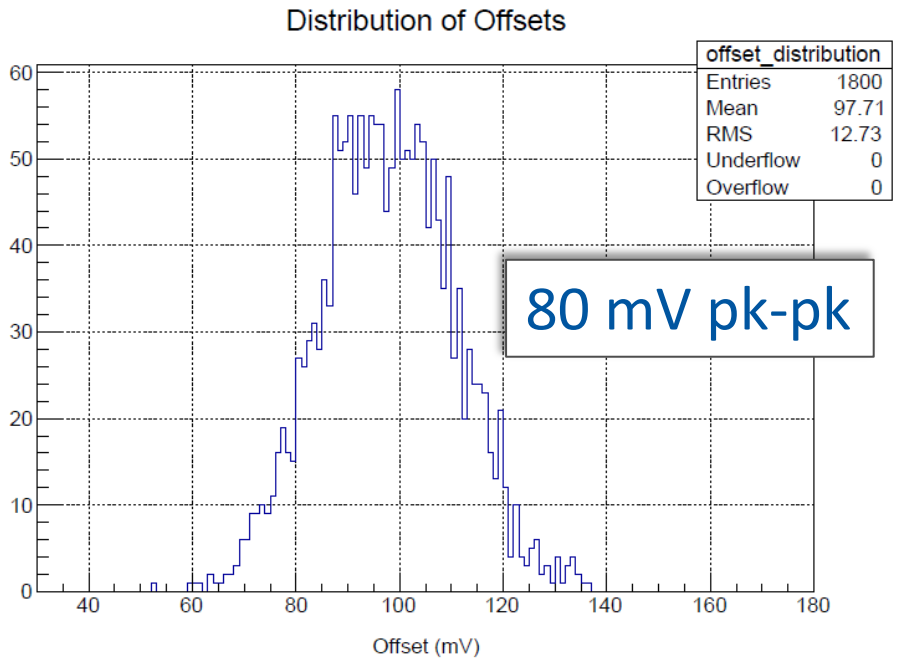
Pixel front-end

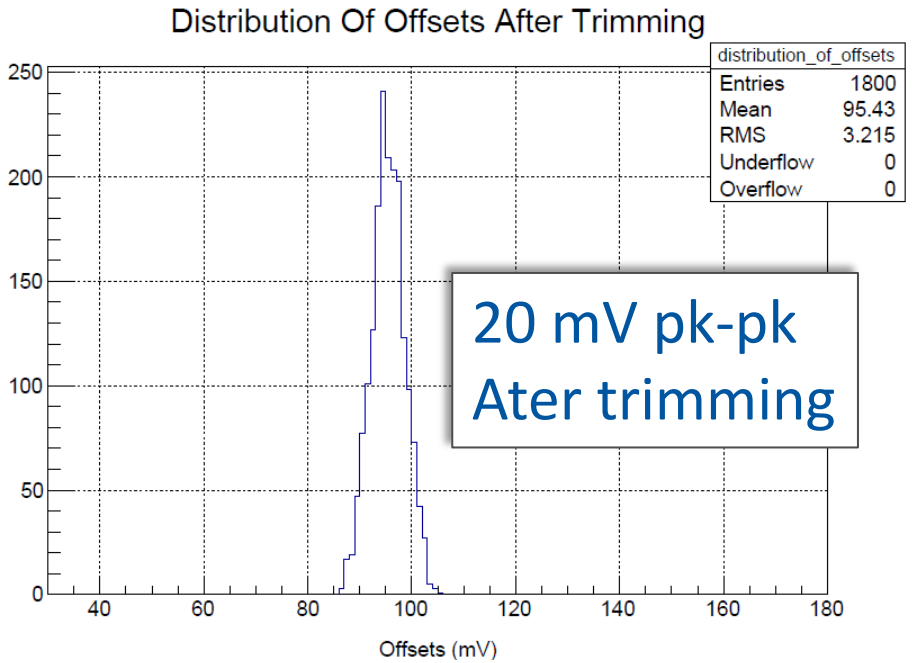
- All 1800 pixels functional
  - Injection of charge pulses
  - Threshold scans
- Gain and ENC
  - Good agreement with simulations





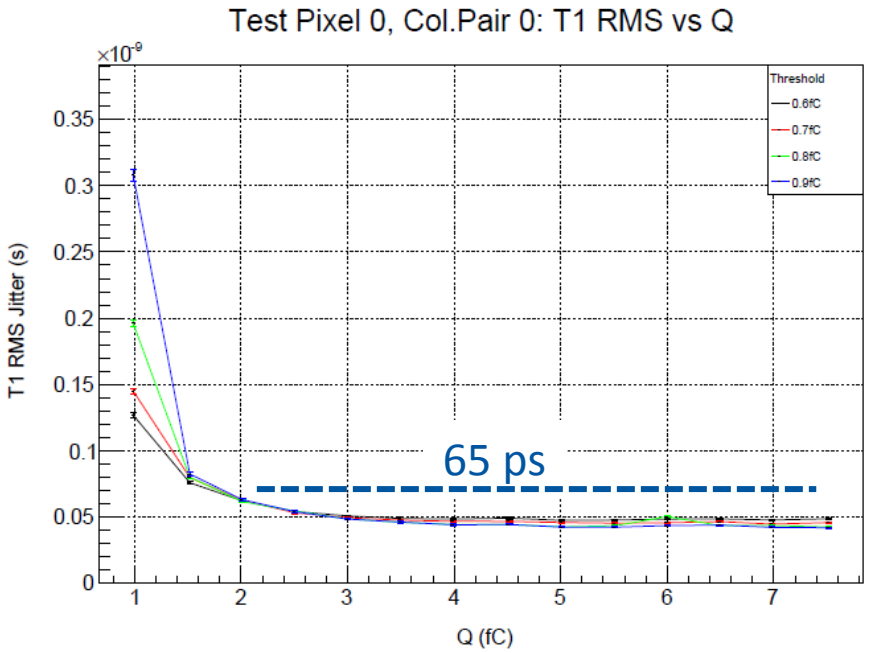
Threshold offsets

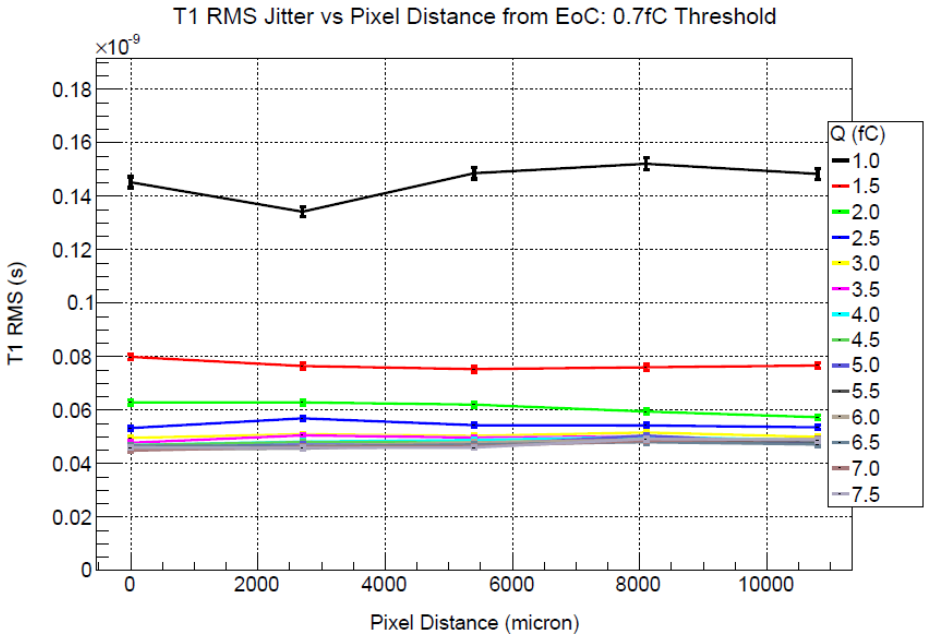




Hit transmission timing performance

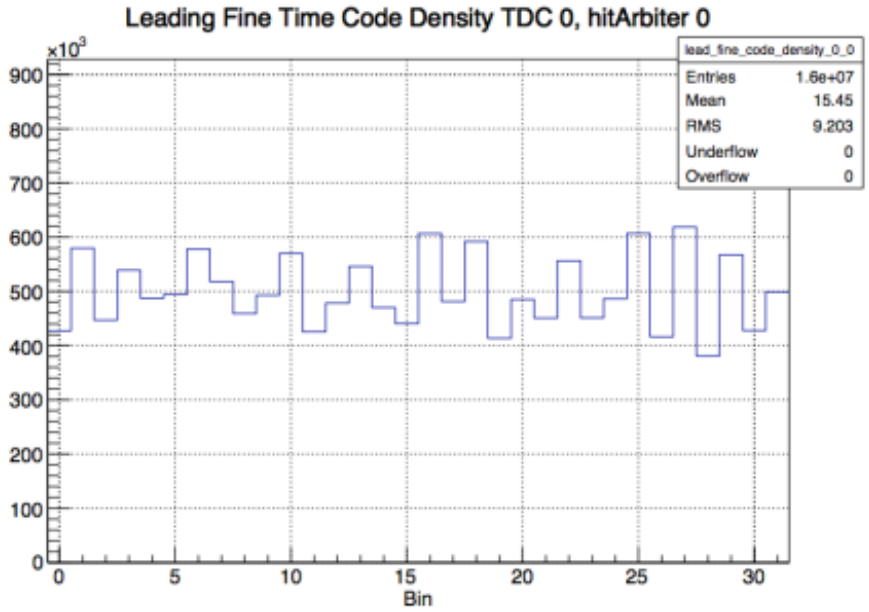
- Pixel -> TX line -> Arbiter -> Test output
  - TDC not included
- Less than 65 ps RMS
  - Q > 2 fC
- No dependence on position in the column

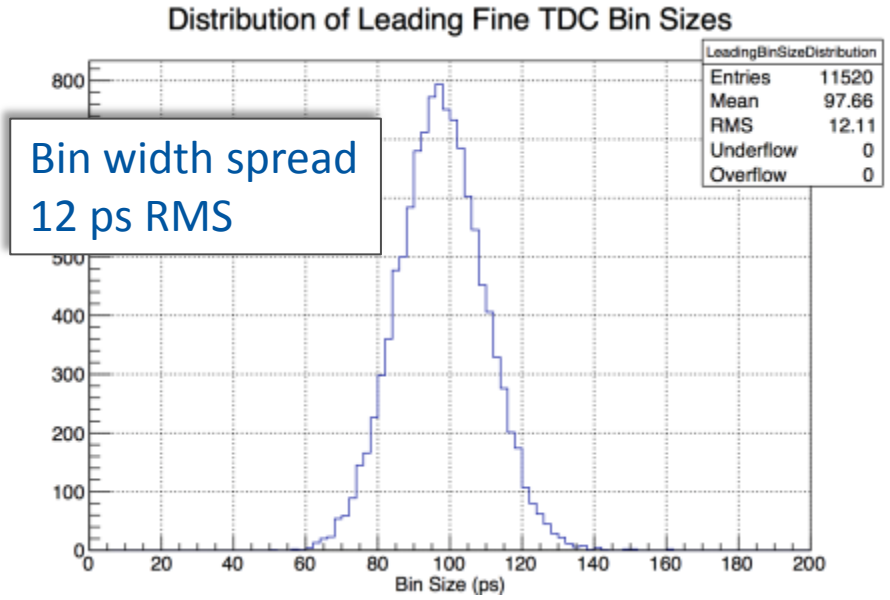




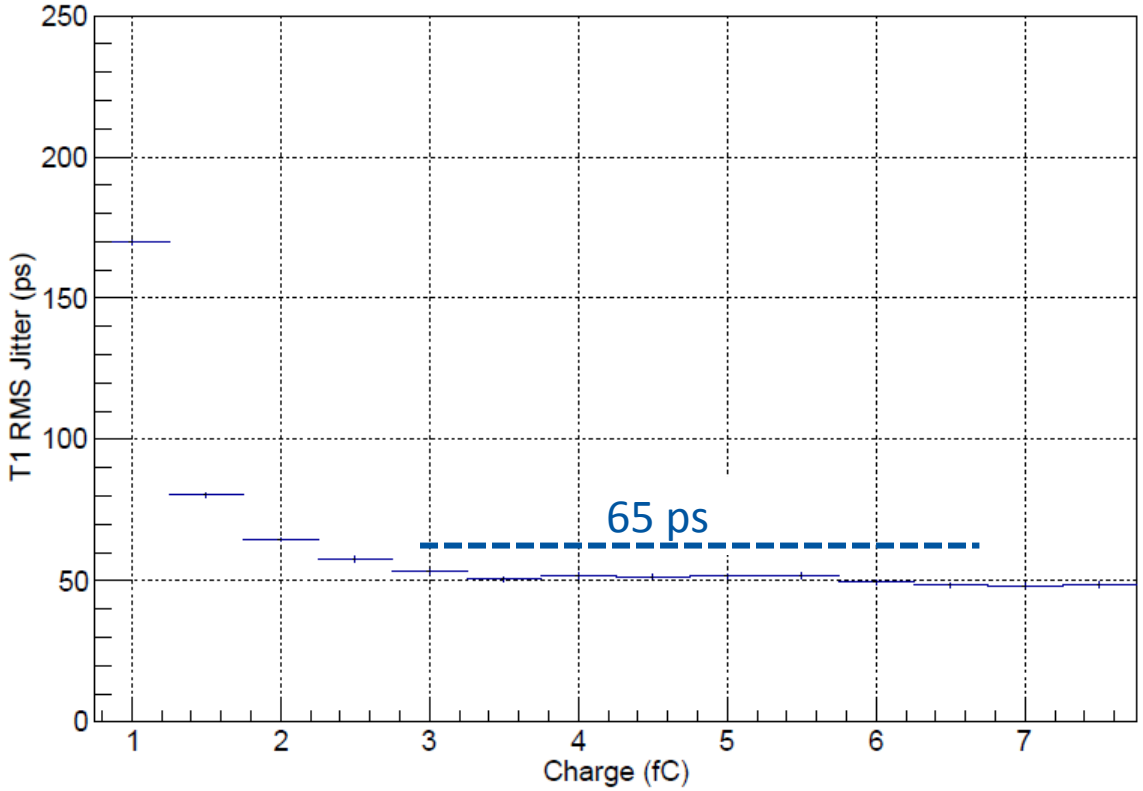
TDC linearity

- TDC test input
  - External test pulse
  - No pixels involved
  - Random timing
- DNL and INL < 0.4 LSB



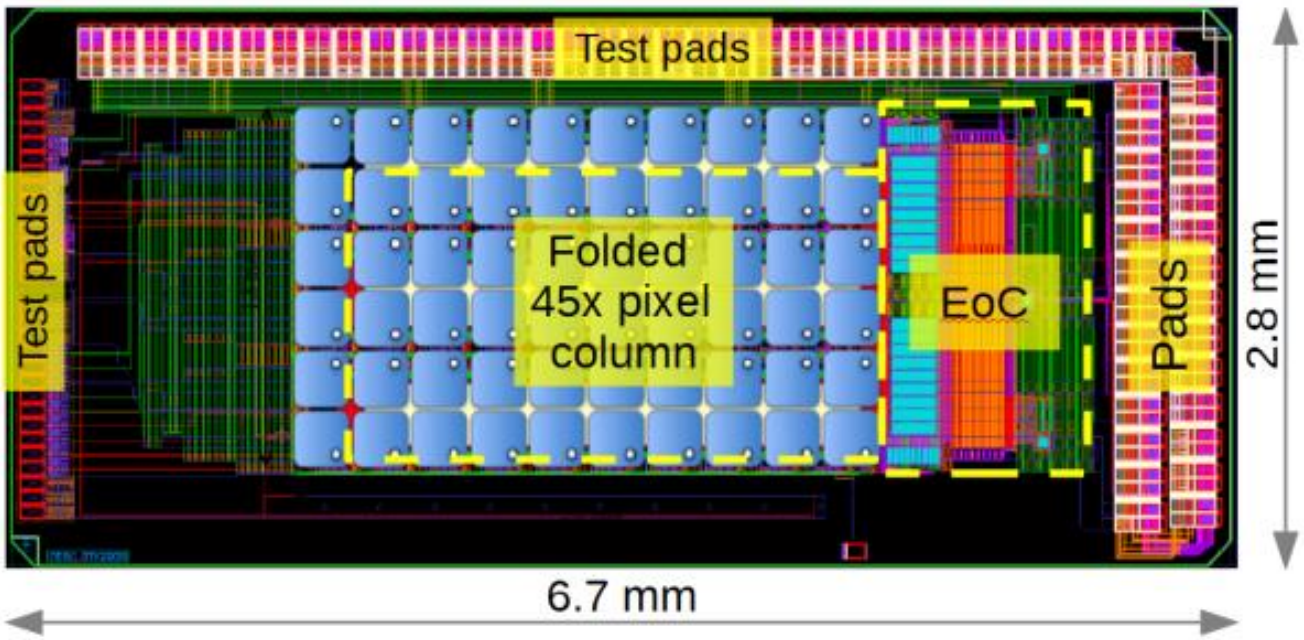


Full chain timing performance

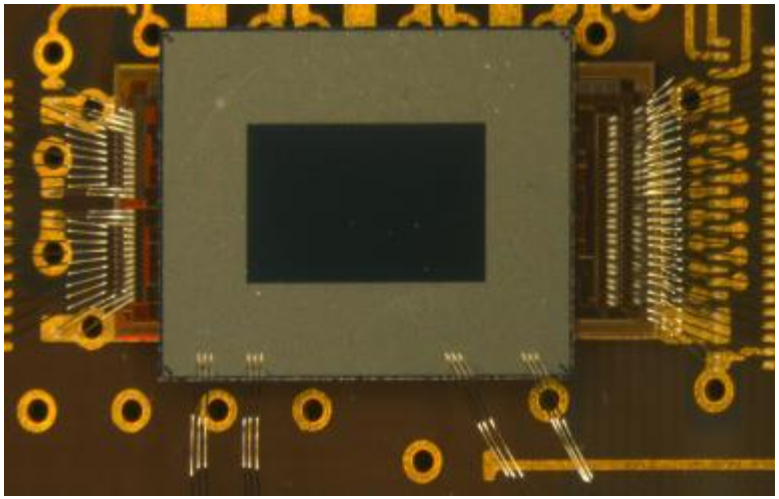


- Pixel -> TDC -> Output
  - Scan over the full clock period for each charge
  - Timing performance dictated by pixel discriminator output jitter

Measurements with prototype

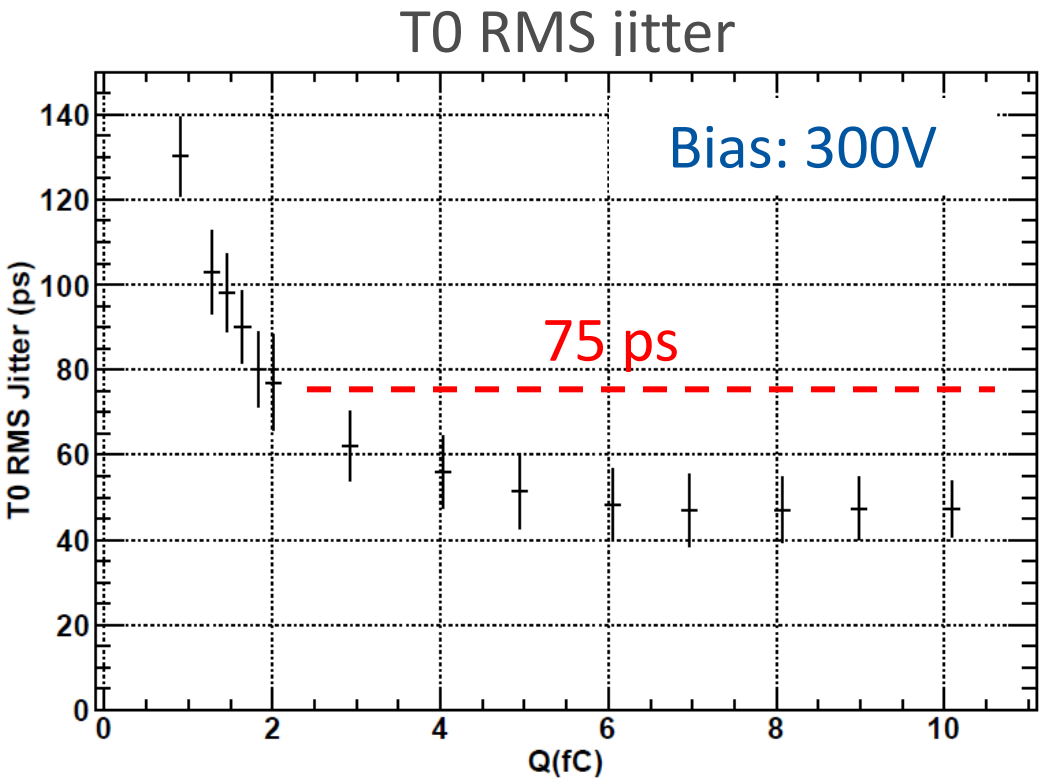


- Hybrid assembly prototype
  - 200 μm thick, p in n pixel sensor

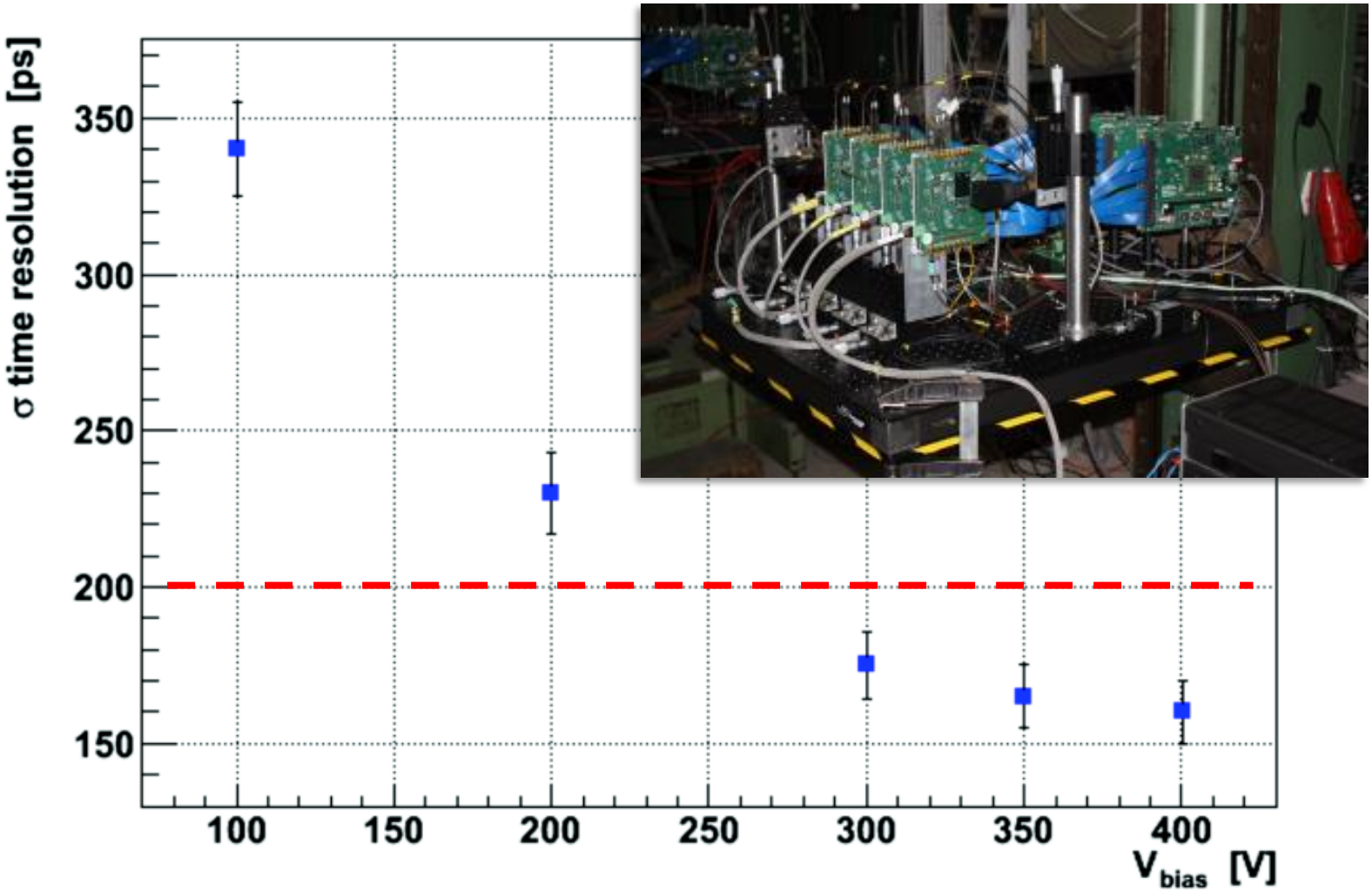


Full chain timing performance (prototype)

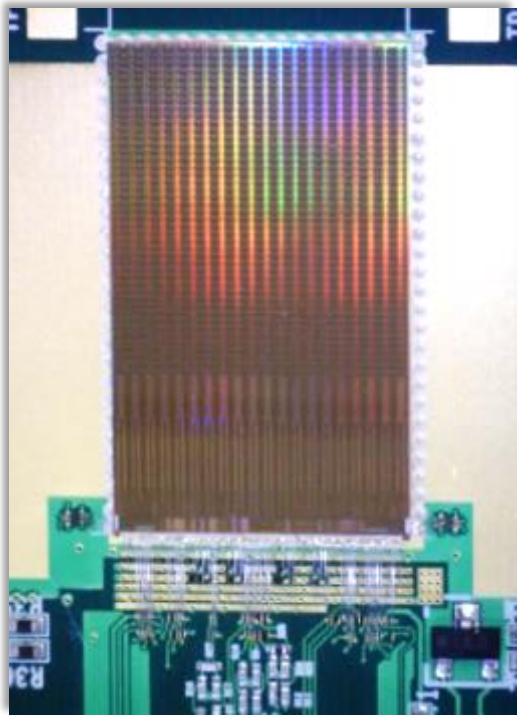
- Laser pulses
  - Sensor Bonded
- Front-end and discriminator
  - Jitter < 75 ps RMS
- TDC
  - Jitter: < 10 ps RMS
  - Resolution: 40 ps @ 320 MHz
- T_0 < 75 ps RMS
  - Including Time walk Compensation
  - Bias 300 V, Q > 2 fC, C_{det} = 250 fF



Timing particles in beam test

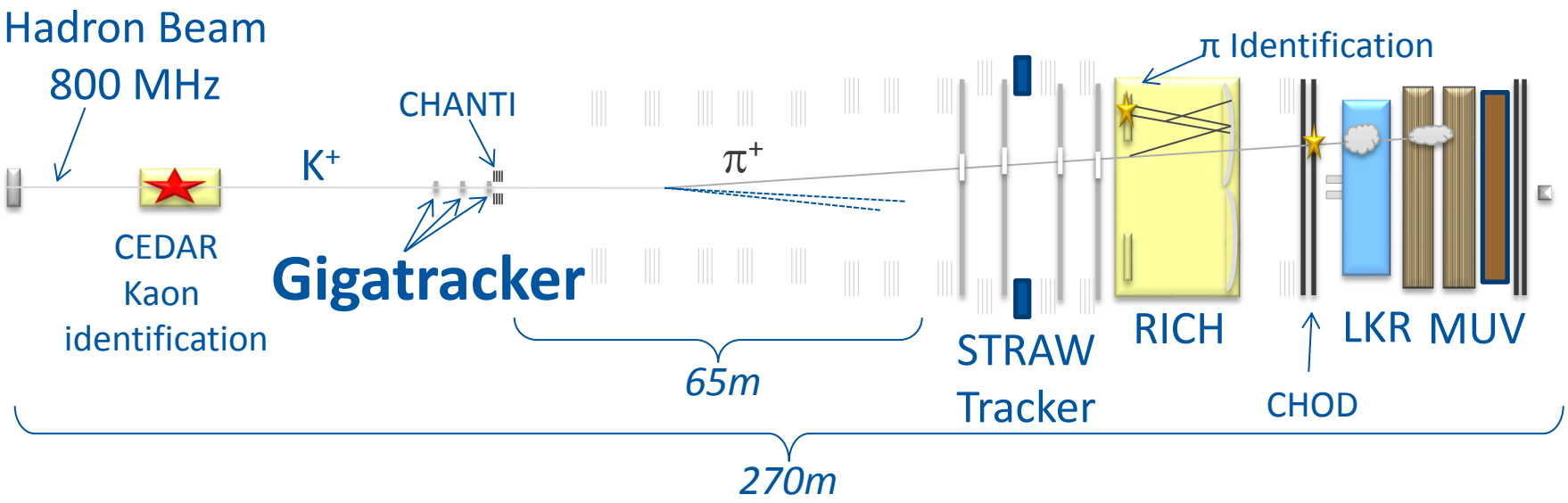


Summary



- TDCpix hybrid pixels readout ASIC
  - 45×40 pixels of 300×300 µm^2
    - Nominal input range 0.5-10 fC / 3100-62500 e
  - Hit rate
    - 0.8 MHz/mm^2, 130 MHits/s
  - Trigger-less architecture
    - 4 × 3.2 Gb/s links
- First laboratory tests
  - No bugs detected
  - Analog and TDCs performance as simulated and very close to prototype
  - No performance changes due to large scale integration
- Timing performance with particles < 200 ps RMS
  - Measured with prototype chip

Spare slides


Hadron Beam
800 MHz
CEDAR
Kaon
identification
K+
CHANTI
Gigatracker
π+
65m
π Identification
STRAW
Tracker
RICH
CHOD
LKR
MUV
270m

Full list of requirements

Parameter	Requirement
Number of pixels per chip	1800 = 45 x 40
Size of pixels	300 μm x 300 μm
Active area per chip	12 mm x 13.5 mm = 162 mm^2
ASIC design time binning	100 ps
Sensor size	27.0 mm x 60.8 mm = 162 mm^2
Thickness of sensor	200 μm
Type of sensor	p in n
Thickness of read-out chip	100 μm
Dynamic input range	0.7 - 10 fC, 5000 - 60000 electrons
Design particle rate per chip	105 MHz
Rate of center pixel	114 kHz
Rate of center column	2.7 MHz or 0.66 MHz/mm^2
Average rate per pixel	58 kHz
Max. dead time	1 % (2 % in beam center)
Data transfer rate per chip	6 Gbit/s
Design transfer rate per chip	12.8 Gbit/s
Total dose in 1 year	6 x 10^4 Gy
Neutron flux in 100 days	2 x 10^{14} 1 MeV neutron equivalent cm^{-2}
Max. Material budget/thickness	0.5 % X_0 per station
Operating temperature	-20 to 5 °C
Operating vacuum	10^{-6} bar

Radiation

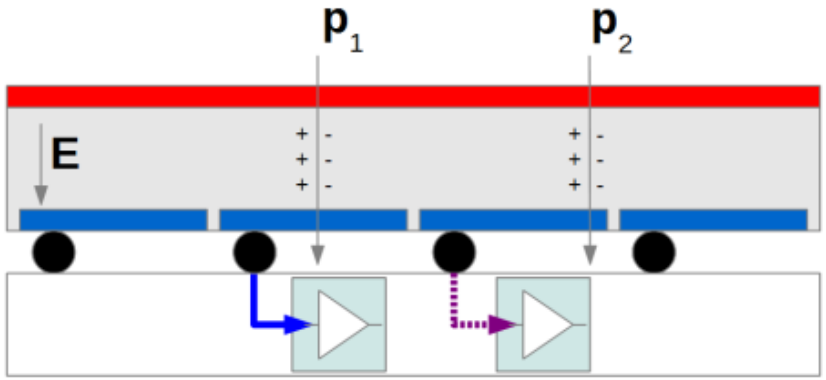
- 2×10^{14} 1 MeV n_{eq} cm^{-2} / year
- 6×10^{4} Gy / year
  - 1 year = 100 days beam time
- Fluence and dose gradient
- Sensor cooling
- SEU protection
  - Triple Modular Redundancy for all configuration bits and state machines
  - Data FIFOs not protected
    - Permanence on chip ~10ms

Timing resolution limit of sensor

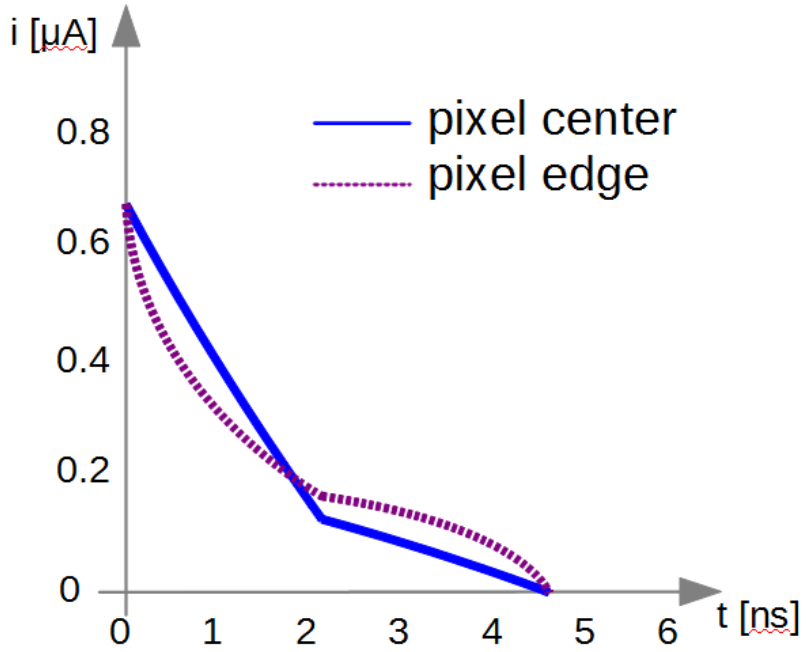
Timing resolution
- Laser: 75 ps RMS
- Test beam: 175 ps RMS

Random fluctuations of input current signal shape
- Position of track hit in pixel
- Charge straggling

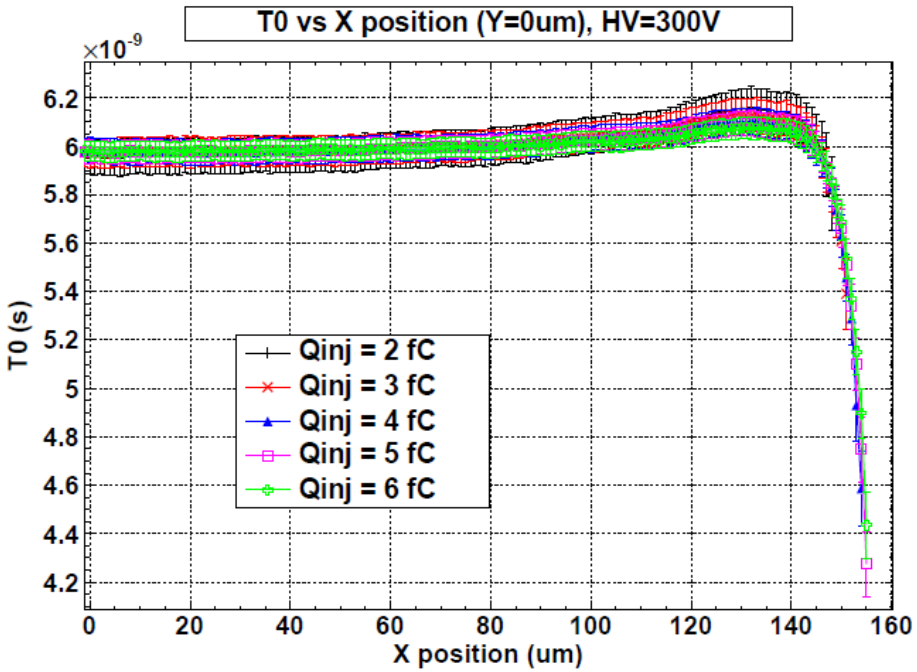
- Position scan with laser
  85 ps RMS
- Charge straggling
  > 60 ps RMS

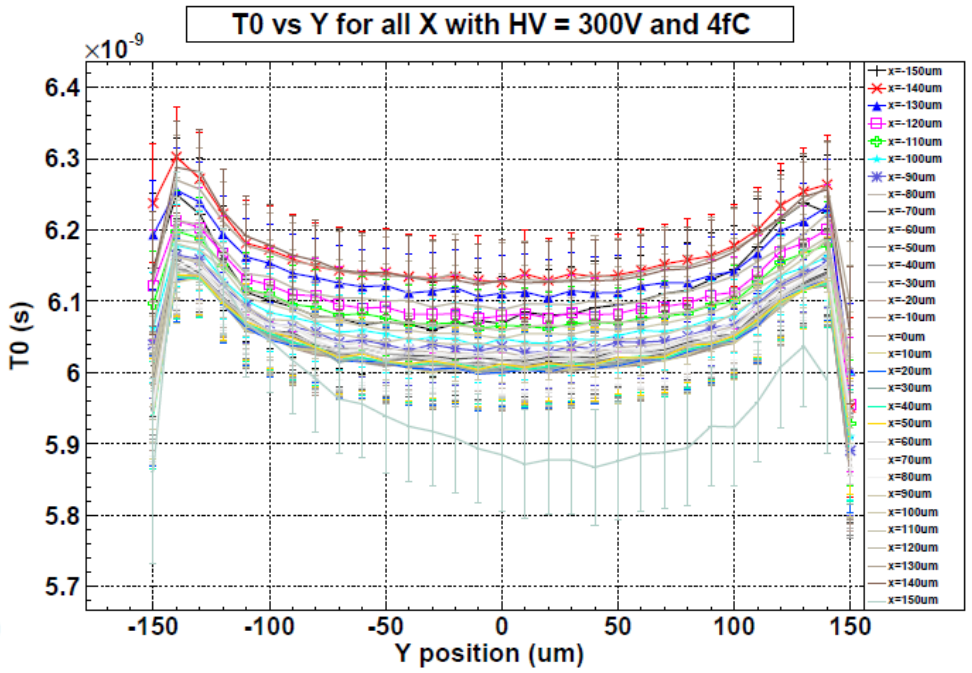


Sensor current pulses

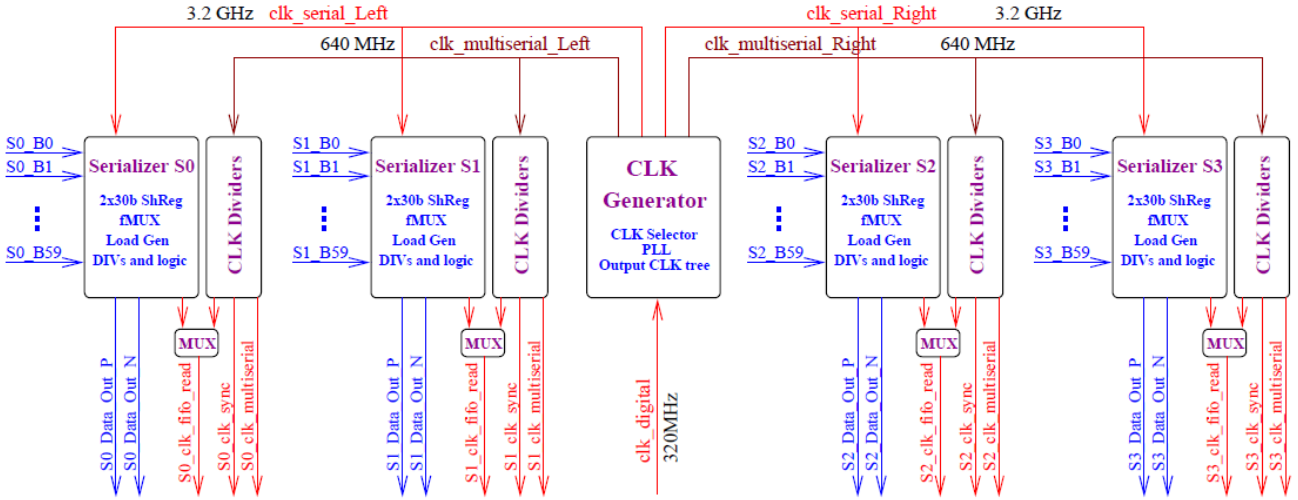


Pixel scans with laser



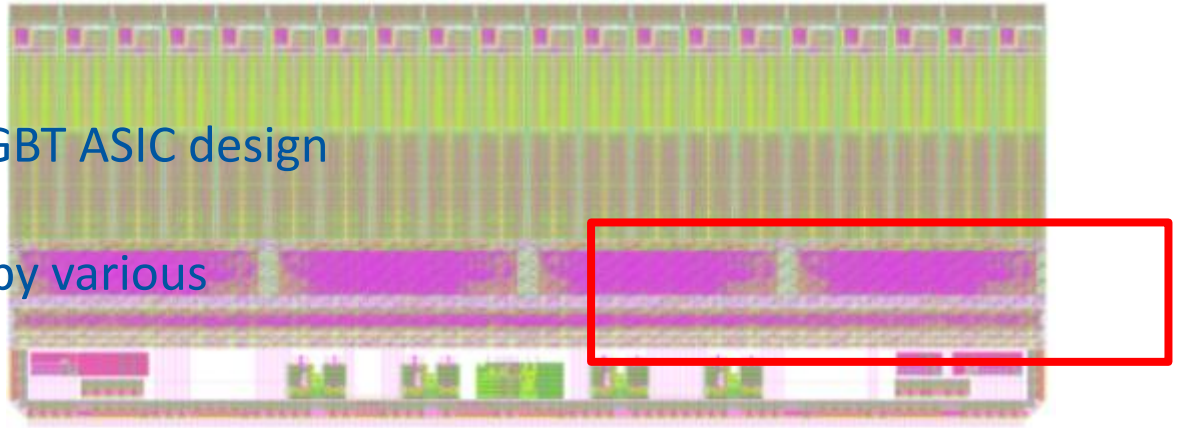


CLK generator, PLL, Serializers



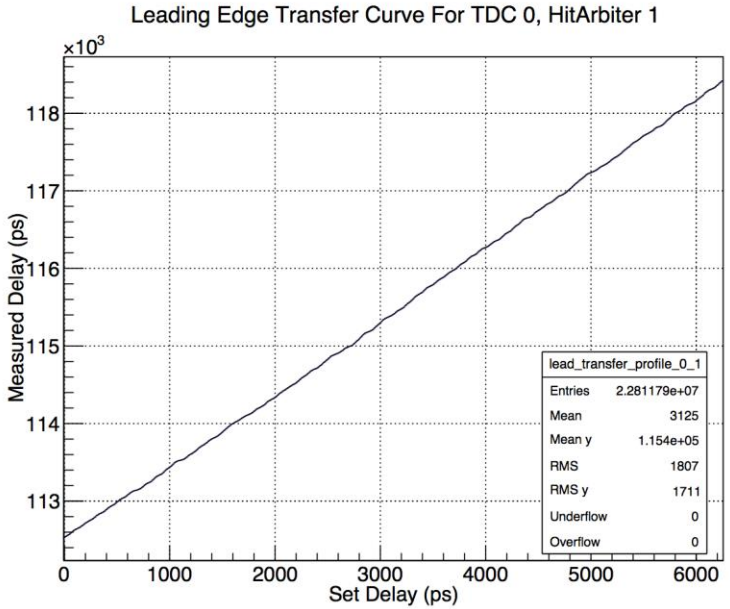
Adapted from GBT ASIC design

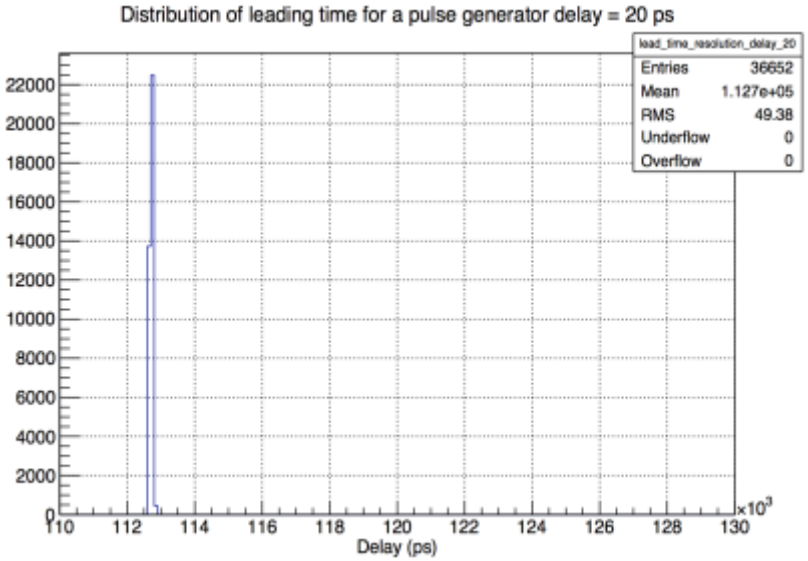
SET mitigation by various techniques



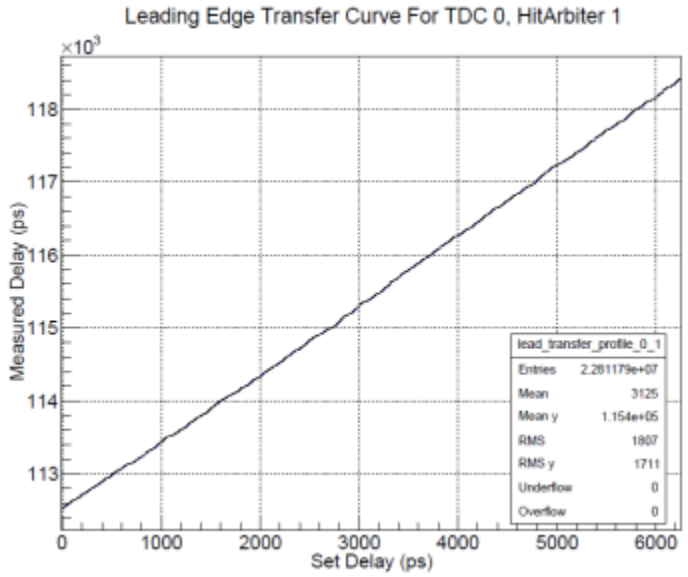
TDCpix TDC jitter

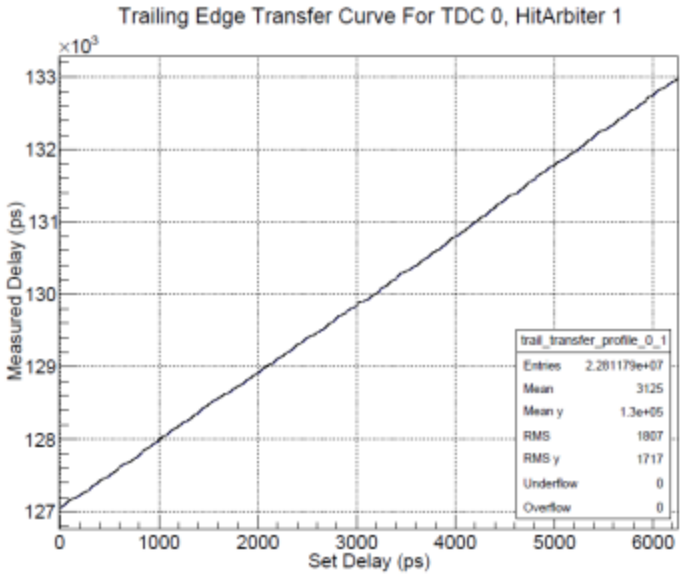
- External pulse source
  - Jitter: 30 ps RMS
  - Scan of 10 ps steps
- 50 ps RMS
  - Include on chip pulse distribution
  - Upper limit to TDC intrinsic jitter

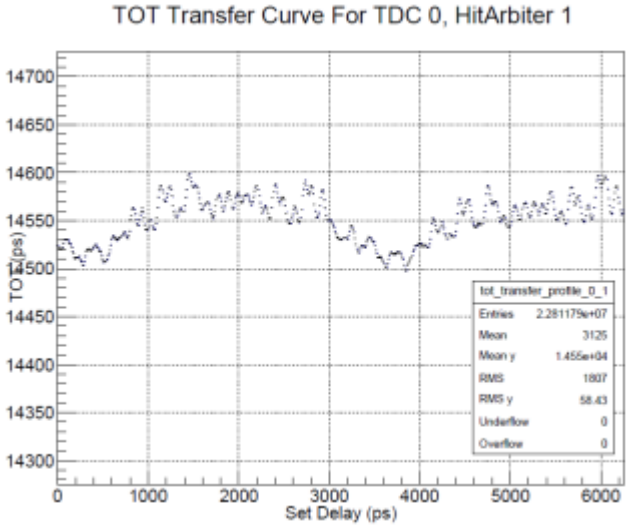




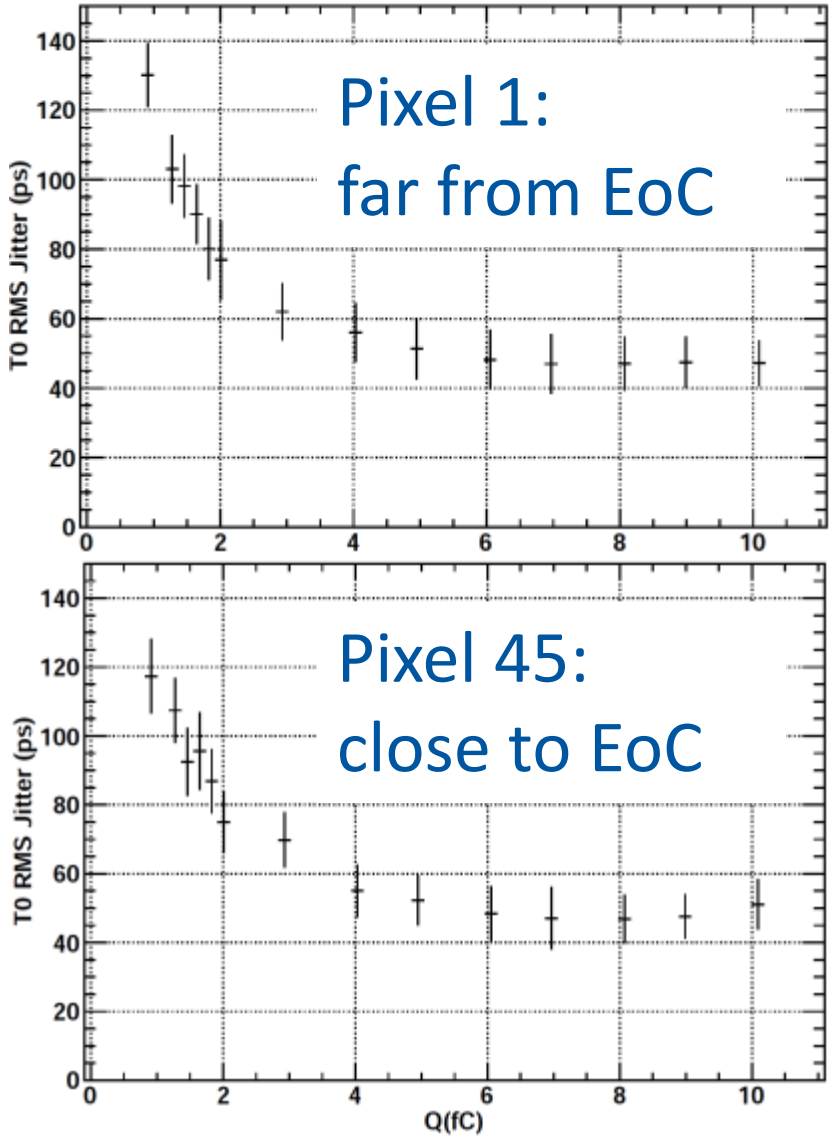
TDC jitter


Leading Edge Transfer Curve For TDC 0, HitArbiter 1
×10³
Measured Delay (ps)
Set Delay (ps)
lead_transfer_profile_0_1
Entries 2.281179e+07
Mean 3125
Mean y 1.154e+05
RMS 1807
RMS y 1711
Underflow 0
Overflow 0


Trailing Edge Transfer Curve For TDC 0, HitArbiter 1
×10³
Measured Delay (ps)
Set Delay (ps)
trail_transfer_profile_0_1
Entries 2.281179e+07
Mean 3125
Mean y 1.3e+05
RMS 1807
RMS y 1717
Underflow 0
Overflow 0


TOT Transfer Curve For TDC 0, HitArbiter 1
TOT (ps)
Set Delay (ps)
tot_transfer_profile_0_1
Entries 2.281179e+07
Mean 3125
Mean y 1.455e+04
RMS 1807
RMS y 58.43
Underflow 0
Overflow 0

Full chain timing performance



Data readout and data word format

- High speed serial
  - 4× 3.2 Gb/s ports with 8b/10b encoding
- Auxiliary multi-serial ports
  - 4× (4× 640 Mb/s) ports

Type (1)	Pixel address (12)	Pileup (5)	Lead coarse time (13)	Lead Fine Time (5)	ToT (7)	Trail Fine Time (5)

(48)

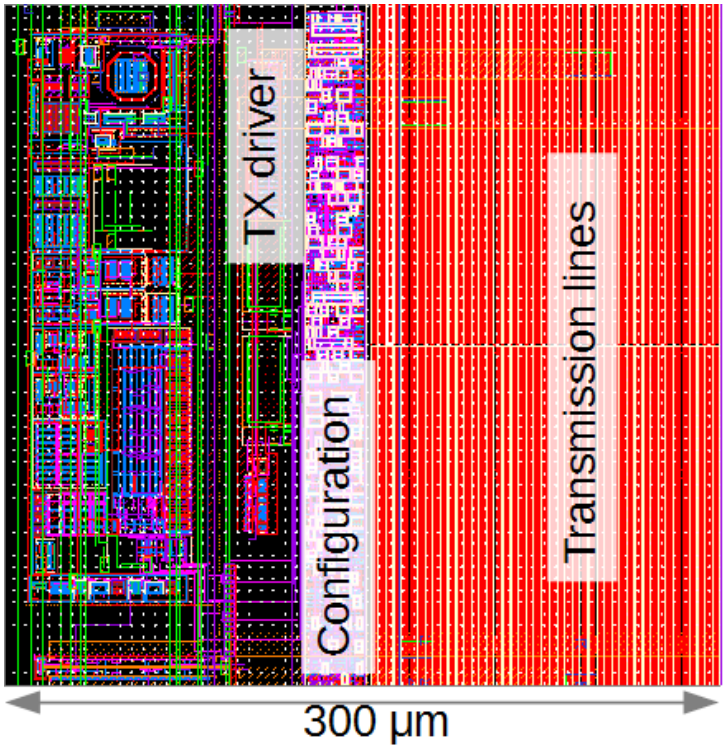
Hit losses due to collisions

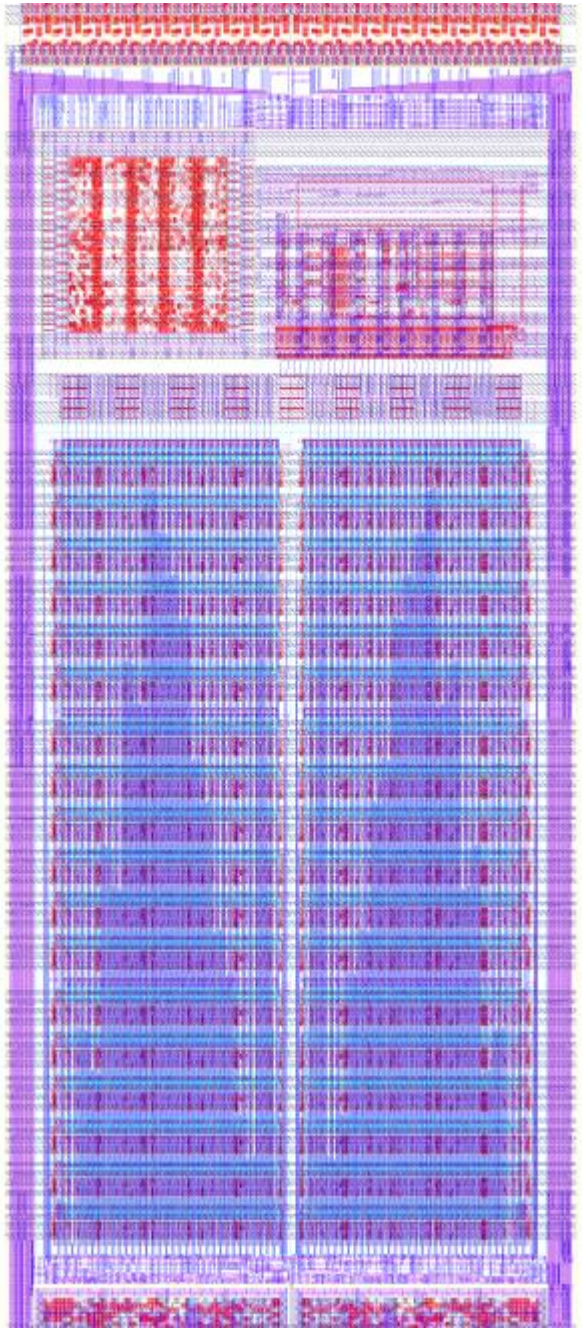
- Hit processing statistics
  - Nominal rate of pixel hits in peak rate column: 3.3 MHz
  - Simulating with **4 MHz** hit rate
  - Nominal readout frequency 320 MHz

```
#########################################################################################################
# Hit statistics report from monitor instance
# :tdc_tb(functional):inst_tdc_mon@
# and process :tdc_tb(functional):inst_tdc_mon@tdc_mon(behavioural):p_col0_datamon:
#########################################################################################################
# Clk Period   3.125 ns
# Mean interval between hits 250 ns
#########################################################################################################
# Group # Hits in      # Hits out     # Pileup       # Pileup cnts  # Matched      # Unmatched    # (
#########################################################################################################
8       2604           2583           19             19             2583           2              0
7       2427           2410           15             14             2410           2              0
6       2394           2376           18             18             2376           0              0
5       2329           2314           15             15             2314           0              0
4       2230           2214           13             13             2214           3              0
3       2147           2130           17             17             2130           0              0
2       2028           2012           16             15             2012           0              0
1       1946           1934           11             10             1934           1              0
0       1866           1856           10             10             1856           0              0
#########################################################################################################
TOTAL   19971          19829          134            131            19829          8              0
#########################################################################################################
```

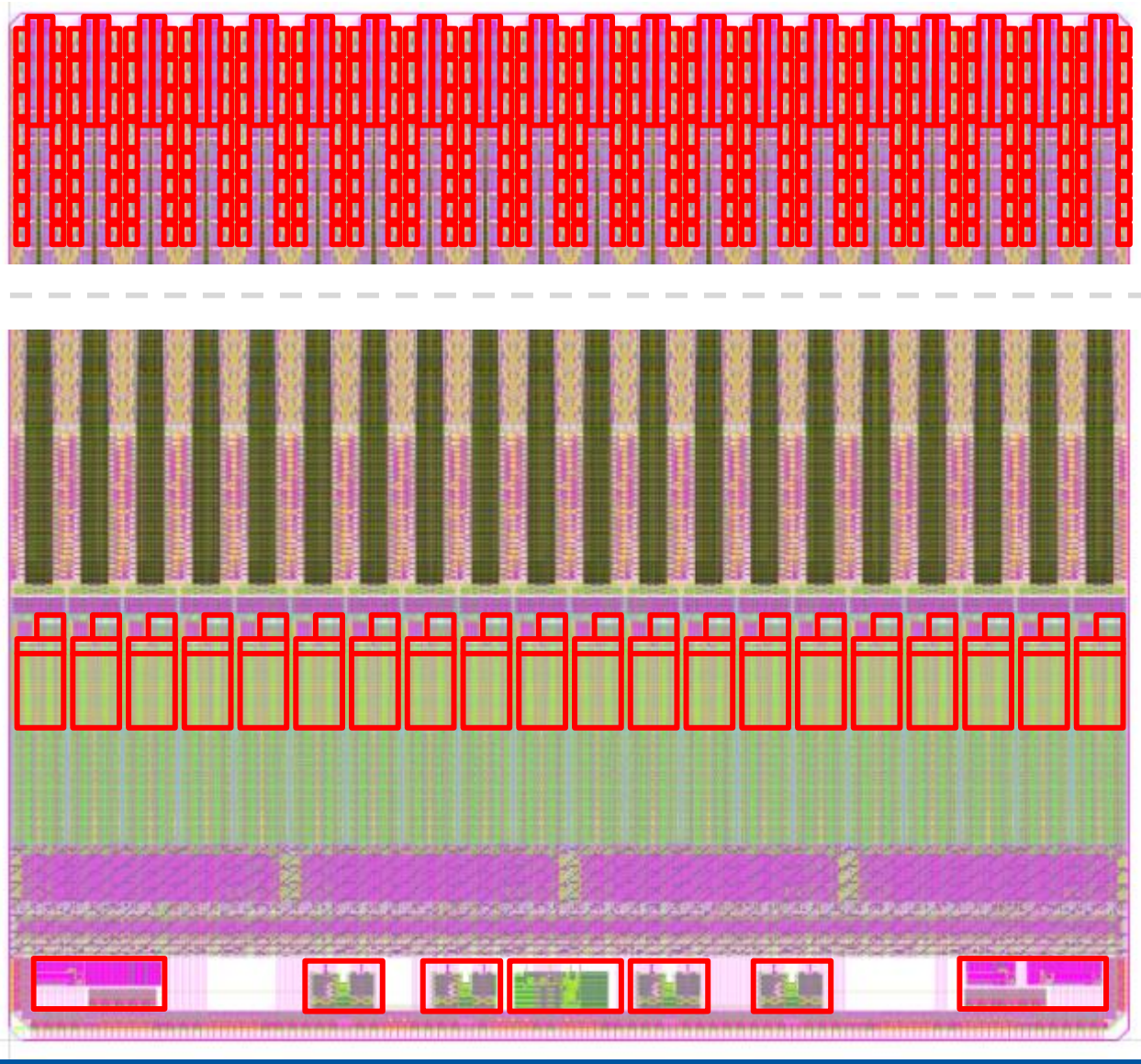
Challenges

- Noise mitigation and signal integrity
  - No digital activity in the matrix
  - Triple-wells, substrate islands separated by low doped regions
  - Routing with shielding
- Congestion
  - Careful floor-planning
- Uniformity of TDC bins, channels, skews
  - Custom design, placement, routing of critical blocks
- Functional and physical verification
  - Complex and large design
  - Mixed signal


TX driver
Configuration
Transmission lines
300 µm

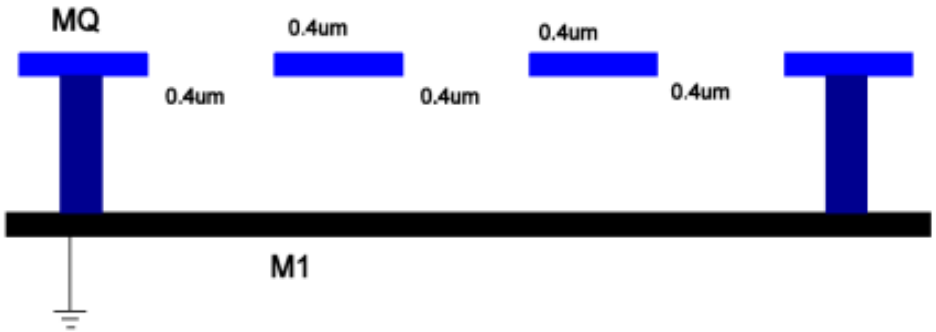


Substrate separation



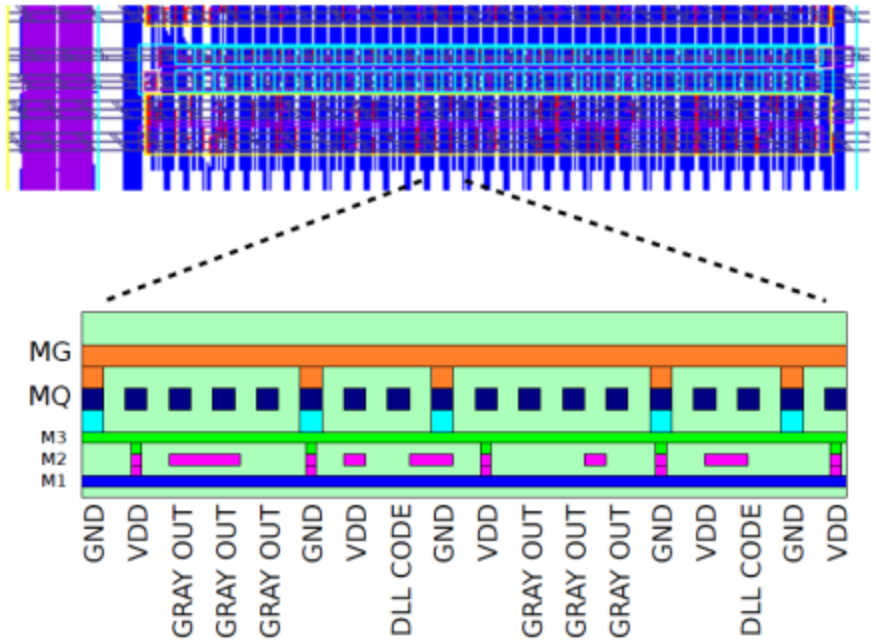
Signal integrity

Differential line from pixels to EoC
15 mm, 3ns delay, R=1.3 kΩ



Schematic cross-section of wiring of time stamp registers banks

DLL code traces shielded by power/gnd traces



Power estimates

NOMINAL CONDITIONS

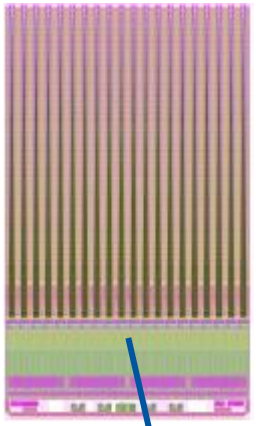
Supply voltage	1.2 V	Note: at cell inputs
Temp	25 C	
Main clk freq	320 MHz	

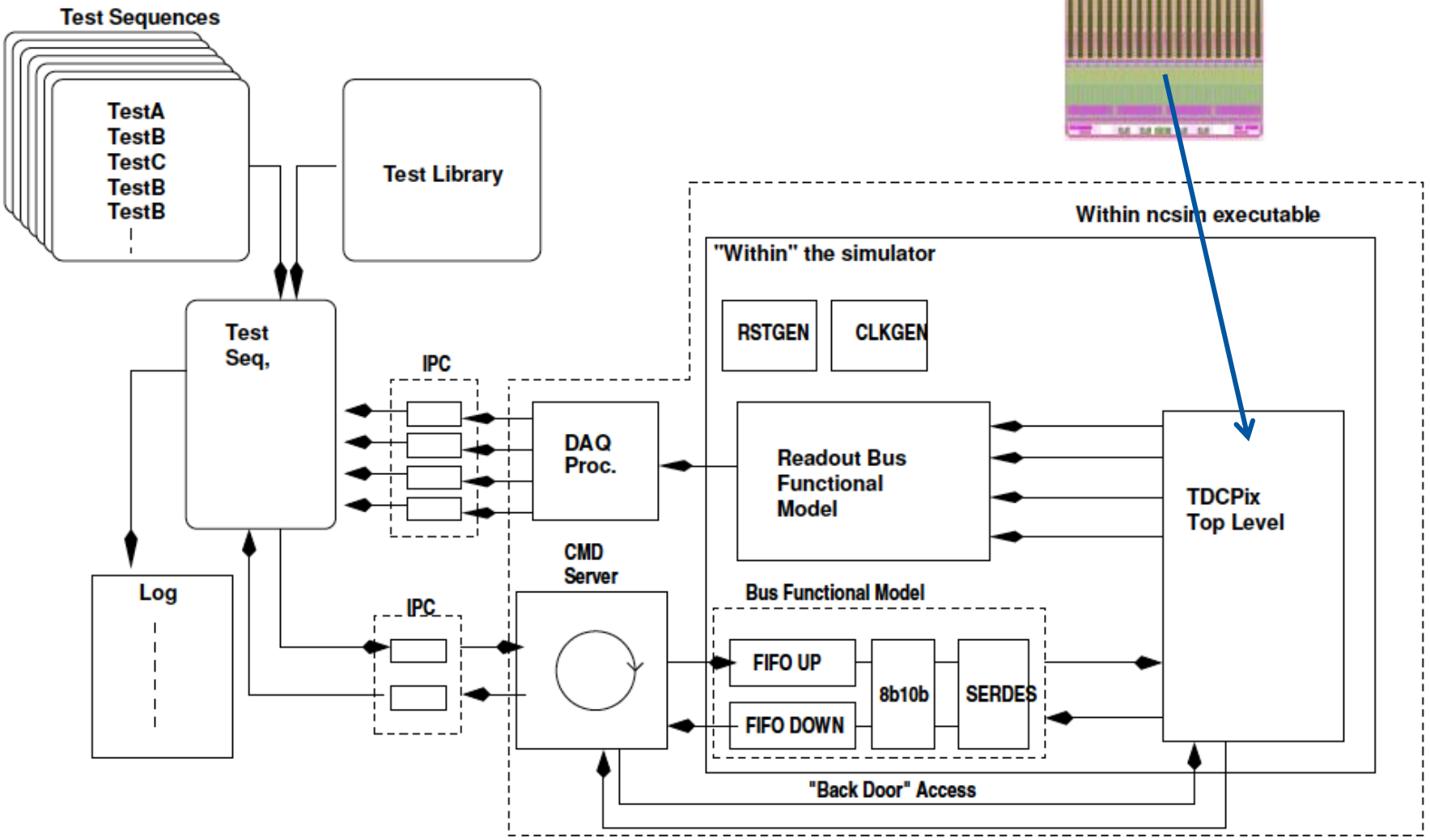
Nominal	Qty	Power domain	Current [mA]	Total Current [mA]	Power [mW]	Total Power	Remarks and conditions
Pixel Analog	1800	VDDanalog	**0.140**	252.000	0.168	302.4	Constant current bias
Pixel Digital	1800	VDDdigital	**0.160**	288.000	0.192	345.6	Constant current bias
Col bias analog	20	VDDanalog	**1.000**	20.000	1.2	24	Constant current bias
Col bias digital	20	VDDdigital	**0.340**	6.800	0.408	8.16	Constant current bias
Hit Arbiter	360	VDDdigital	0.046	16.500	**0.055**	19.8	GAR Power Static calc, VCD
DLL SM	20	VDDdigital	0.950	19.000	**1.14**	22.8	AK estimate, checked by GAR
DLL	20	VDDtdc	10.333	206.667	**12.4**	248	Lukas DLL review
Buffers_32x	120	VDDtdc	1.750	210.000	**2.1**	252	Spectre sims
FineRegister	720	VDDtdc	0.208	150.000	**0.25**	180	Spectre sims
Encoder	720	VDDtdc	0.001	0.840	**0.0014**	1.008	Power Static calc, vcd
Coarse time unit	40	VDDdigital	10.583	423.333	**12.7**	508	Power Static calc, vcd
Quarter chip RO	4	VDDdigital	46.667	186.667	**56**	224	Analysis by GAR
Serializer	4	VDDserializer	72.917	291.667	**87.5**	350	Reviewed 4/2/2013, with TxLines buffers
PLL	1	VDDpll	91.667	91.667	**110**	110	Reviewed on 4/2/2013

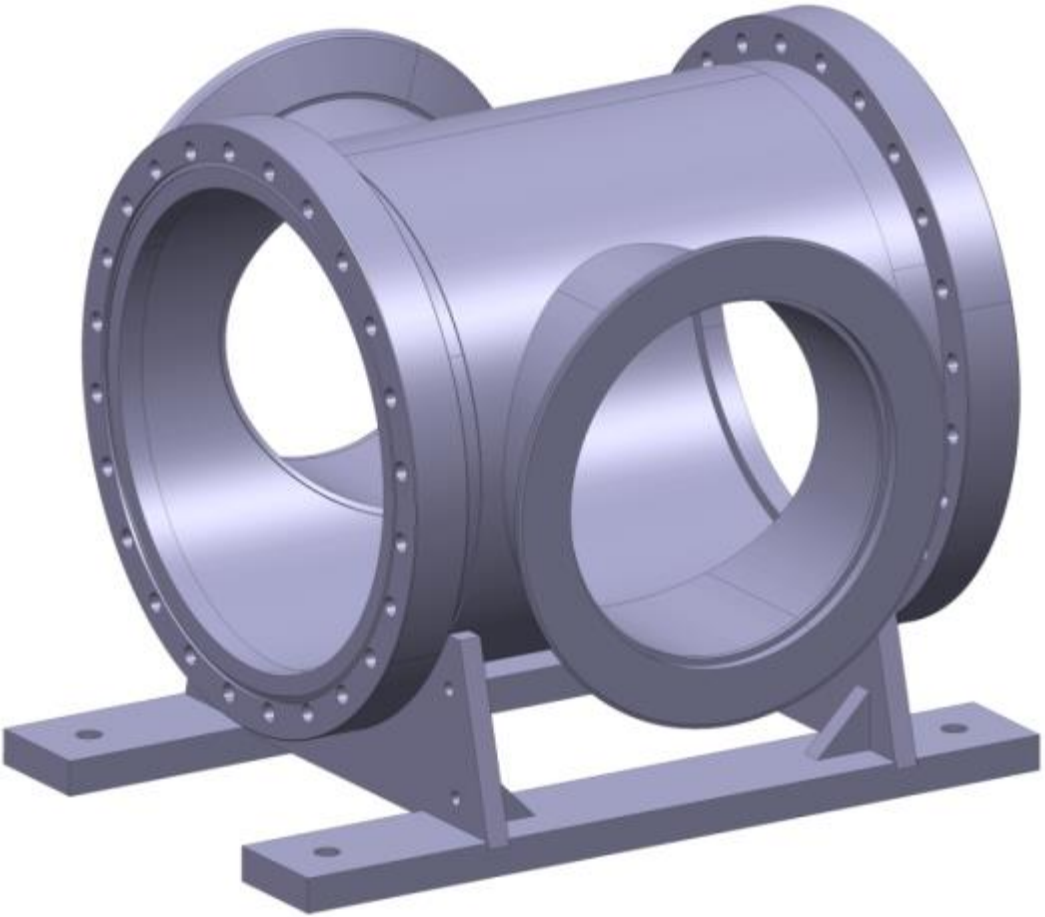
TOTAL [mW]	**2596**	
VDDanalog	326	12.6%
VDDdigital	1128	43.5%
VDDtdc	681	26.2%
VDDpll	110	4.2%
VDDserializer	350	13.5%

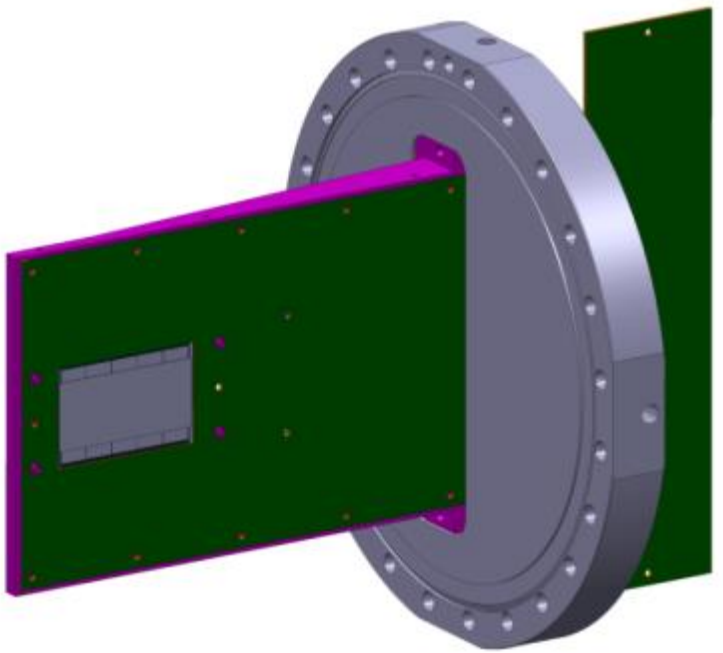
TOTAL [mA]	**2163**
VDDanalog	272
VDDdigital	940
VDDtdc	568
VDDpll	92
VDDserializer	292

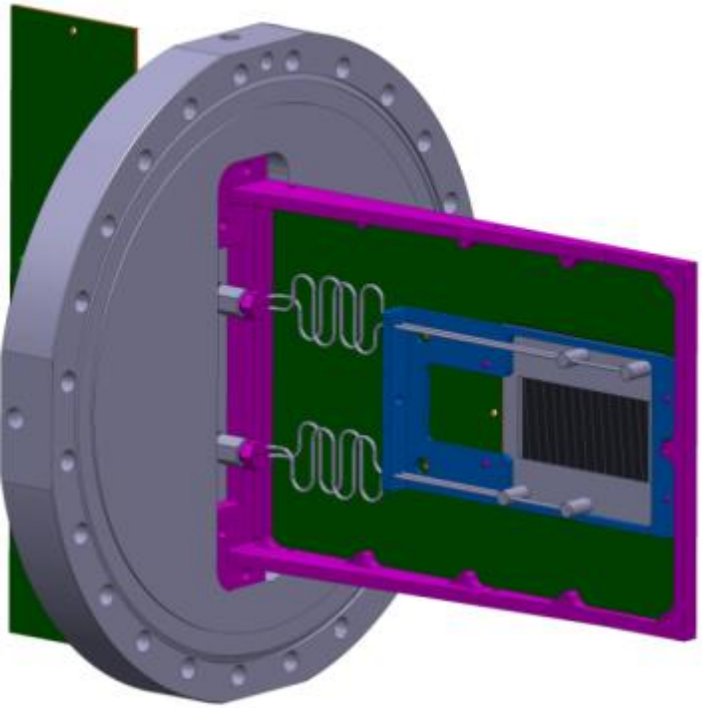
Full chip simulation

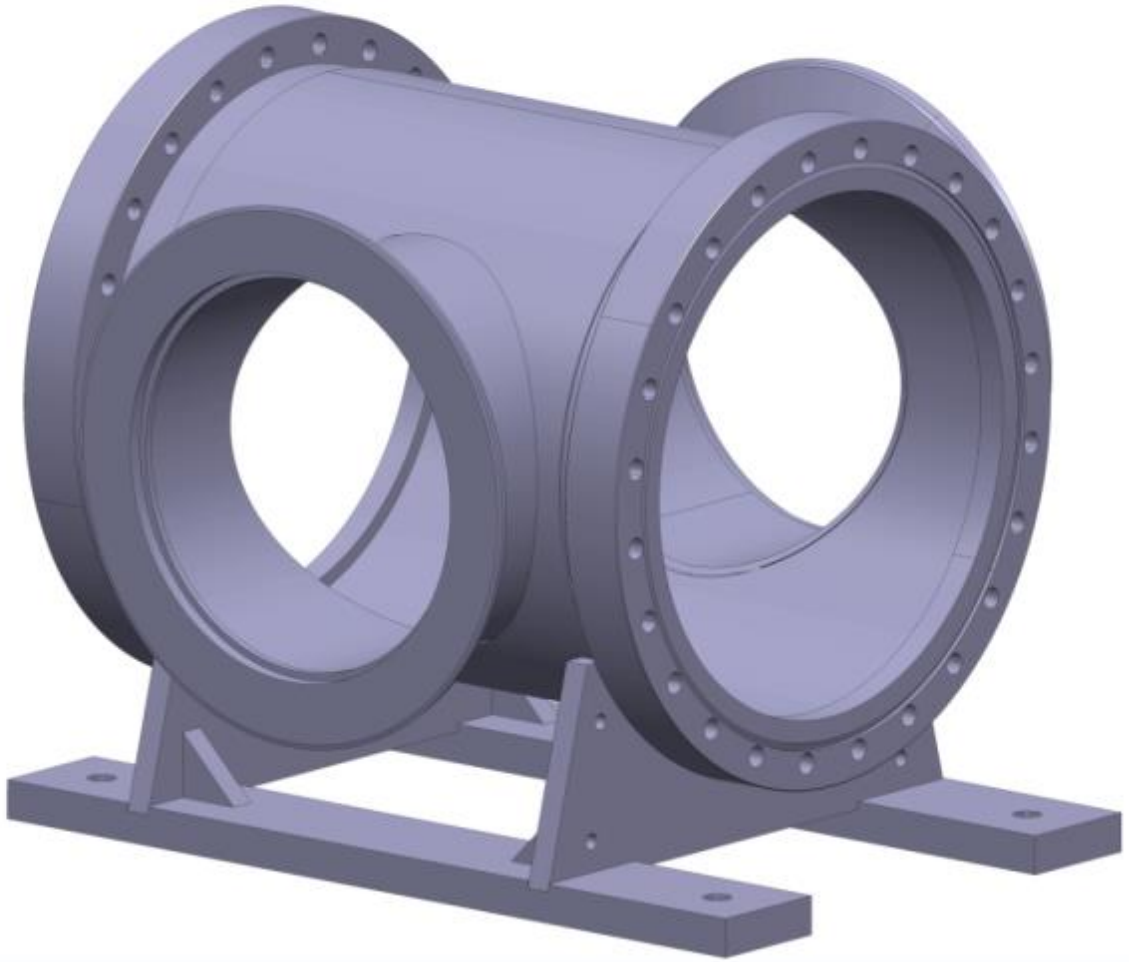


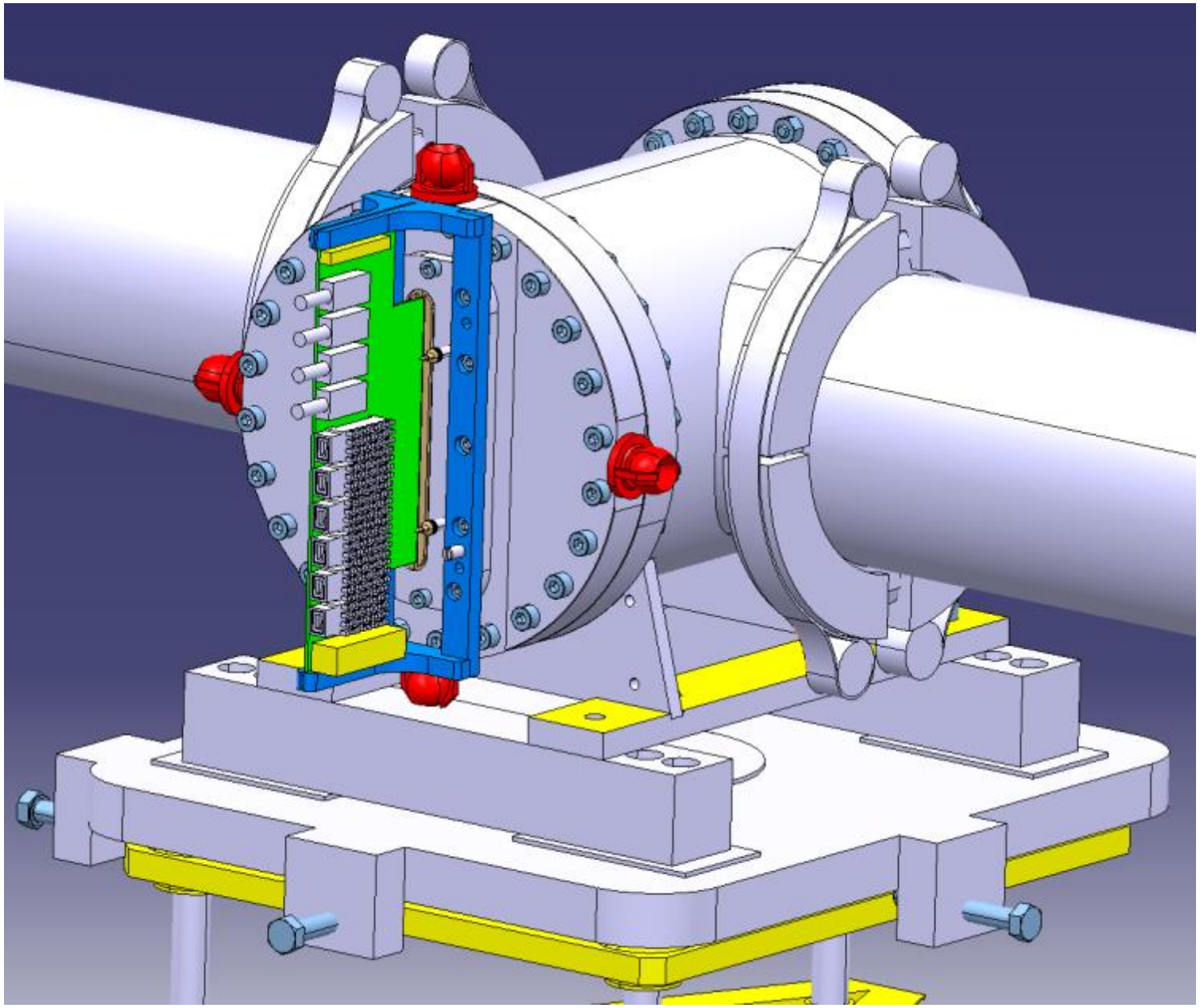


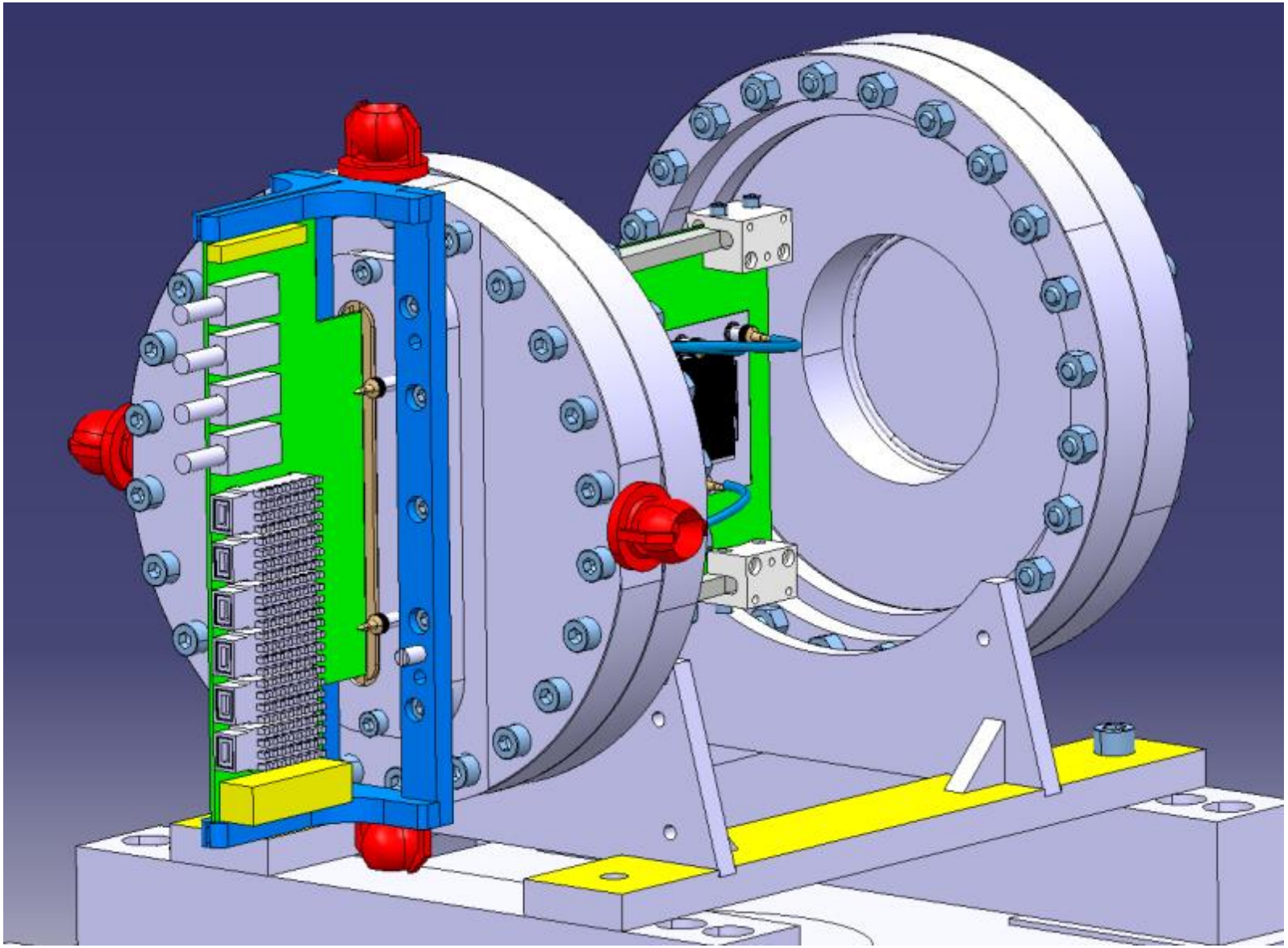


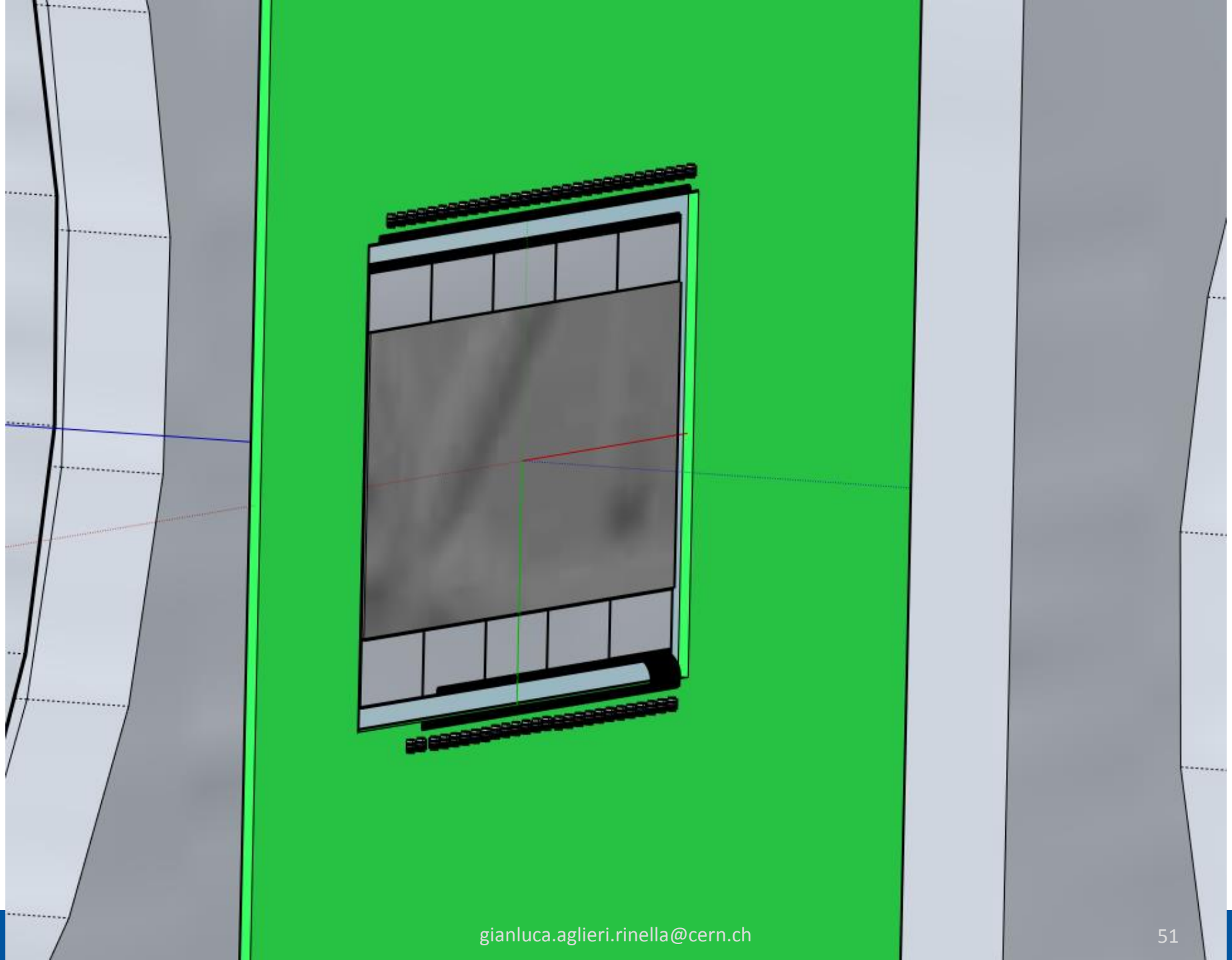


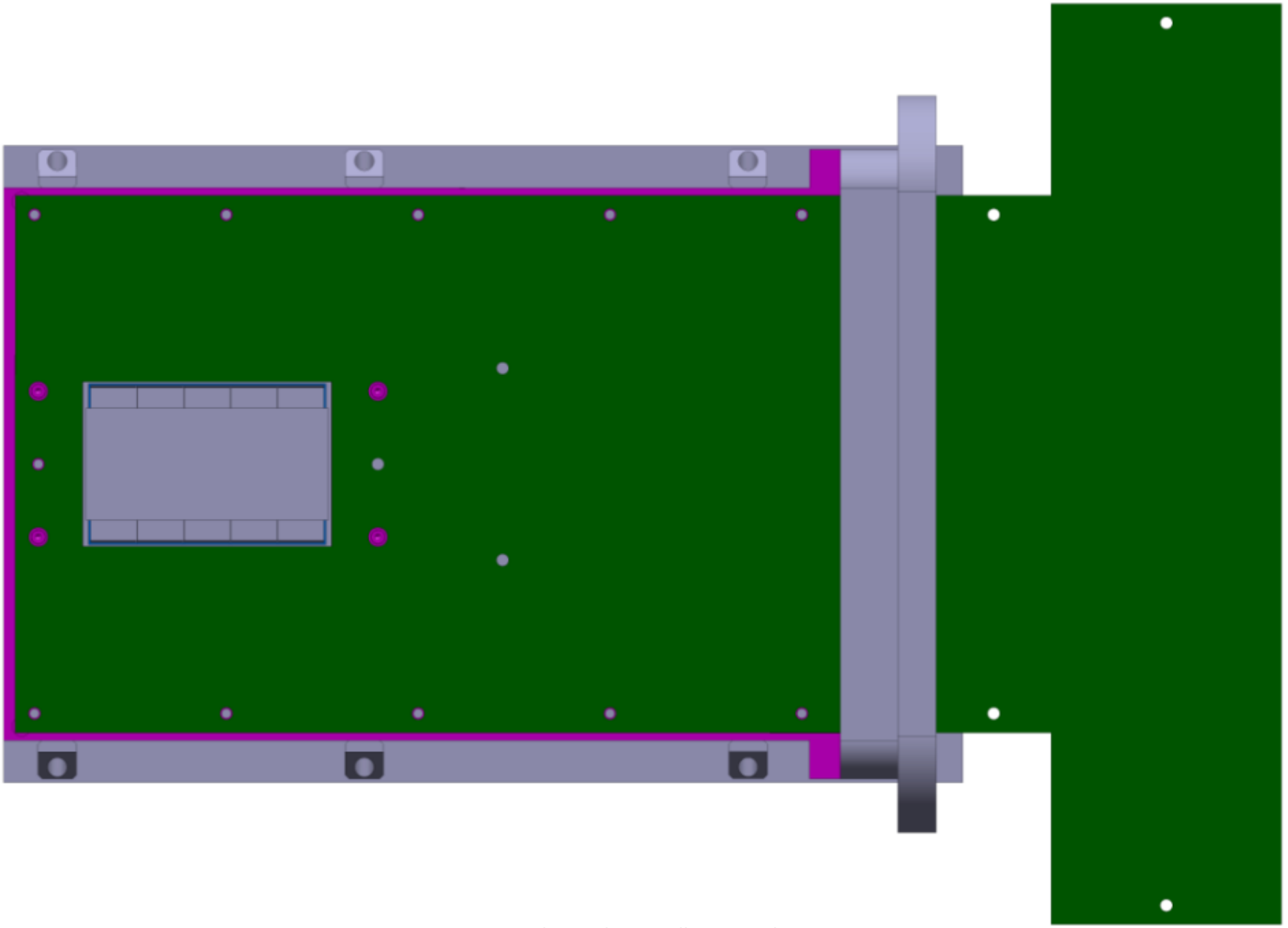


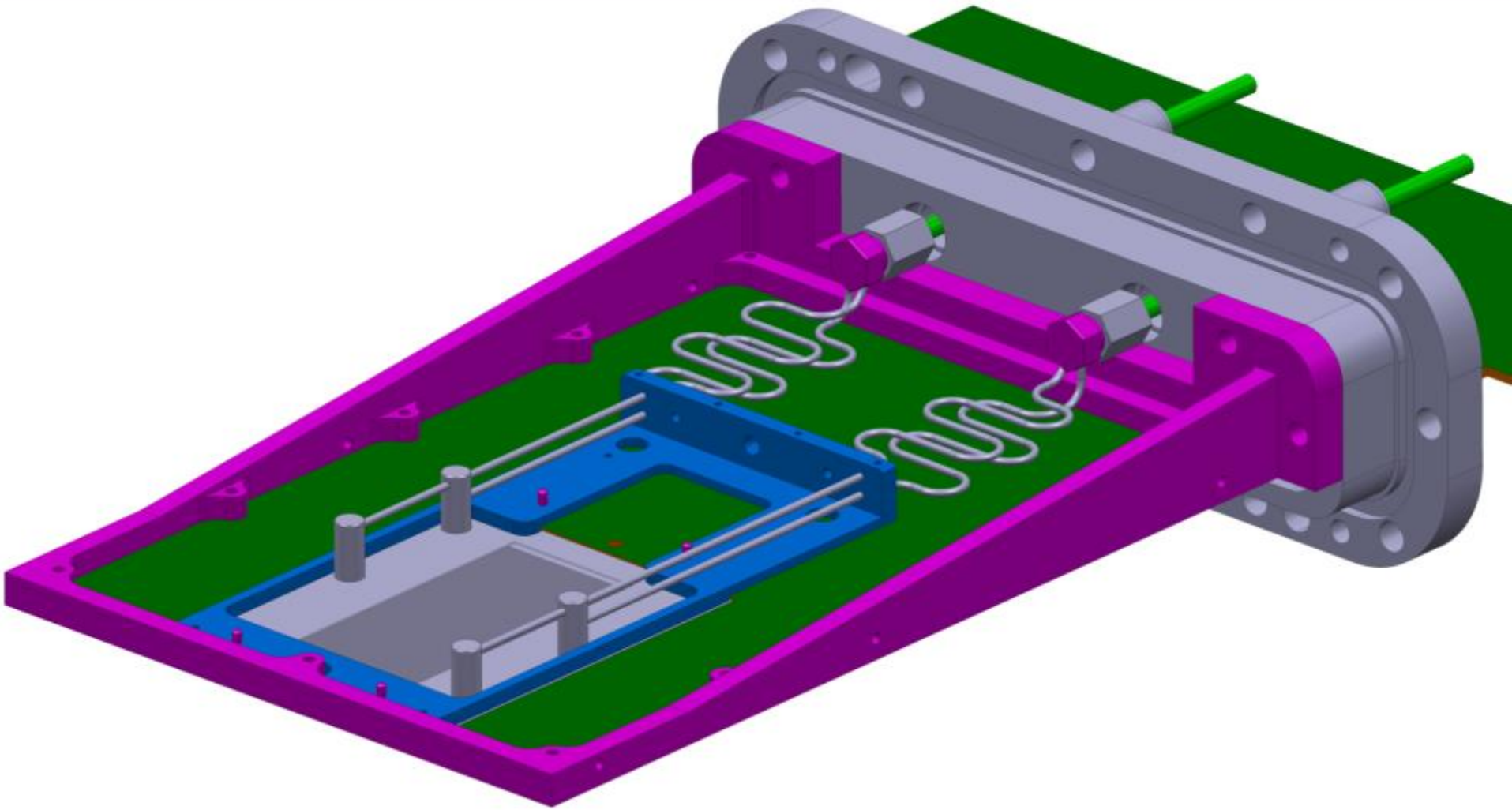


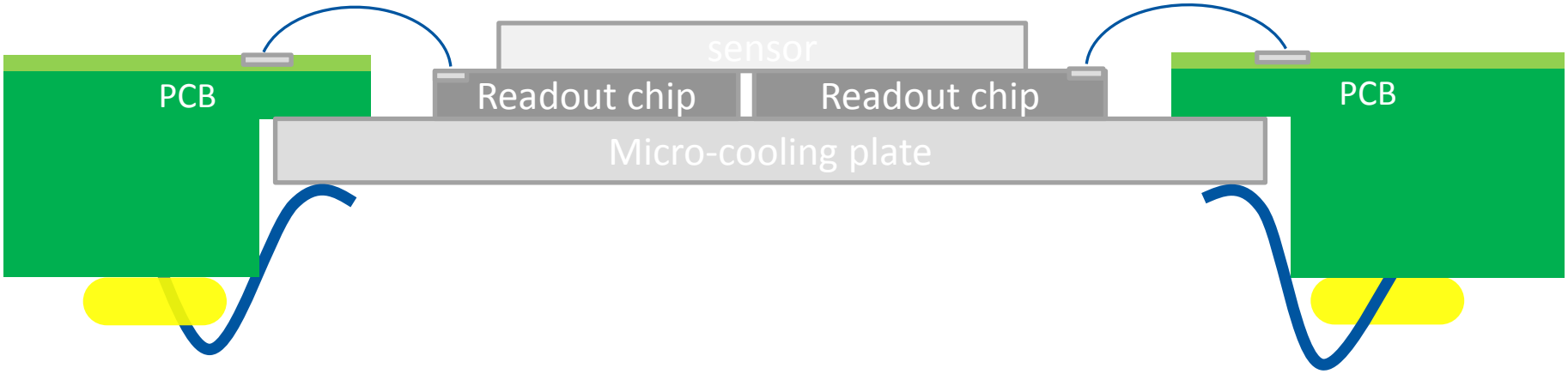











sensor
PCB
Readout chip
Readout chip
PCB
Micro-cooling plate