ABC 130 – Silicon Strip Readout Chip for ATLAS Inner Tracker Upgrade

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Design Team

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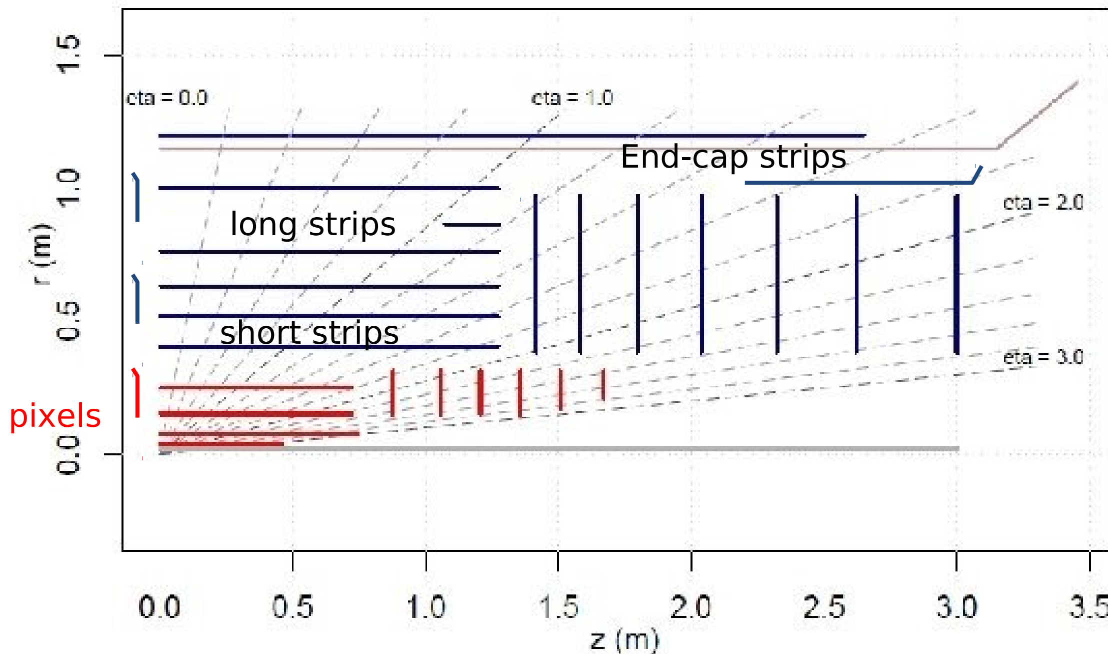
- UCL: M. Warren, S. Kilani
- University of Liverpool: A. Greenall

ABC130 purpose and history

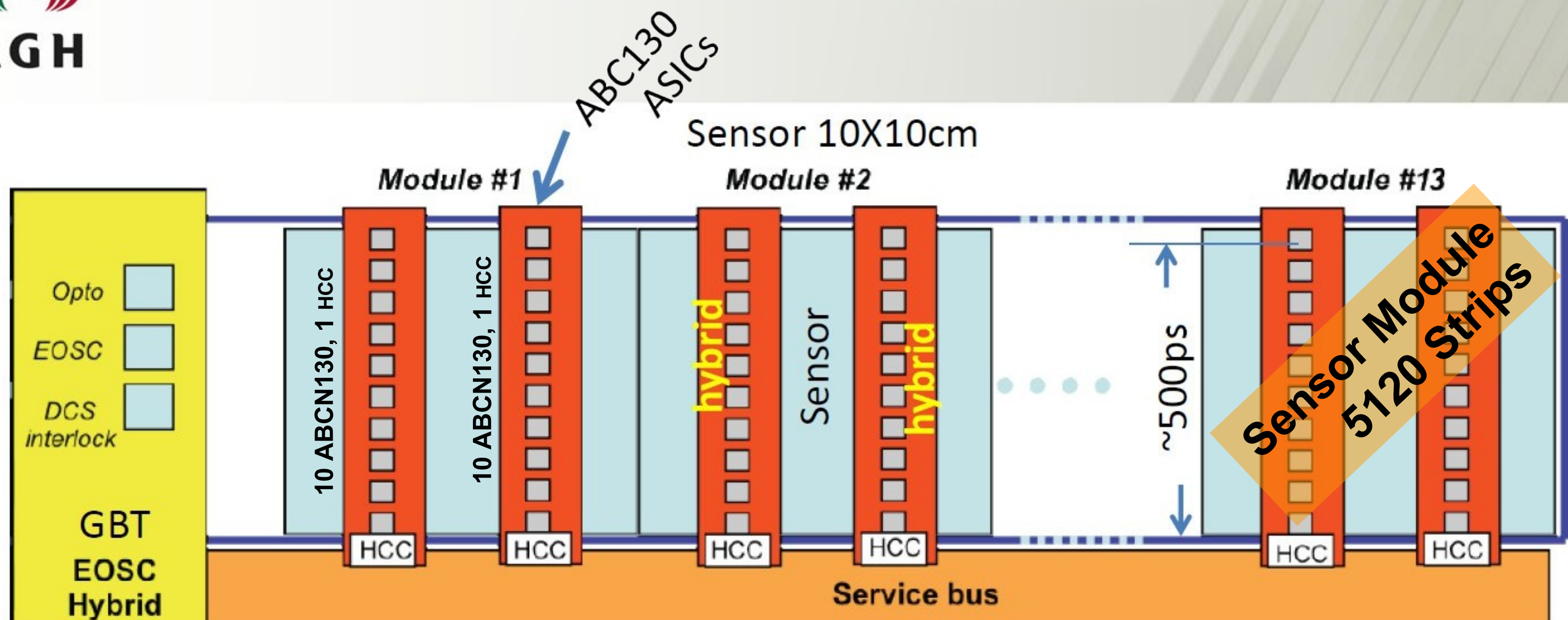
New All-silicon ATLAS Inner Tracker



- New strip tracker size
  - 193 m^2 of silicon, 74×10^6 channels
  - ~20 000 modules
  - ~300 000 ABC130 chips

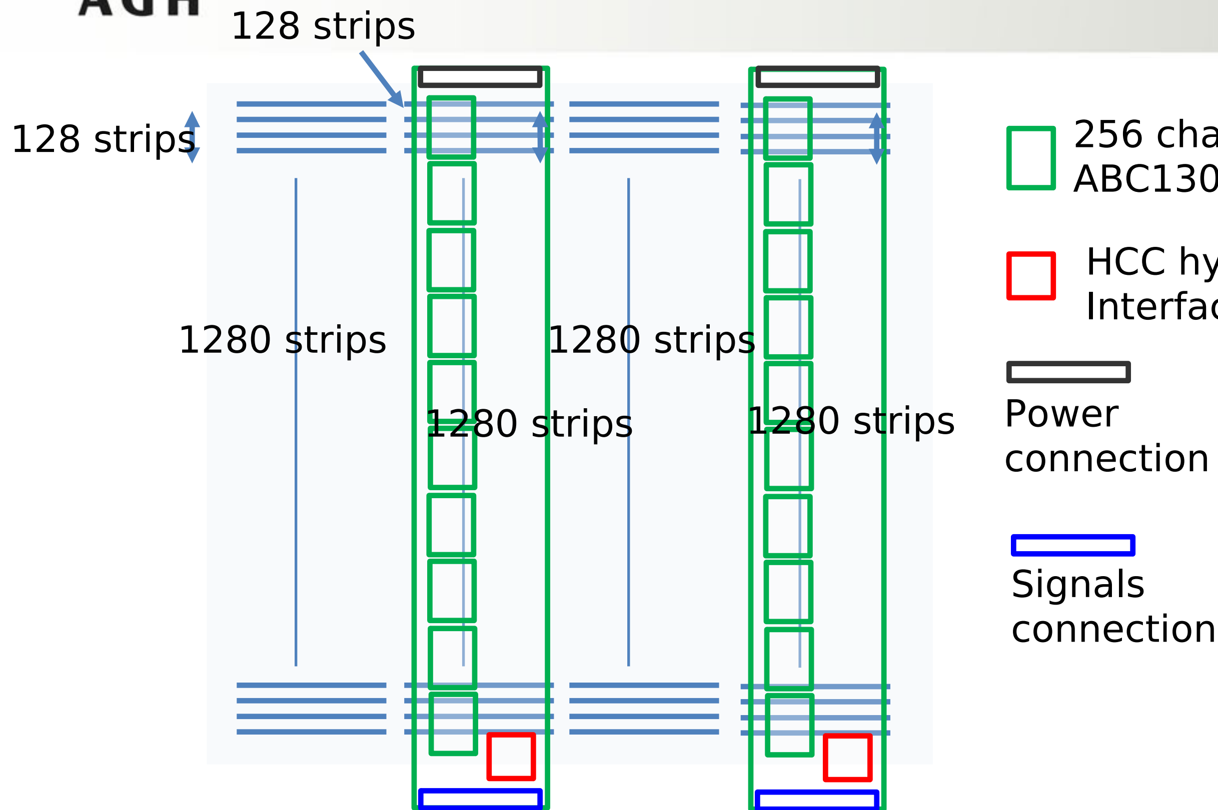
- ABCD3T
  - presently used in ATLAS SCT
  - BiCMOS DIMILL 0.8um
- ABCN-25
  - module development vehicle chip
  - IBM CMOS 250nm
- ABC130
  - new trigger and readout architecture
  - simplified hybrid
  - IBM CMOS 130nm

Silicon Strip Tracker Stave



- Barrel “short” strips stave
  - 26 sensors of 10x10cm
  - 2 hybrids per sensor
  - 52 hybrids in stave, each with 10 ABC130 and single HCC
- Sensor:
  - 4 columns of strips
  - 1280 strips in a column
  - 74.5 um pitch
  - 2.5 cm strip length

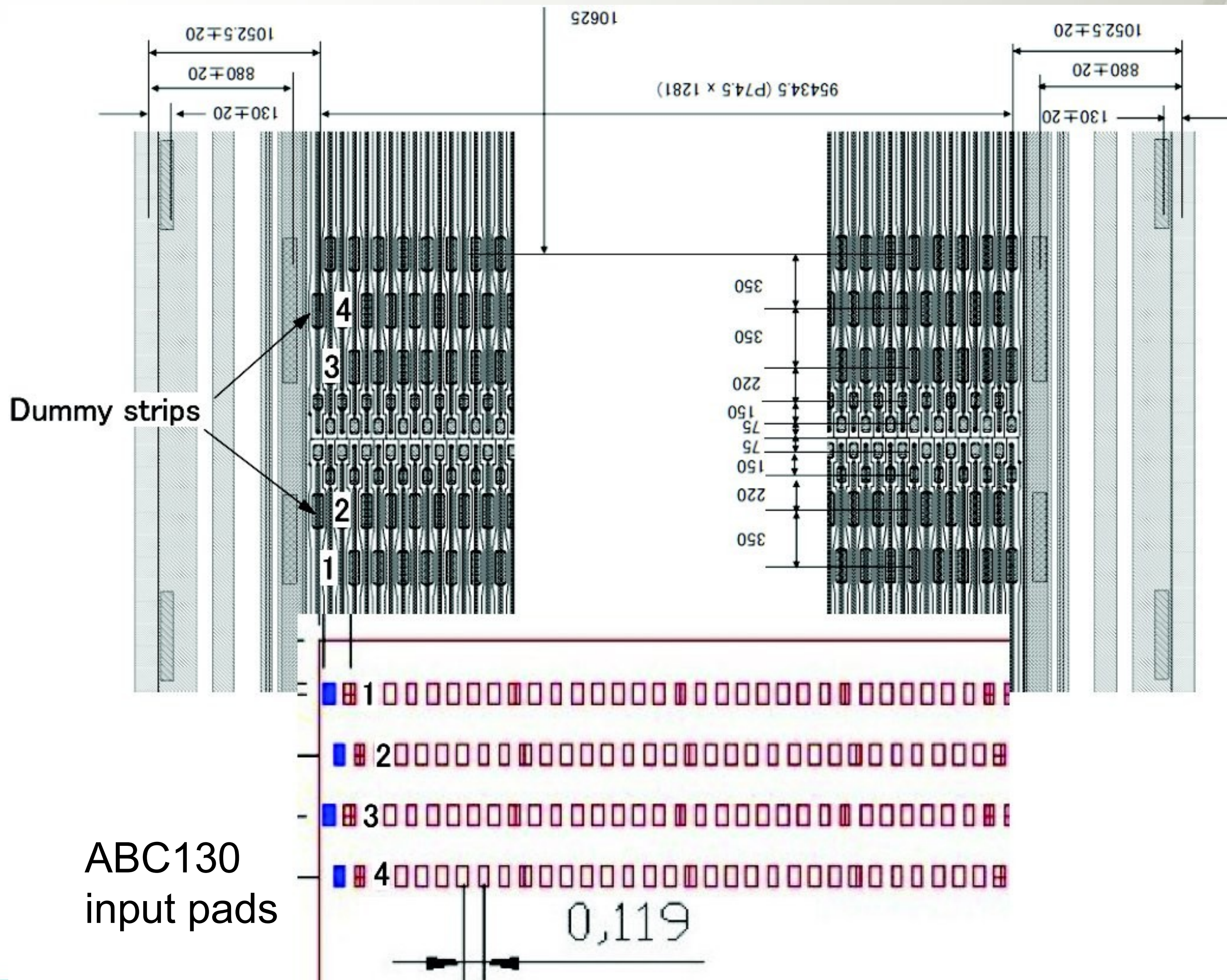
Hybrid concept



- Hybrid glued directly to the sensor
- 256 channels in ABC130

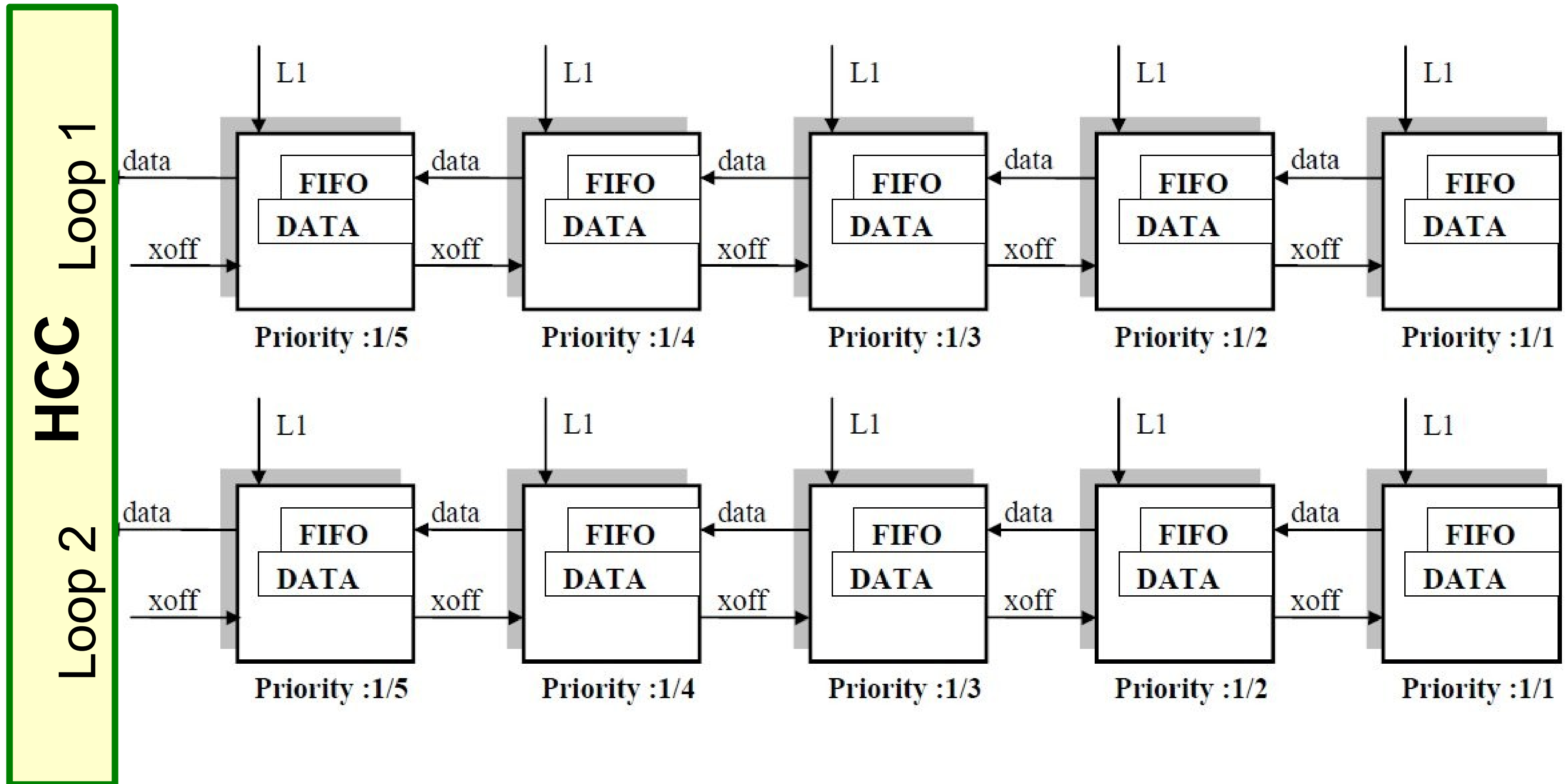
- HCC – Hybrid Controller Chip
  - GBT interface
  - clock generator with phase adjustment
  - Data concentrator

Bonding ABC130 to sensor



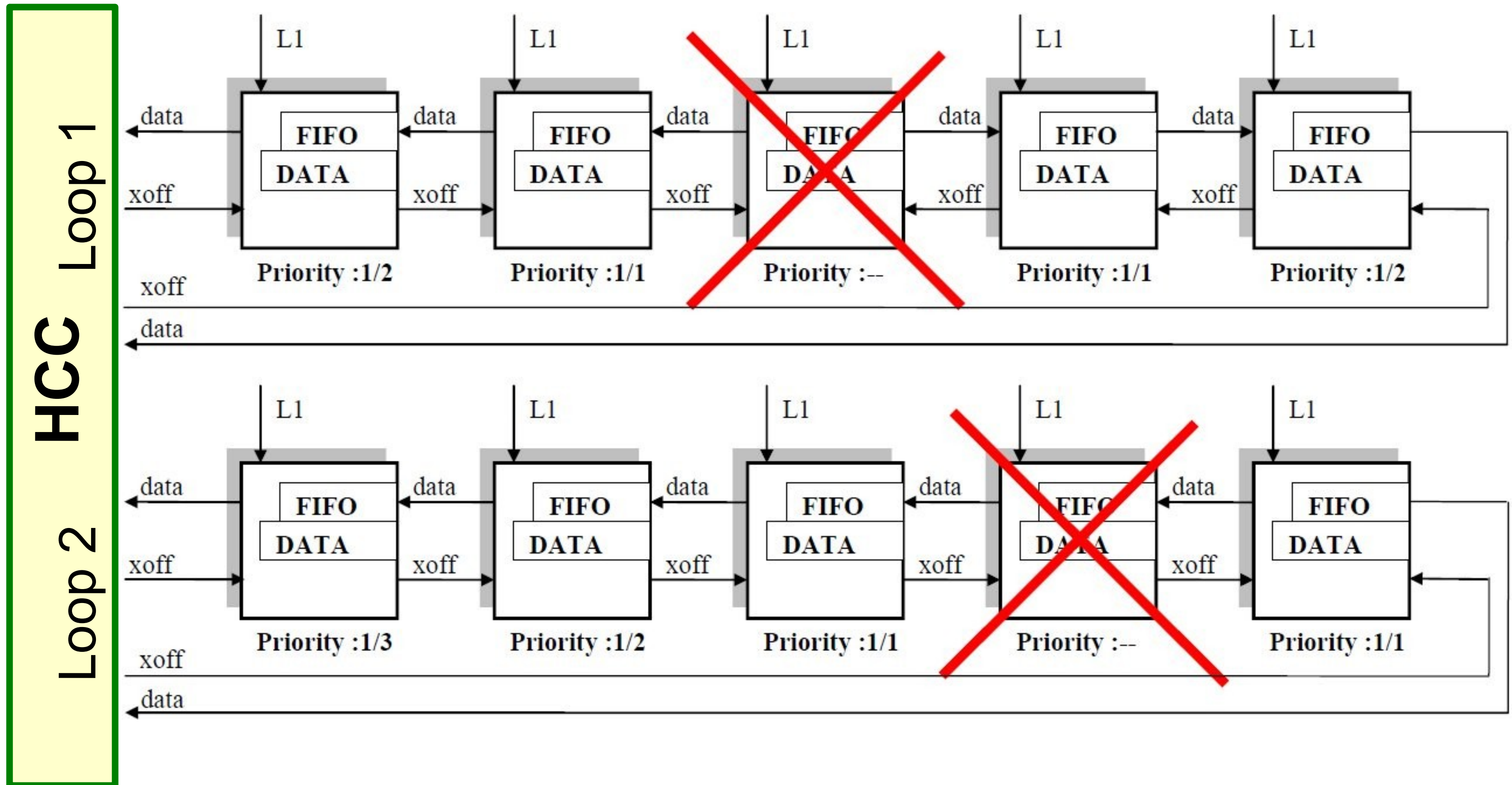
- Single ASIC bonded to two sensor columns/rows
- Four rows of input pads

ABC130 readout chain



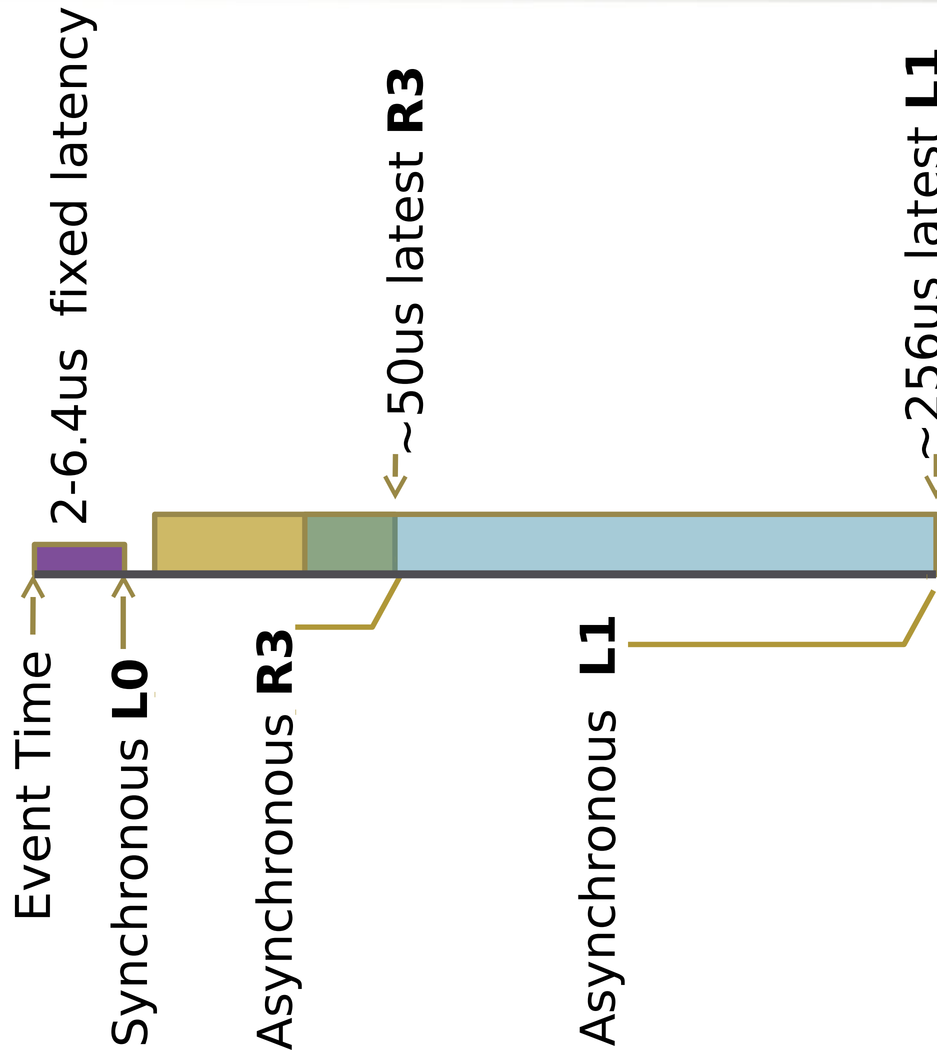
- Simpler hybrid comparing to present one
- Each ABC130 is a data concentrator with priorities

Readout chain with broken chips



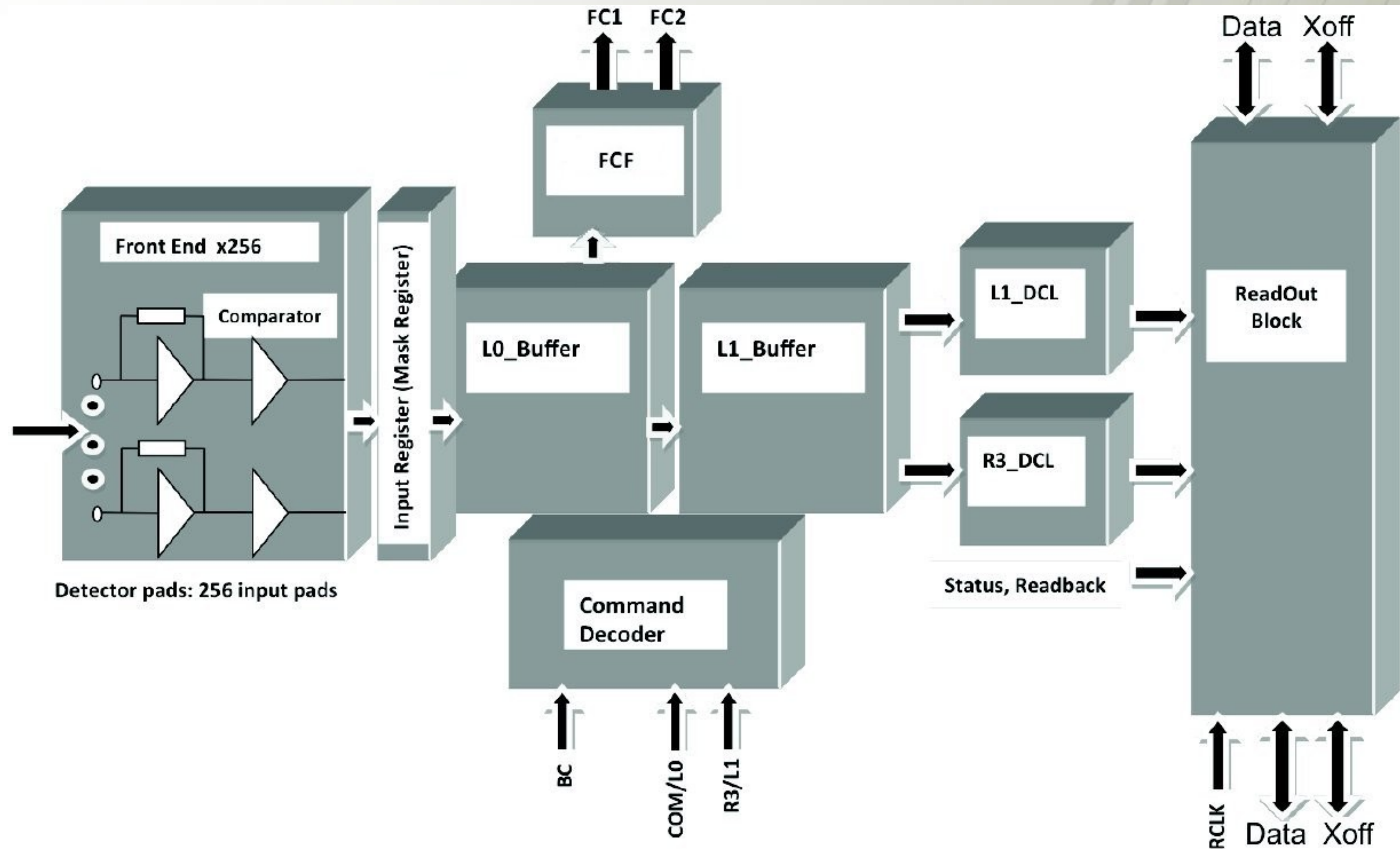
- Bidirectional data connection
- Single broken chip/connection in a loop is acceptable

Triggers sequence



- Three triggers
  - L0 – synchronous
  - R3 – Regional Readout Request (~10% of detector) – input for L1 decision
  - L1 – whole detector readout
- R3 prioritised over L1
- Non sequential readout – self describing data blocks needed

ABC130 block diagram



- Two RAM buffers L0 & L1/R3
- Different data compression logic (DCL) for L1 & R3

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Front-end Design

Designed by Jan Kaplon

Preamplifier

Amplifier and integrator

Amplifier, integrator, threshold separation and trimming

Comparator

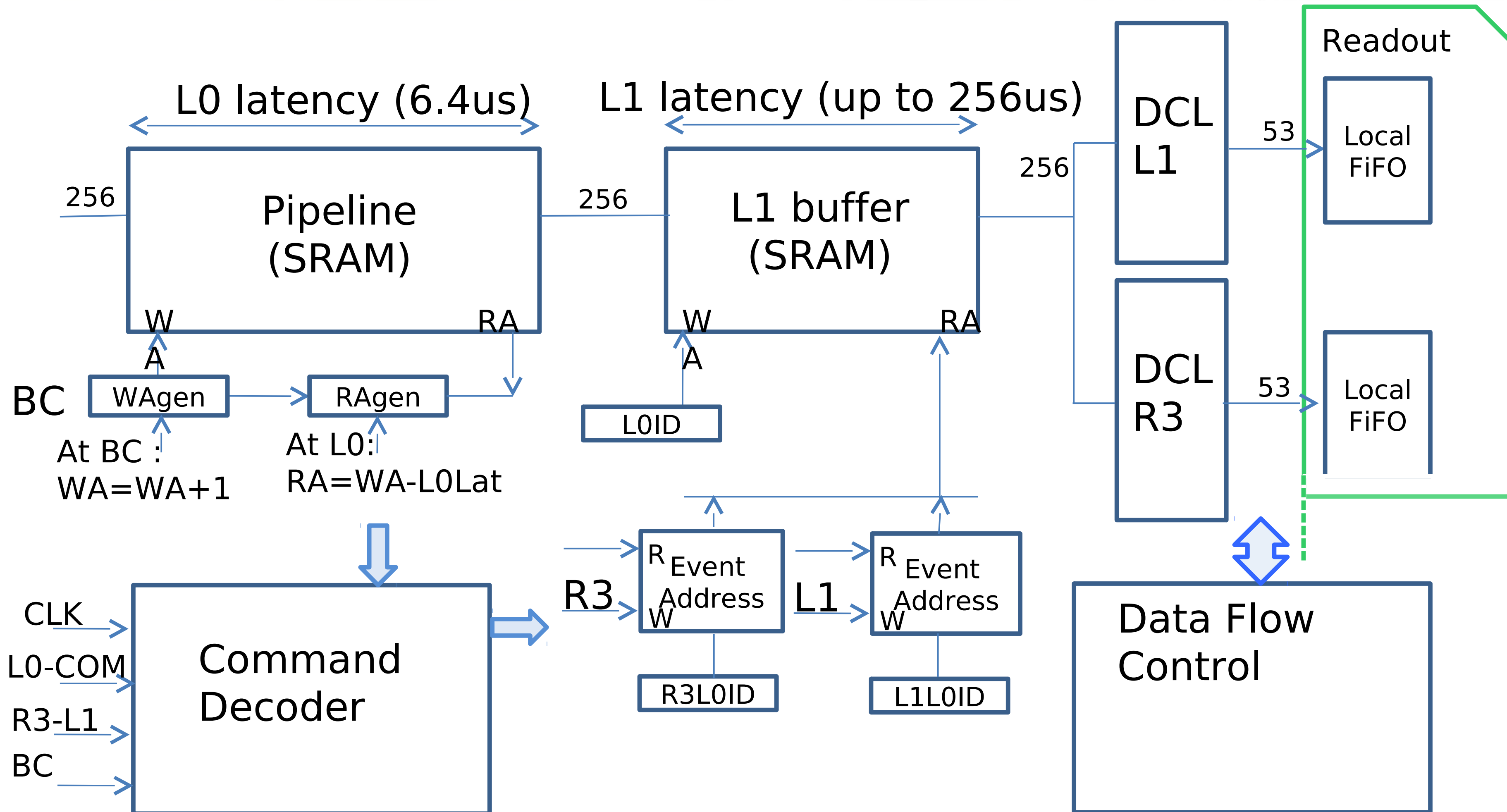
Requirements:

- ENC <1000e- @3pF
- ENC <1500e- @10pF
- Low power consumption (<300uW/channel)
- Peaking time <25ns (time walk <16ns)

Architecture:

- binary output
- 5-bit current DAC in each channel
- single 8-bit threshold DAC for 256 channels

ABC130 Data Flow

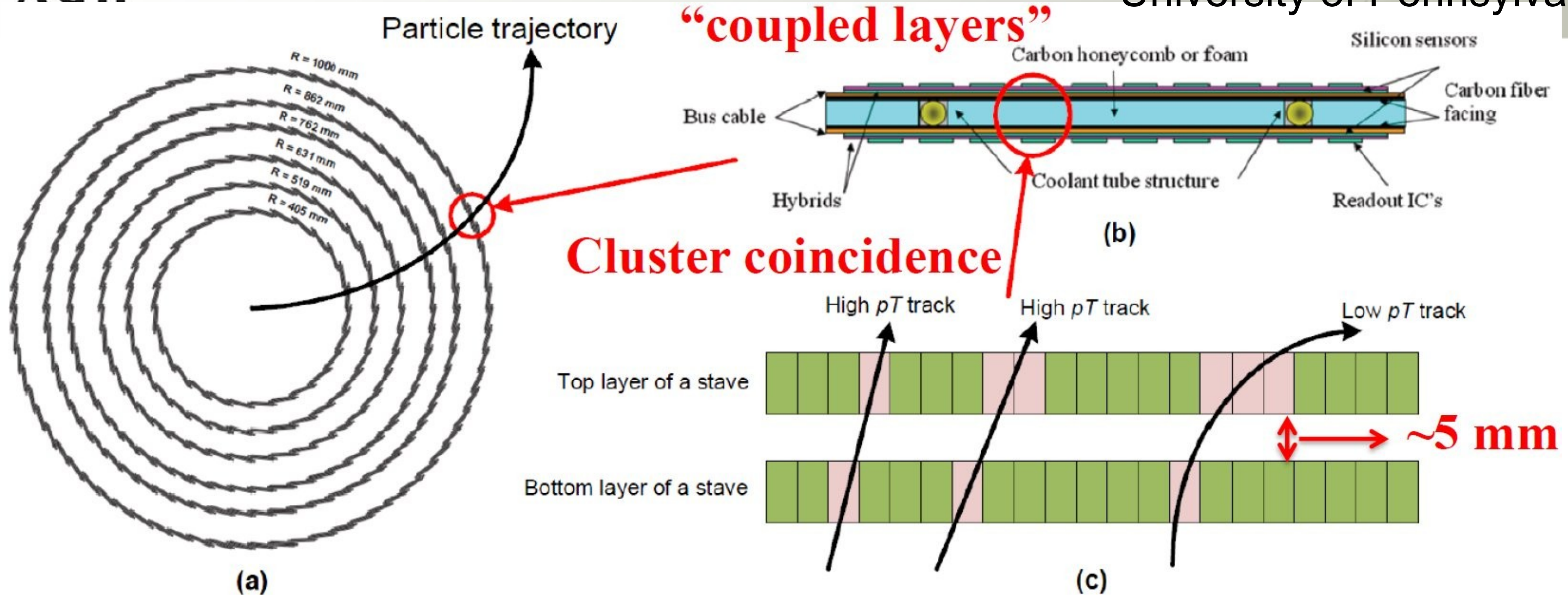


DCL – Data Compression Logic

Data readout

Fast Cluster Finder – optional input to L1

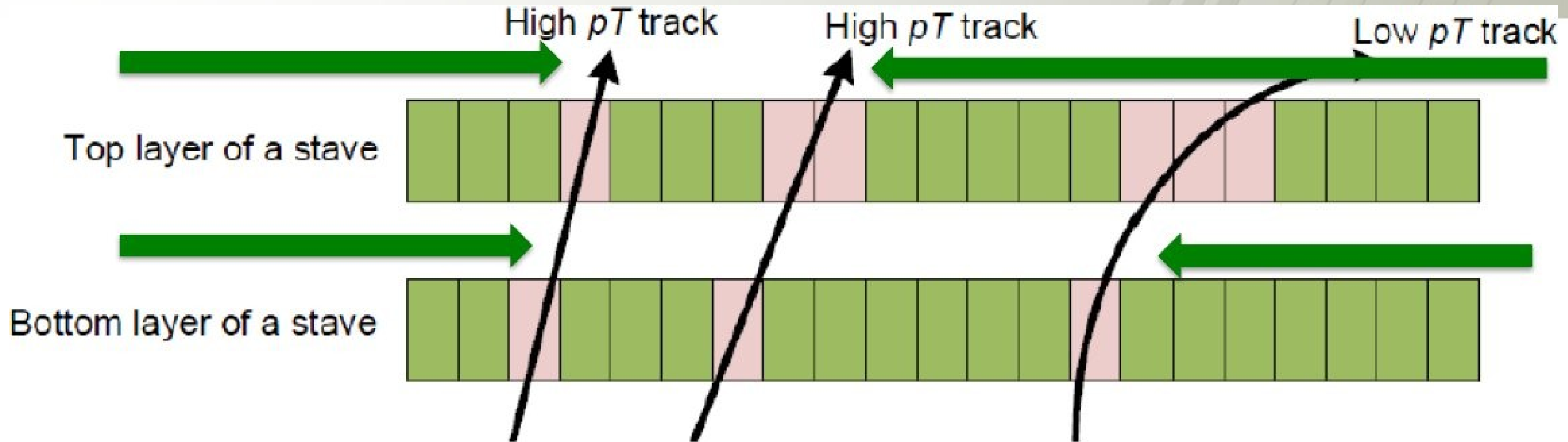
University of Pennsylvania



- Sensors are mounted to both sides of a stave
- A charged particle crossing these coupled layers would leave one "cluster" at each layer. The coincidence of clusters indicates the presence of a track. The offset in the cluster positions is related to the pT of the track.
- No input from muon or calorimeter is needed.

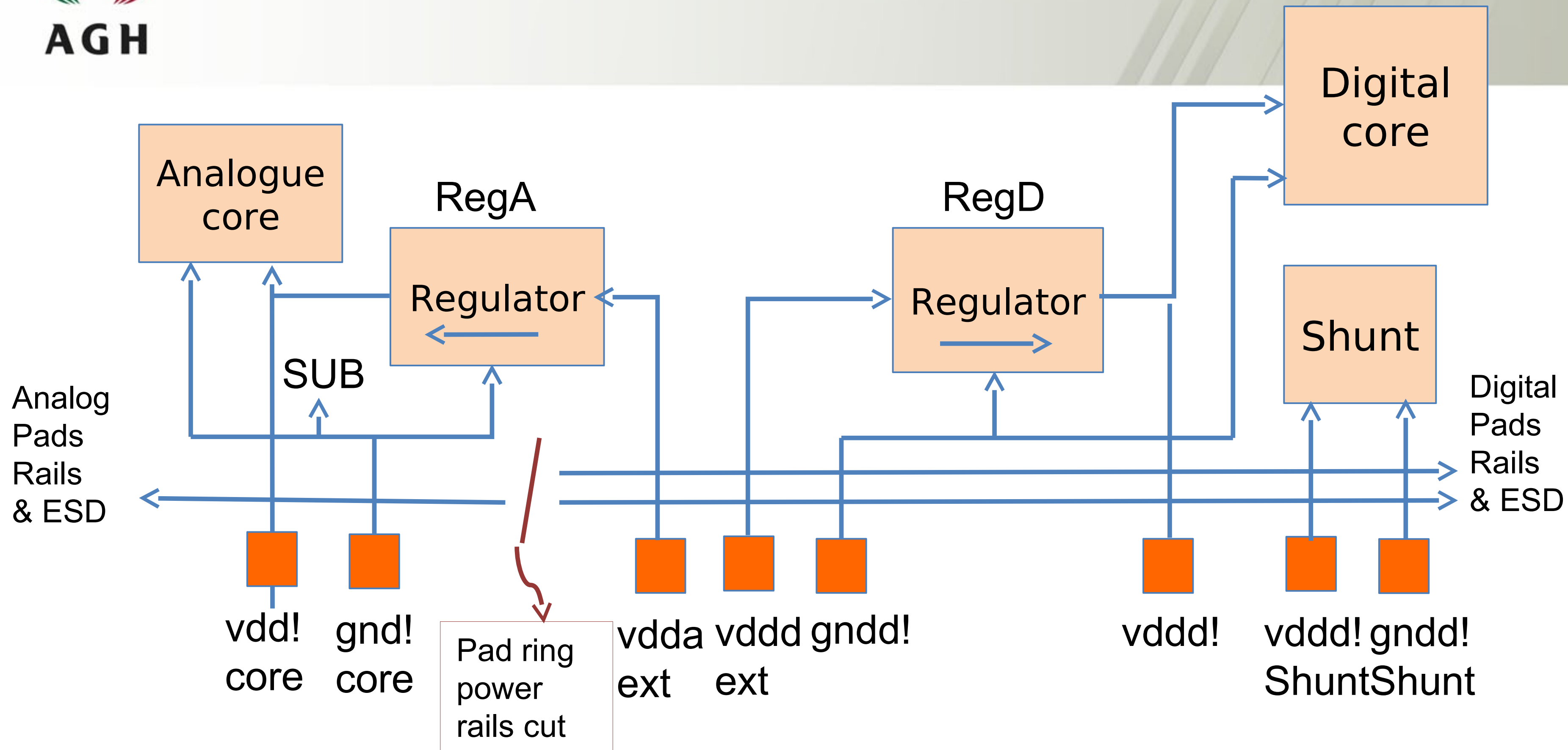
Haichen Wang, Workshop on Intelligence Tracker 2014, May 14 2014, University of Pennsylvania

FCF prototype operation



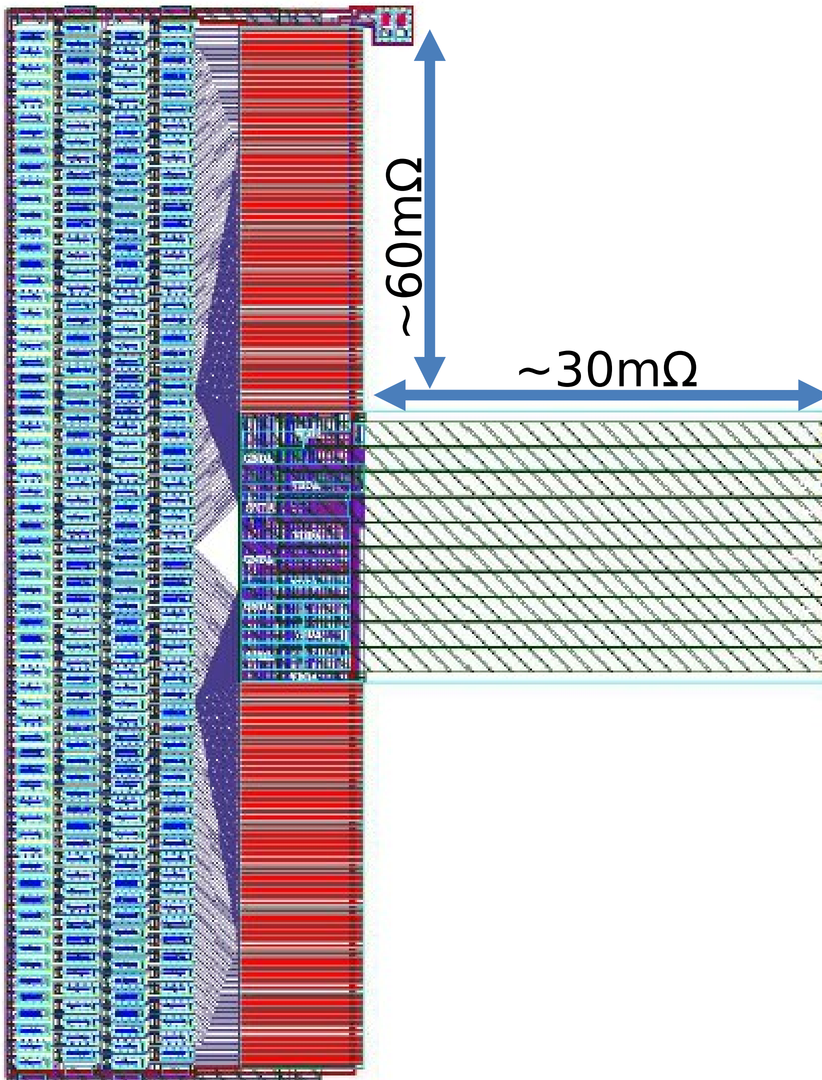
- Cluster size limited to 2 strips or less, to reject low pT tracks (R3 DCL is similar in operation but more flexible & much slower)
- Up to 2 clusters can be find (in R3 DCL up to 4)
- The cluster finding algorithm takes ~6 ns – every single clock 16 information bits are send out (x 2 dedicated outputs)
- Additional ASIC called Correlator is necessary
- Functionally correct

Powering scheme



- Ready for both power options: serial powering and DC/DC converters
- Internal shunt transistor – serial powering

Front-end Floorplan



- Main analogue GND/VDD connection on the back (close to regulator) – easier hybrid design
- Power lines resistivity
  - vertical ~60mΩ
  - horizontal <30mΩ
- Pads and fan-in occupied 2/3 of area

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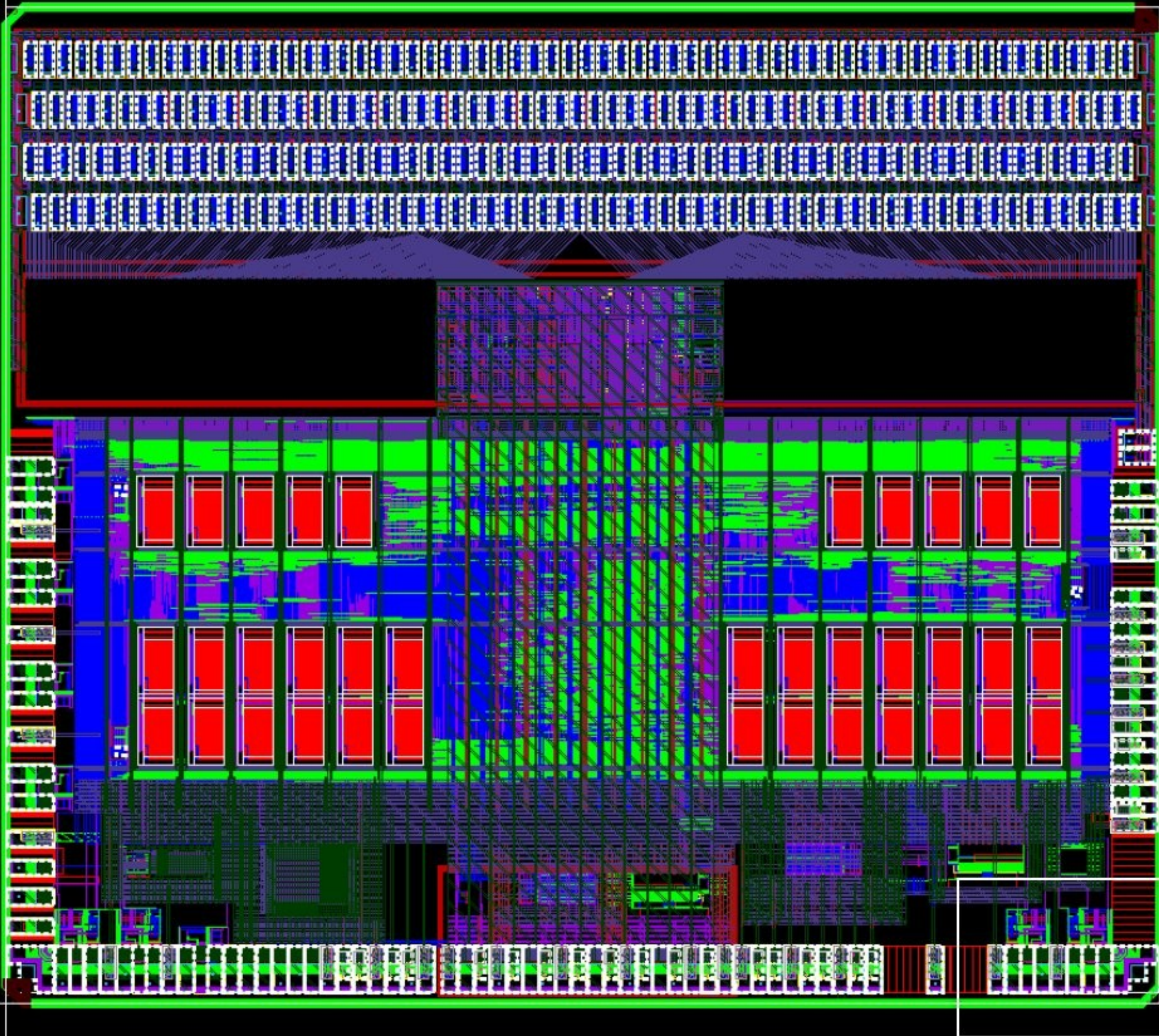
Design methodology – design

- Analogue part designed fully custom
- Digital part written in Verilog with macros delivered by CERN or designed by our team
  - memories delivered by CERN (corrections and abstracts generation necessary)
  - pads design fully custom then Verilog models, abstracts and liberty description created
  - for other blocks (e.g. regulators) only Verilog models and abstracts created
- Extensive simulation based verification done
  - Verilog scripts to verify ASIC basic operations
  - Matlab based framework for a chain of ASICs with realistic trigger and data structure

Design methodology – implementation

- Whole digital part synthesised in single step (finally FCF delivered as macro block)
  - clock gating applied
  - scan chain added
- Place & route done in flat flow
  - floorplan (very time consuming)
  - placement (power filtering capacitance added)
  - clock tree synthesis with clock grouping
  - routing with antenna removal
- Hand DRC error removal (remaining after P&R)
- Digital and analogue parts put together and verified – DRC, LVS with Calibre and Assura

ABC130 layout



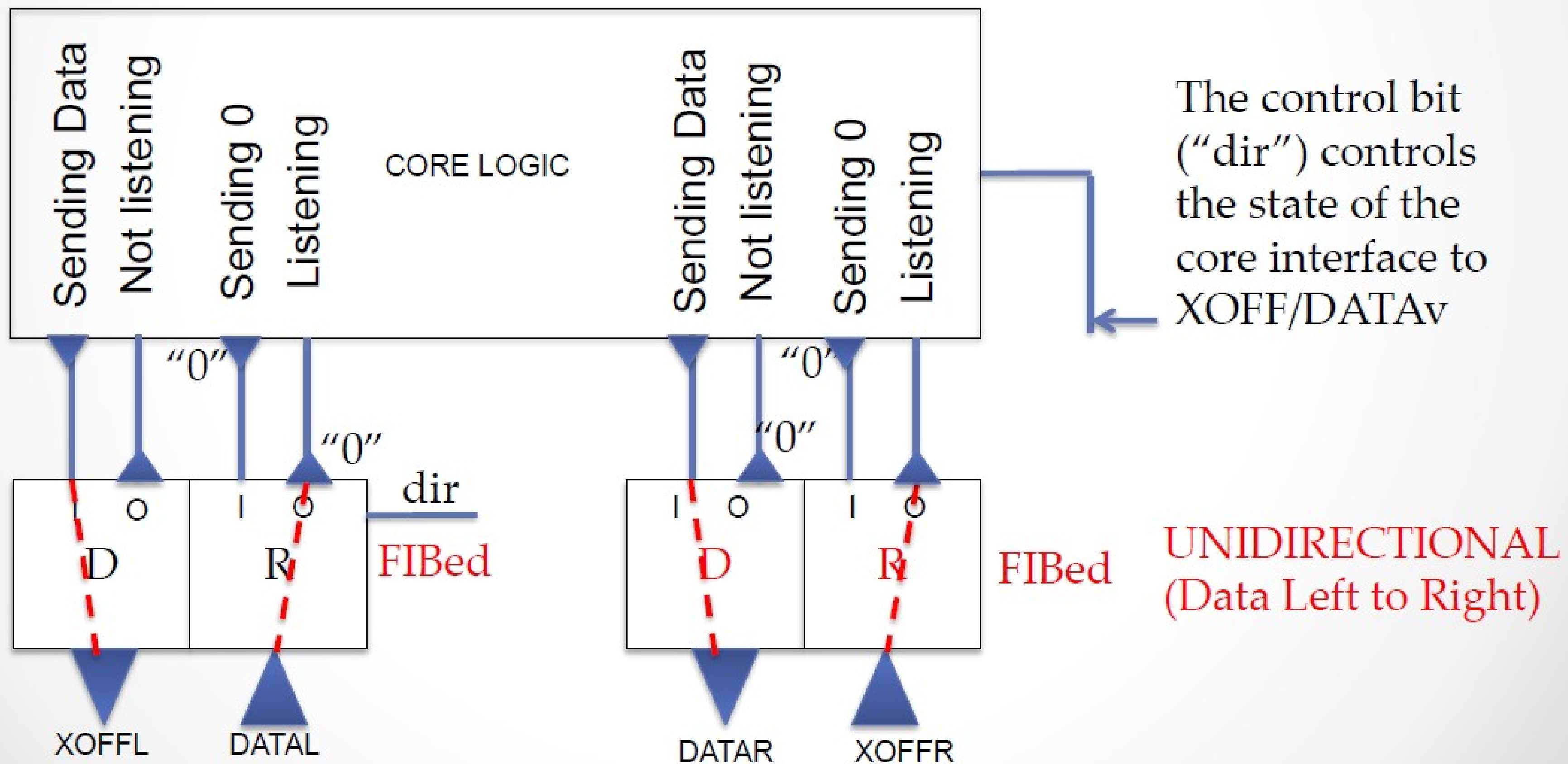
Size:
7.9 x 6.7 mm

Data should be bidirectional but …

IO model and circuit mismatch

Early Tests and Findings

- **Present FIBed chip operation**

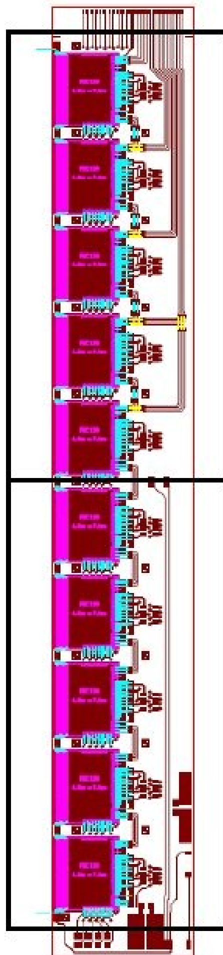


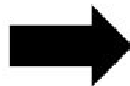
Francis Anghinolfi, ATLAS Upgrade Week, 7-11 April 2014, University of Freiburg

ASICs bonded to hybrid and sensor

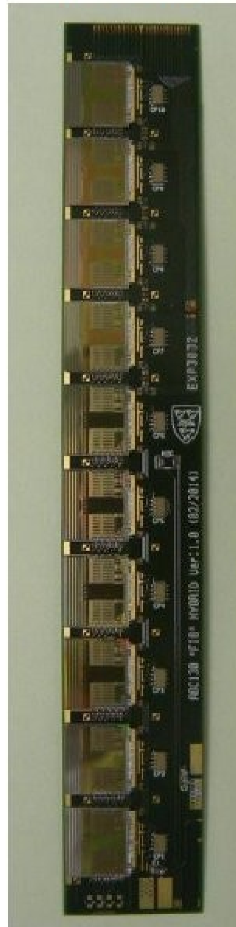
“FIB’d” ABC130s

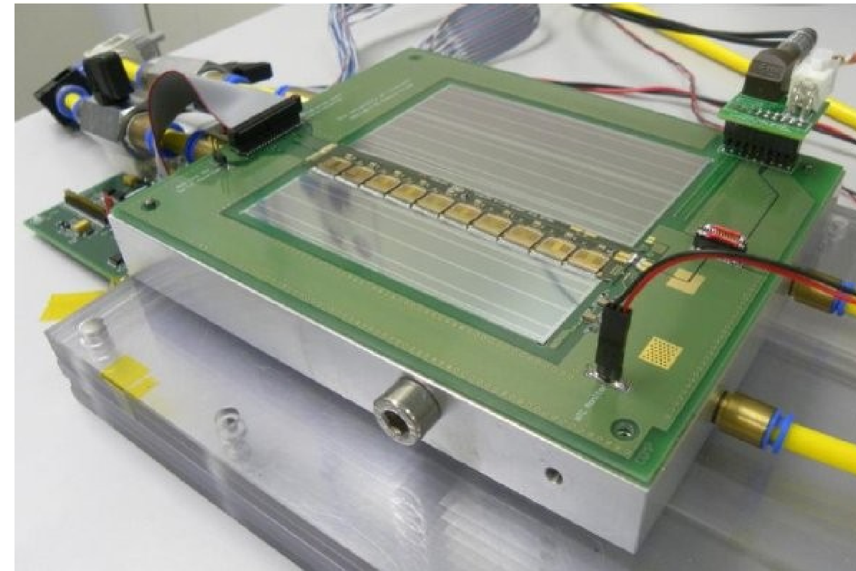
“Non-FIB’d” ABC130s





The reality





- First measurements done
- No problem with wire-bonding from ASIC to sensor

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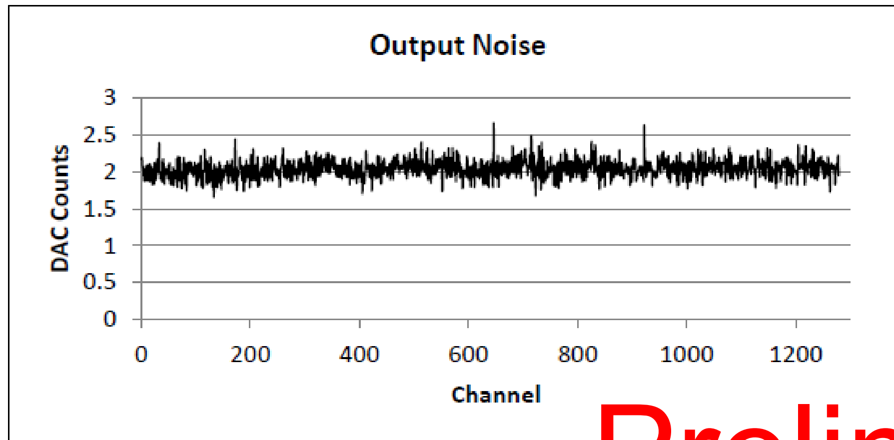
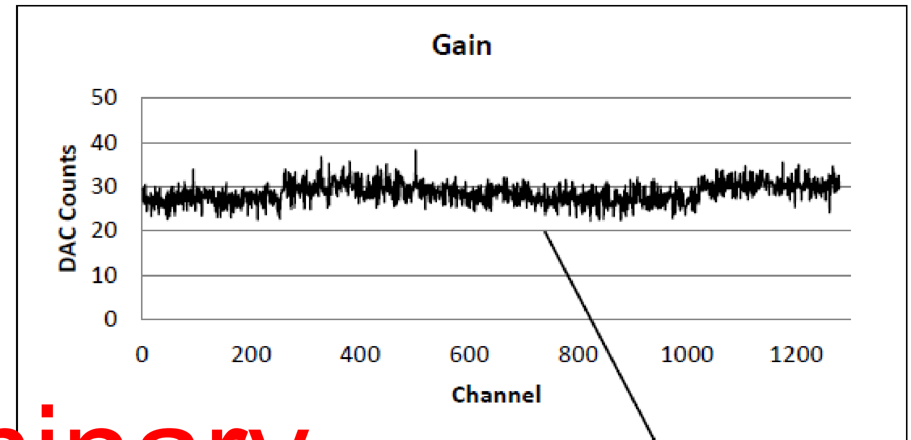
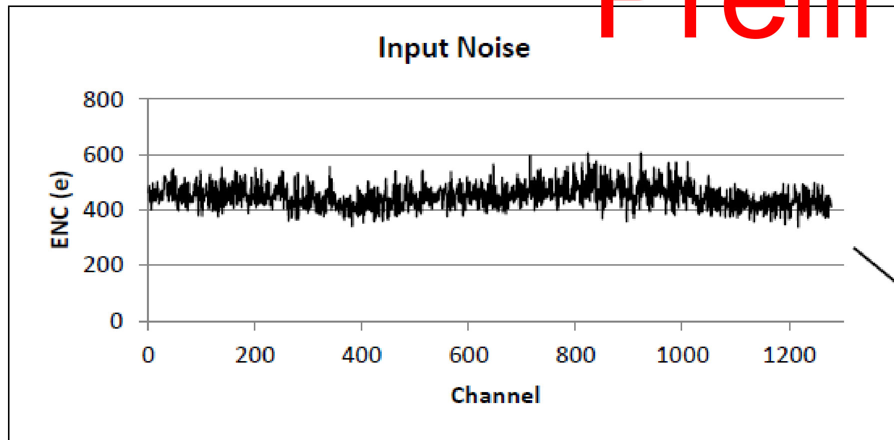
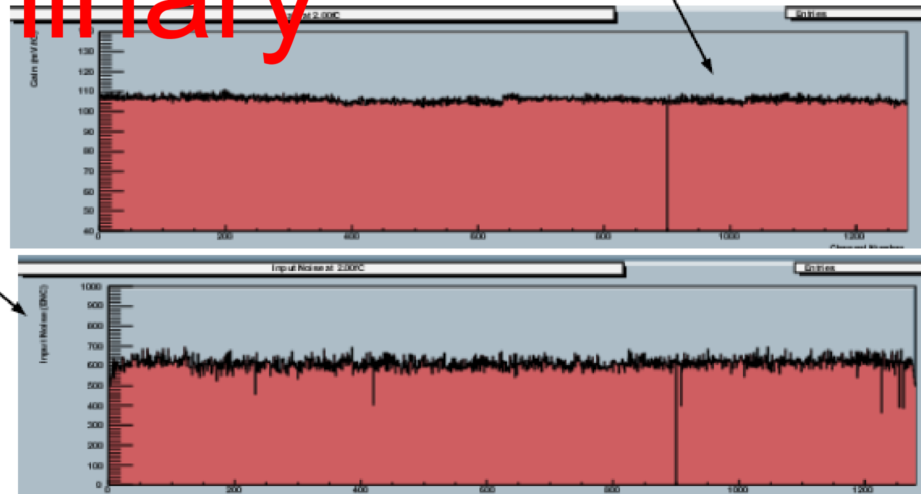
FIB Hybrid with ABC130 – Electrical Results





Preliminary





I/P Noise and Gain of Barrel Hybrid ABCN-25

Gain (92mV/fC) and noise as expected ???

Power consumption: 96 mW/chip

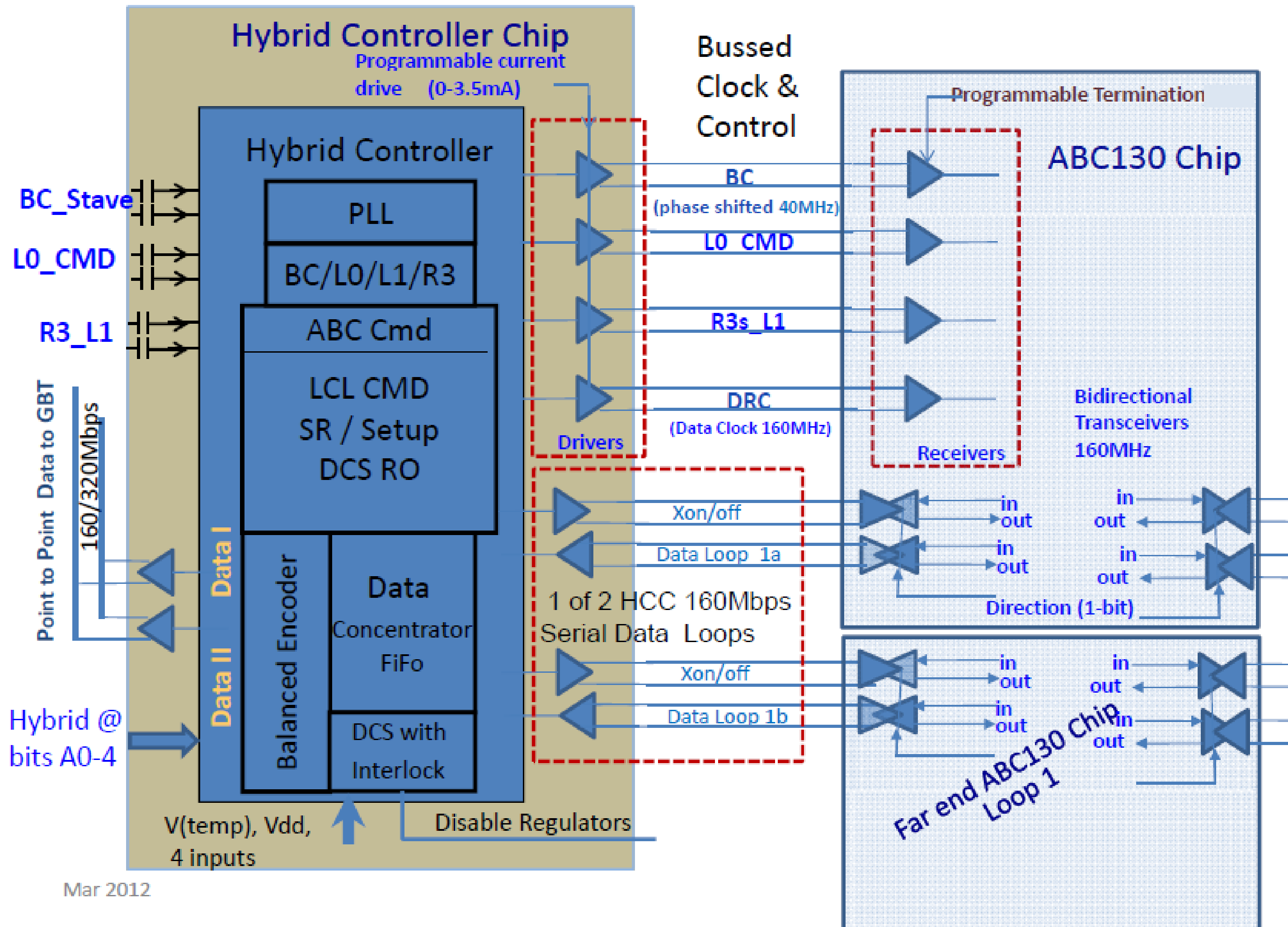
Ashley Greenall, ATLAS Upgrade Week, 7-11 April 2014, University of Freiburg

Summary

- ABC130 is a fairly complicated ASIC with two level memory, prioritised data multiplexer and bidirectional data outputs
- In spite of careful design and extensive verification small fibbing was necessary
- After fibbing chip is fully functional with expected parameters
- No problems encountered during ASIC assembly and bonding on hybrid and sensor
- 6 “respin” wafers were already ordered with correction in single layer
- Waiting for corrected ASICs

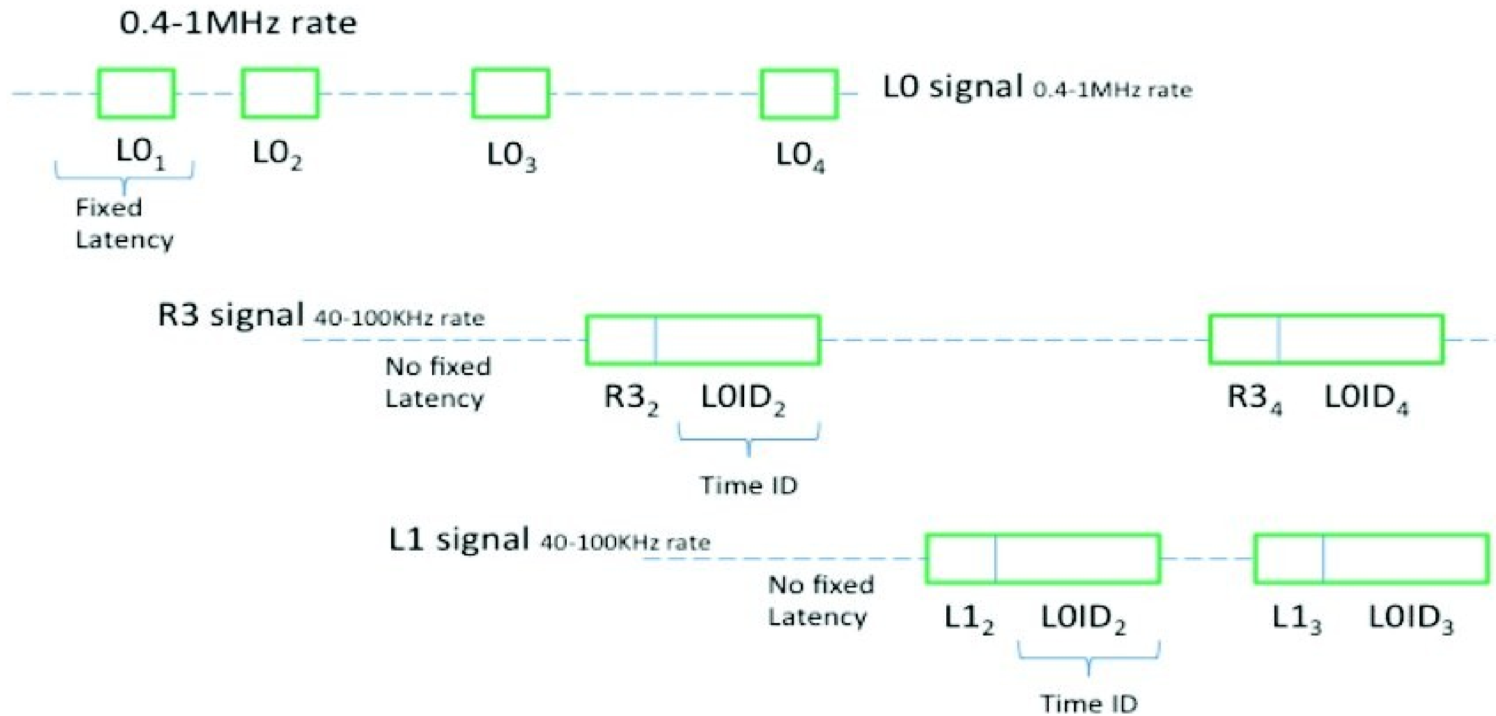
Backup slides

HCC Block Diagram

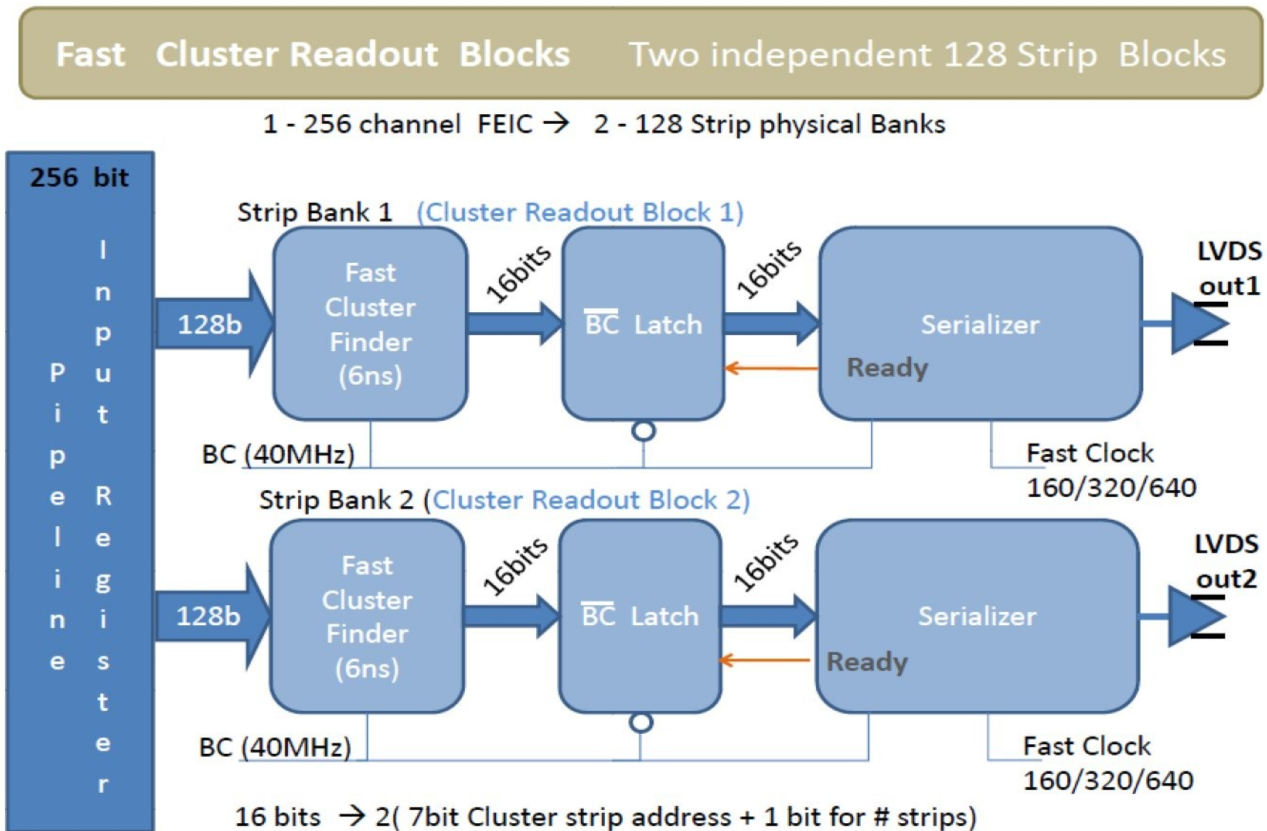


Mar 2012

Example of Triggers Sequence



FCF block diagram



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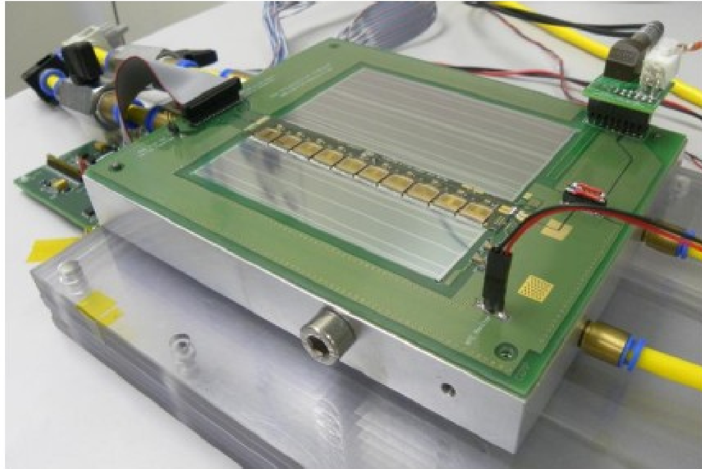
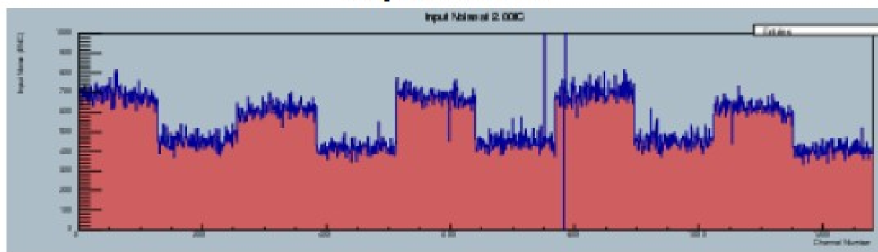
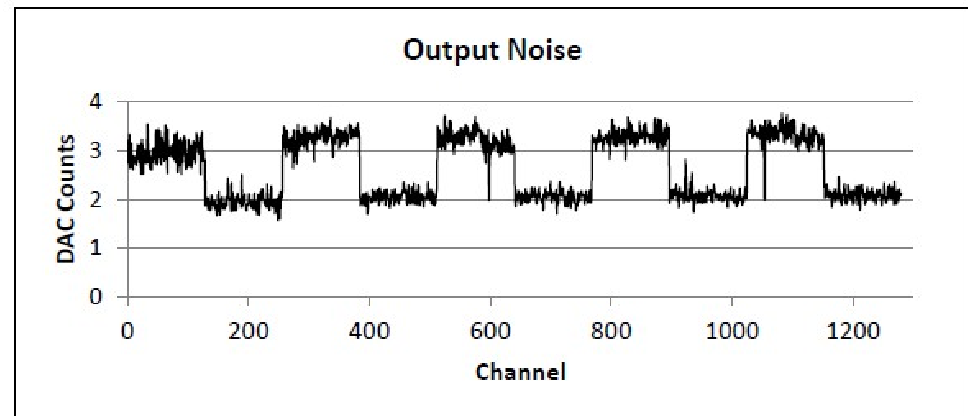
FIB Module – Part Bonded to Sensor



- First test with 2 lower rows of front-end bonded to sensor
  - Sensor strips under hybrid bonded to ALL asics
    - Upper rows left open-circuit
- No problems wire-bonding from asics to sensor
  - Benefit of collaborating with asic designers to 'fix' geometry
- Sensor biased to -250V
  - Thybrid (powered): 16ºC (was 15ºC unpowered)
- Bonded/un-bonded channels clearly visible in both input/out noise plots
- But, again input noise is high and gain is low
  - Un-bonded I/P noise: 440e (as seen for un-bonded hybrid)
  - Bonded I/P noise: 661e (expected 520e-550e)

Input Noise





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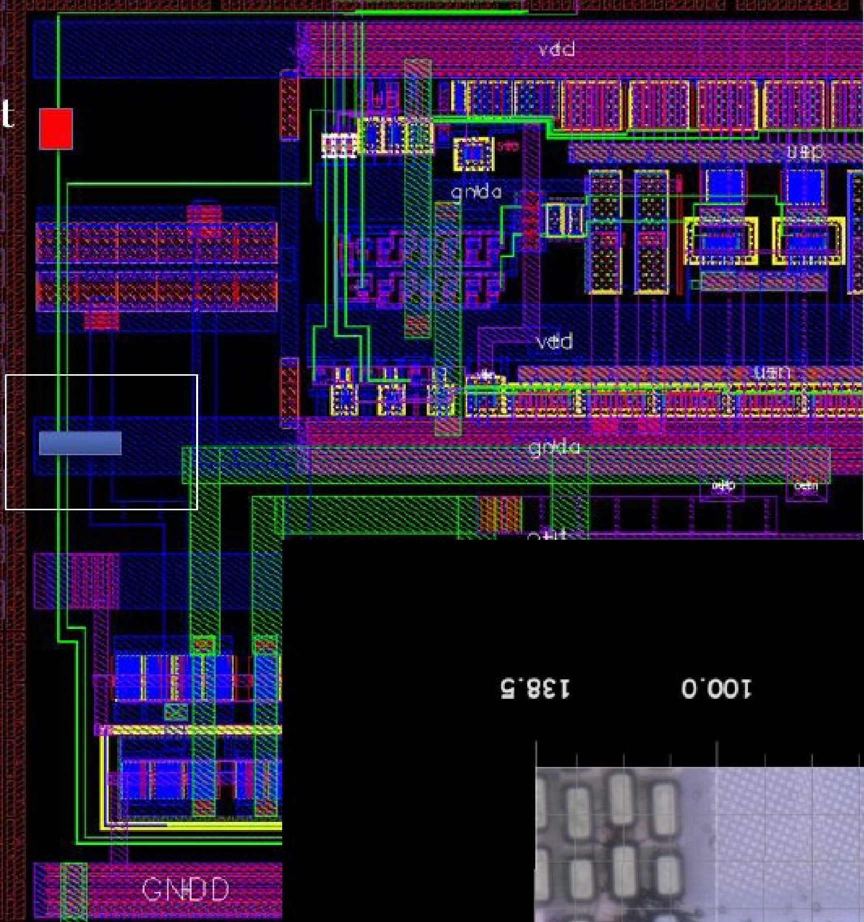
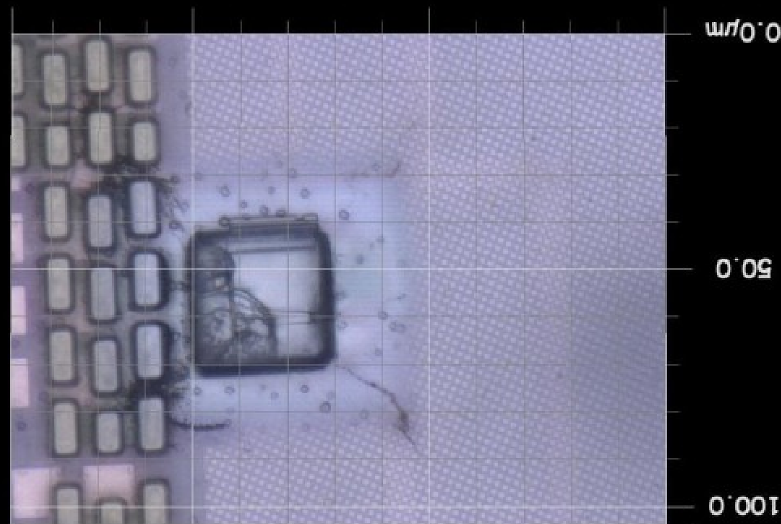
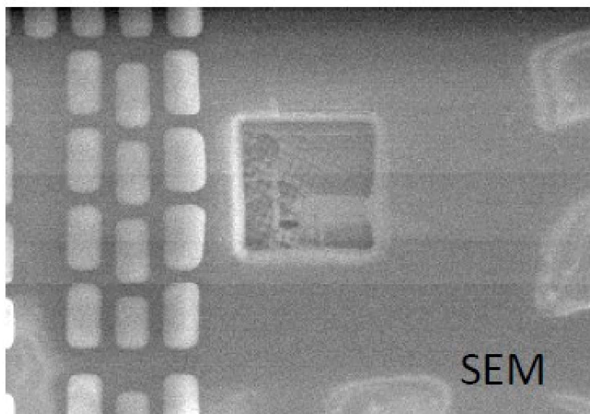
FIB Hybrid - Summary

- Prototype hybrid with 10 x ABC130s has been shown to work successfully
  - Able to configure devices
    - All LDO's programmed to ~1.2V
    - On board termination working
  - Serial readout chain of "FIB'd" devices operating at 80MHz shown to pass data correctly
    - Allowing characterisation of Front-end analogue performance
- Power Consumption better than specification
  - FDR predication was 92mA/ABC130
  - Measured is ~80mA
- No evidence of instability at low charge injection (1fC)
  - DTN not yet performed – better indicator
- Output noise in agreement with expectation but "gain" is low
  - Using analysis adopted for ABCN-25 (and ABCD) chipsets
  - Still to be understood but points to calibration circuit and or procedural error
  - Ideally would like to crosscheck by use of external calibration source (laser, radiation, etc.)

DATAR -> Driver







Full functionality restoring

Status :

- All layout changes (M3 layer only) done
- All verifications (DRC LVS) on full chips (ABC130_0 and ABC130_1) done
- XOR with old layout database (gds) show changes only on M3
- New GDS (ABC130_0_V2 and ABAC130_1_V2) delivered to IBM foundry through the CERN microelectronics service.
- 6 "respin" wafers ordered
- Delivery expected in ~40 days (?)