Towards a 3D-AGIPD

Alessandro Marras

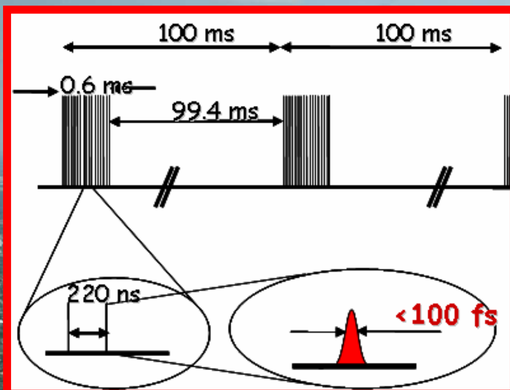
on behalf of the DESY Photon Science–Detector Group

Outline

- The goal and the obstacles to overcome
    - 3DIC: a possible path to the solution
- design and test of 2-tier detector prototype
    - TSVs & tier-to-tier contacts
    - vertically integrated test circuits
    - 16x16 array of vertically integrated pixels
- Conclusion

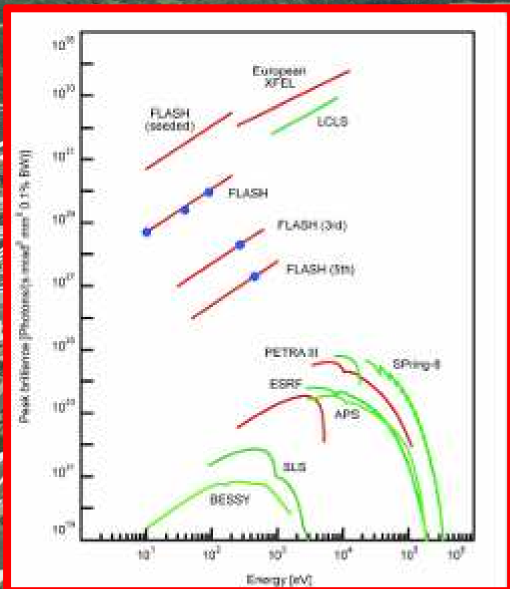
The Motivation

The Motivation



2700 pulses @4.5MHz every 100ms

352 images storing capability

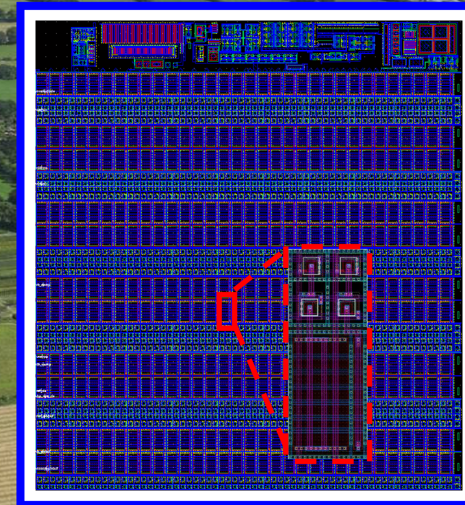


challenging radiation environment

rad tolerant design mandatory

spatial resolution desiderata

200um pitch



A possible solution (long term goal)

1) bump-bond to the detector

tech #1
(CMOS Low Pow)

2) amplification &
double sampling

5) digital
signal
readout

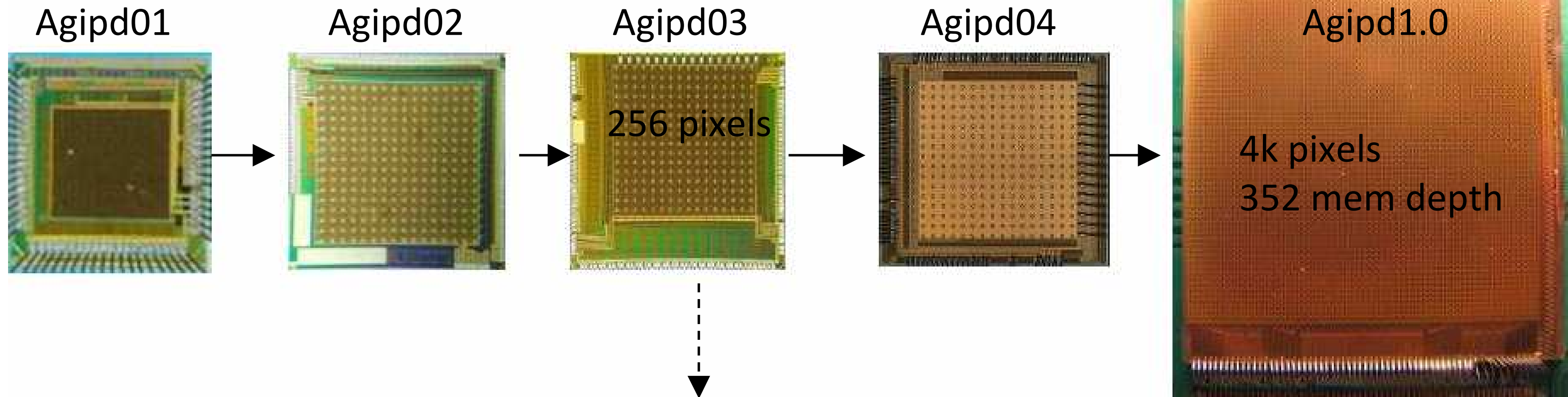
tech #2
(CMOS High Perf)

3) ADConversion

tech #3
(DRAM)

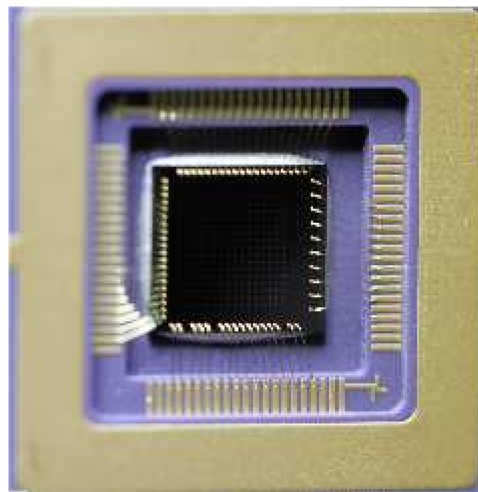
4) store the digitalized signal
in a digital memory cell (on
multiple layers)

A path toward the solution



GF 130nm CMOS Low Power
ARM SC library
Tezzaron FaStack
double-tier

T13C11 MPWrun, via CMP
submitted 2011
delivered Jan 2014



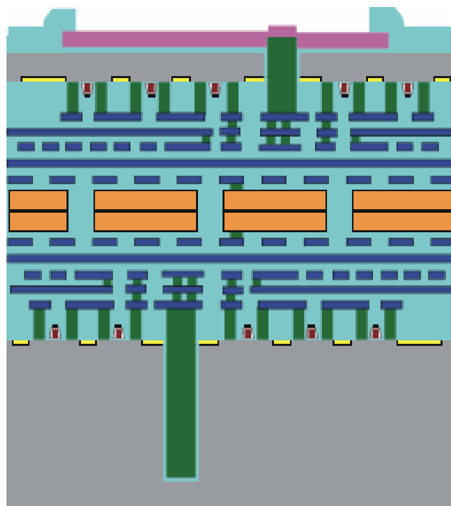
3D-Agipd investigation 01

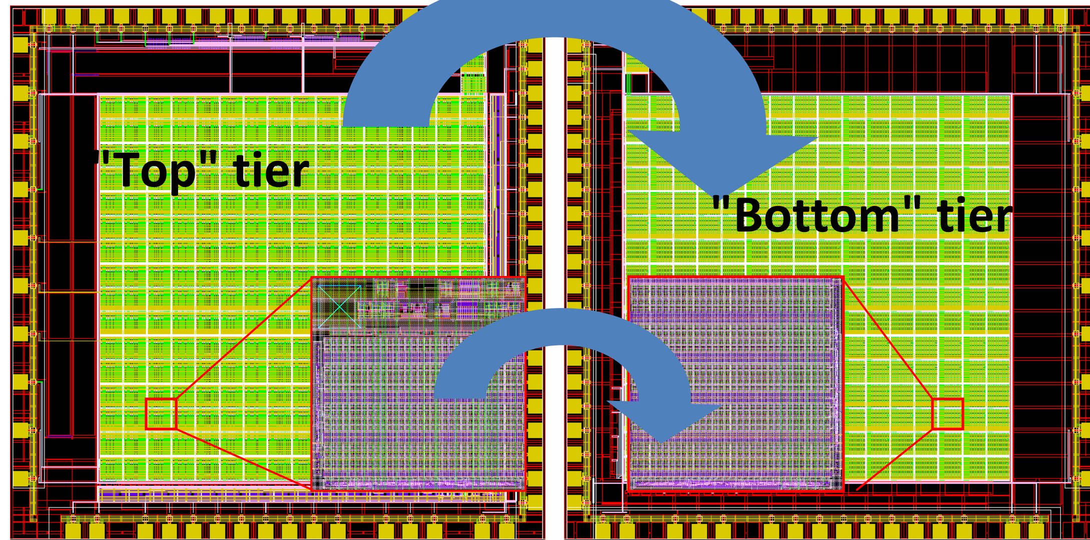
test structures +
256 pixels matrix
200um pitch
544 mem depth

simplified architecture: fixed gain (but reserving the space for multiple-gain circuits; equivalent memcell area)

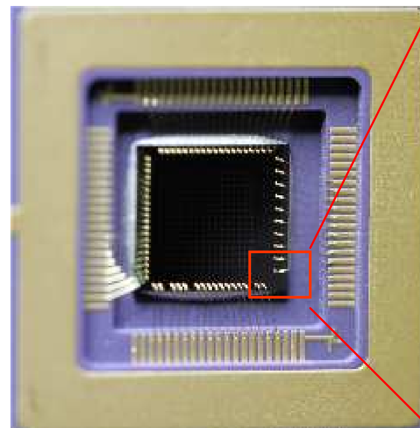
The concept at a glance

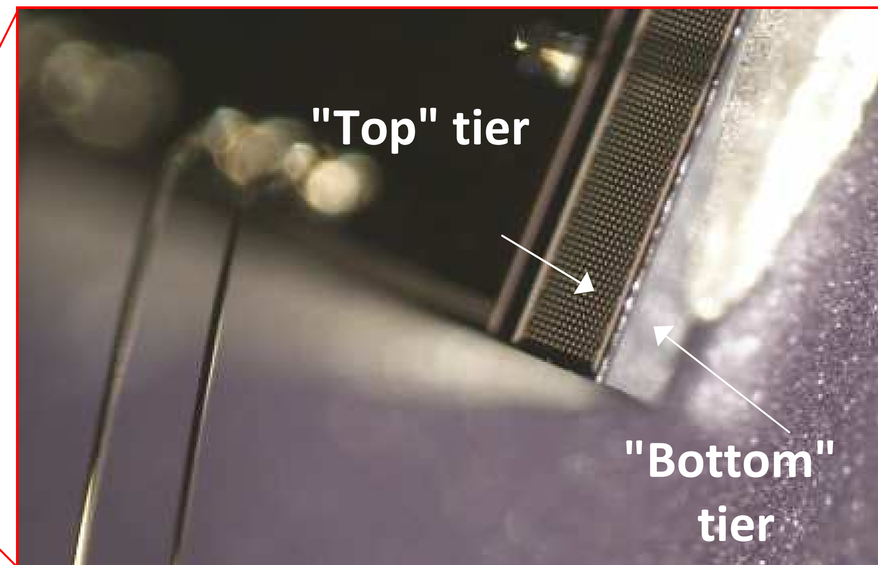
Tezzaron process used





- 2x planar chip manufacture
  - via-middle TSVs
- stacking and face-to-face coupling
- back-grinding of the top tier and exposition of the TSVs
- Pad definition





The concept at a glance

1) bump-bond to the detector

2) amplification & double sampling

3) store the analog signal in a memory cell in the appropriate layer

4) signal readout

same tech (CMOS Low Pow)

x224

x320

x544

pixel architecture

chip architecture

Test summary

chip #	daisy chains (TSV & tier-to-tier)	2D test circuits	single pixel test struct	16x16 matrix (CDS stage input)	power consumption
	Top&Bottom tier	Top tier	Top&Bottom tier	Top&Bottom tier	
1	unbroken	not responding	not responding	not responding	3.75 mW
2	unbroken	responding	not responding	not responding	24.75 mW
3	unbroken	not responding	responding	responding	31.05 mW
4	unbroken	responding	responding	responding	24.3 mW
5	unbroken	responding	responding	responding	26.25 mW
6	unbroken	responding	responding	responding	30.15 mW
7	unbroken	responding	responding	responding	30.9 mW
8	unbroken	responding	responding	responding	31.2 mW
9	unbroken	responding	responding	responding	26.7 mW
10	unbroken	responding	responding	responding	30.0 mW

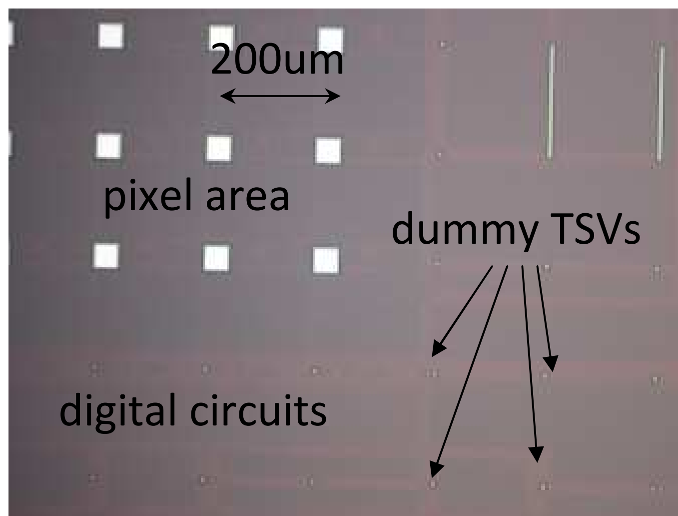
as expected	unexpected

TSV contacts evaluation

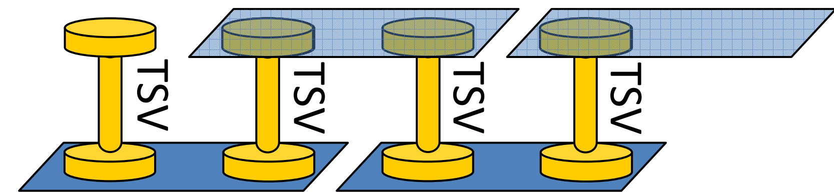
"via middle" TSVs Ø 1.2 um , landing on M1

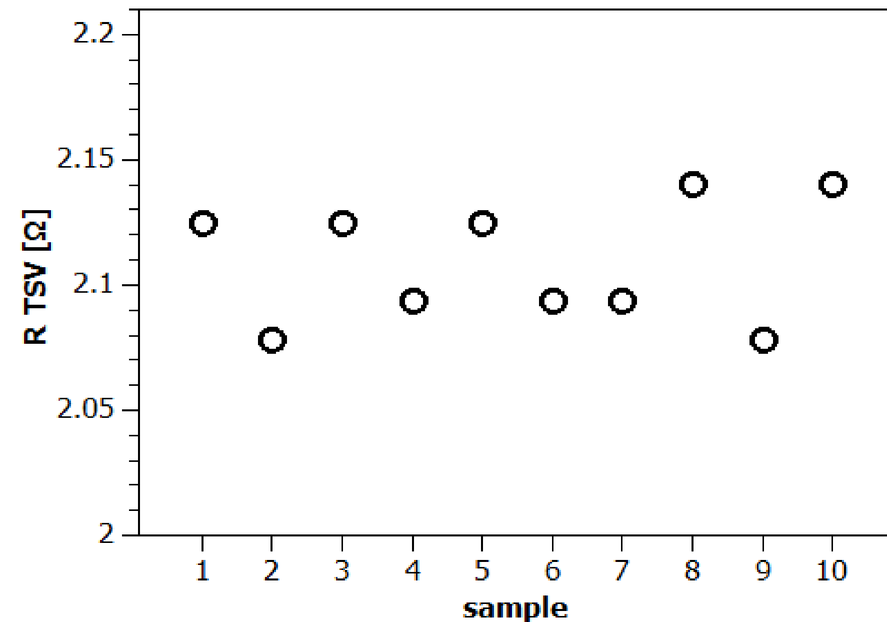
locally: TSV-to-TSV distance down to ~4um
however, globally: "uniform" density of TSVs recommended (→ uniform resistance to grinding)

→ designer constraint: dummy TSVs



test structure for TSV evaluation: daisy chain of 64 TSVs, by connected M1/backM.

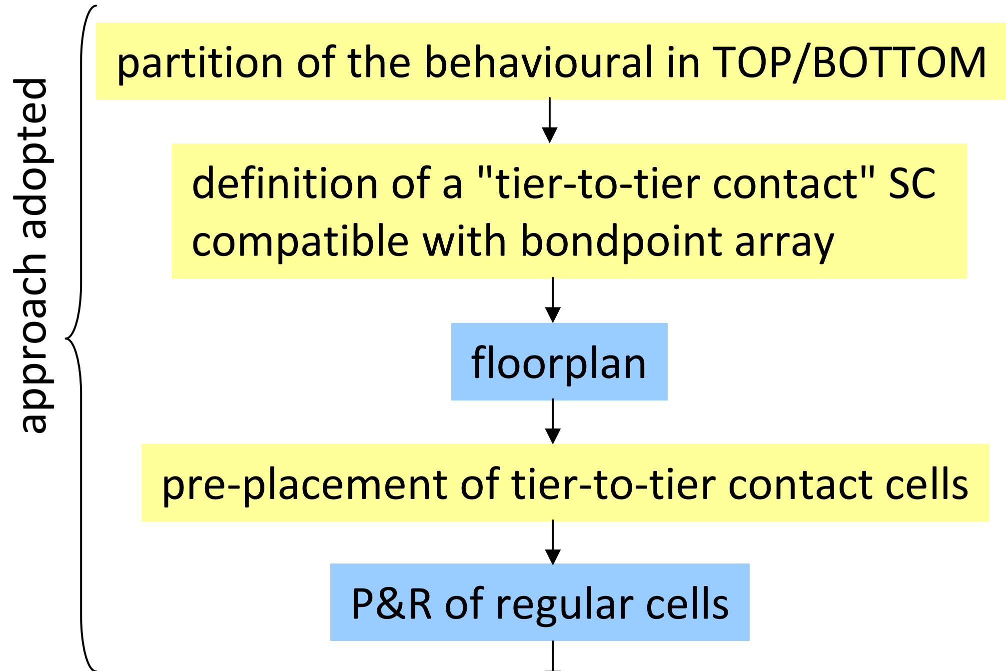


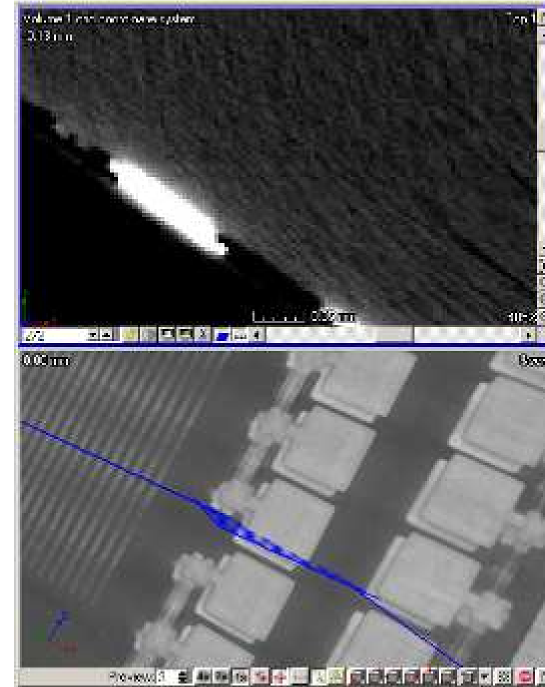


measured on 10 packaged samples
no broken chain, avg R 2.1Ω /TSV

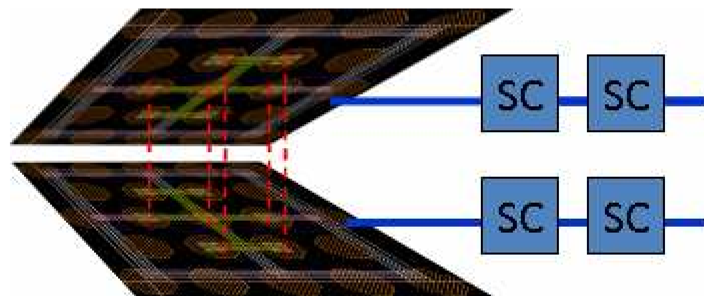
Tier-to-tier contacts

Cu-bondpoints (M6) used for tier-to-tier connectivity



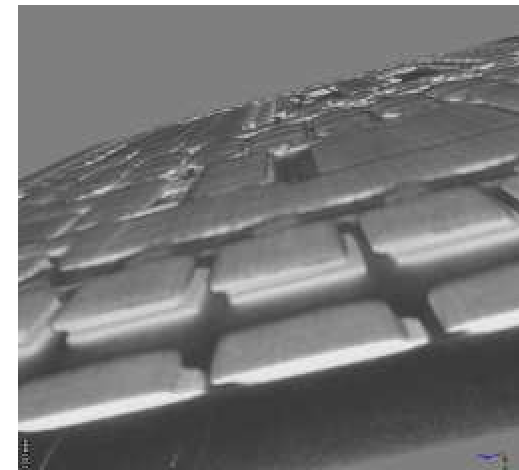


M^{3}APS (courtesy of INFN-Perugia)
submitted end 2009
Tomography by F. Beckmann (DESY)



tier-to-tier contact redundancy was suggested by 2009 MPW experience, to counter eventual tier misalignment ,

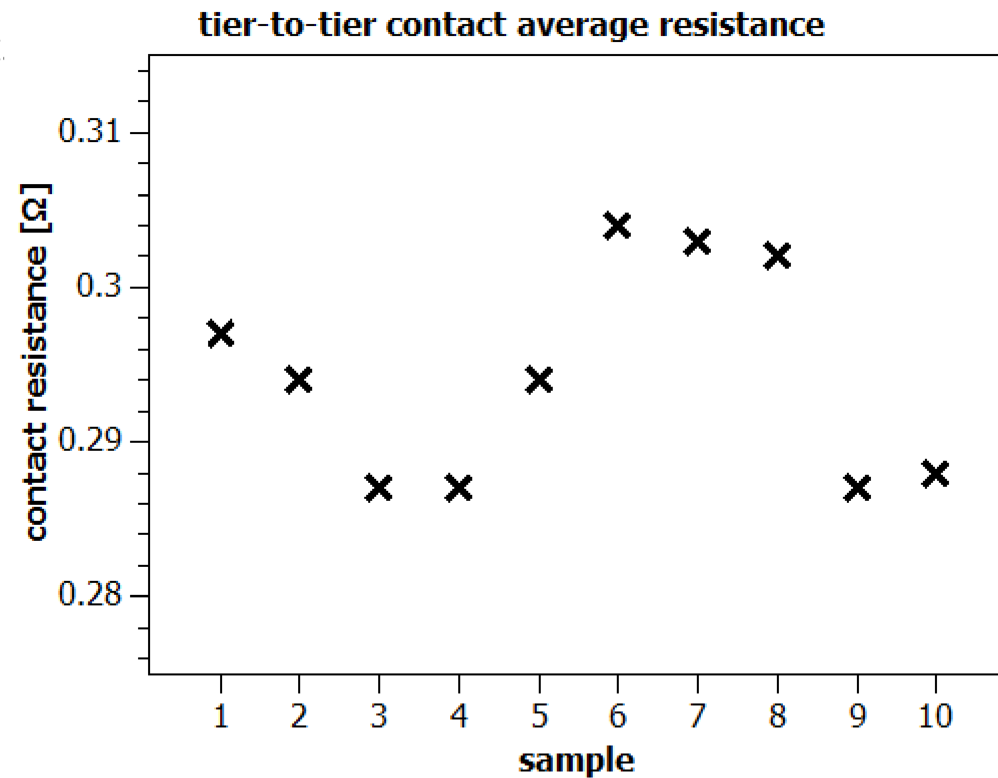
however ...

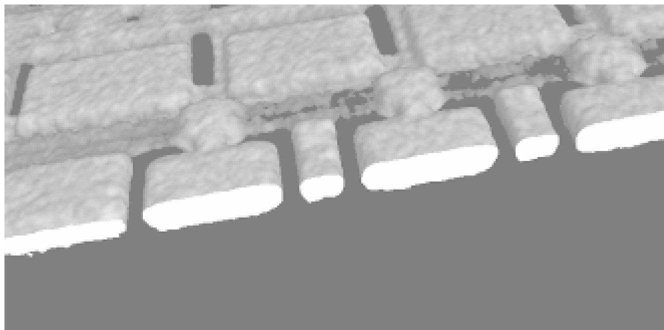


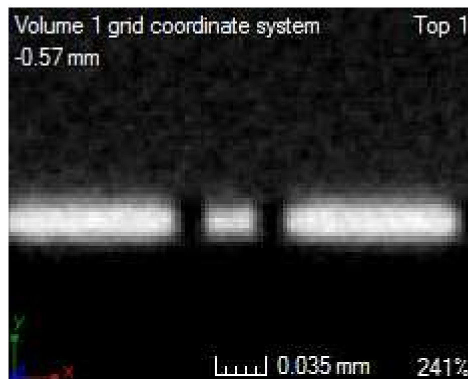
Tier-to-tier contact evaluation

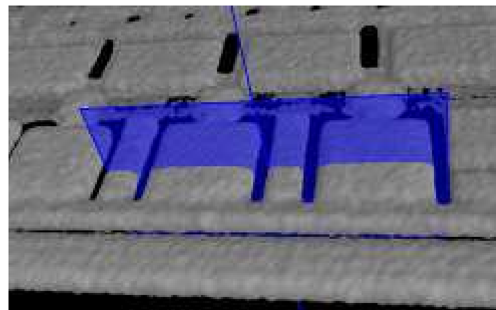
test structure for contact evaluation:
daisy chain of 1000 tier-to-tier contact
connected in series using M5.

measured independently
on 10 packaged samples
no broken chain



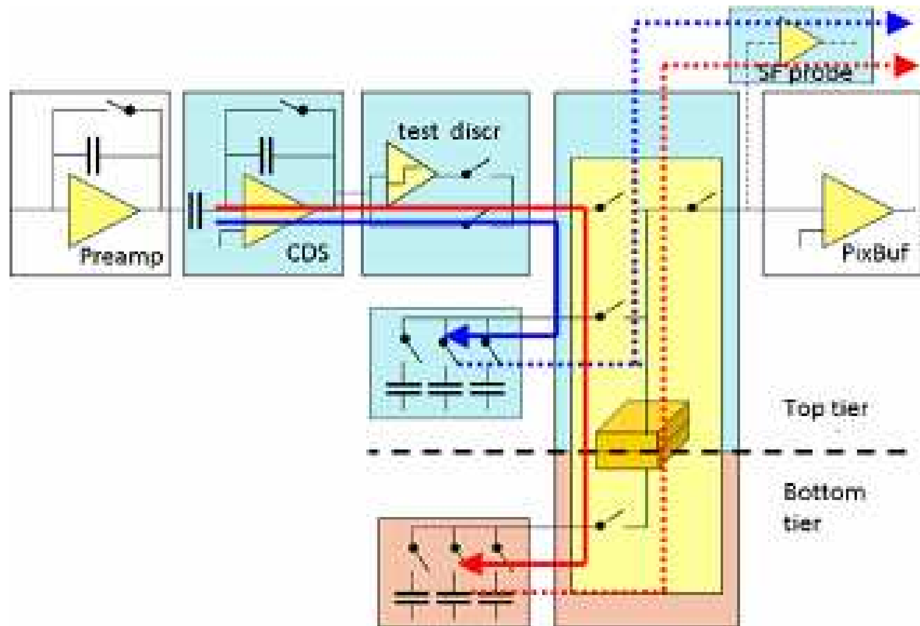


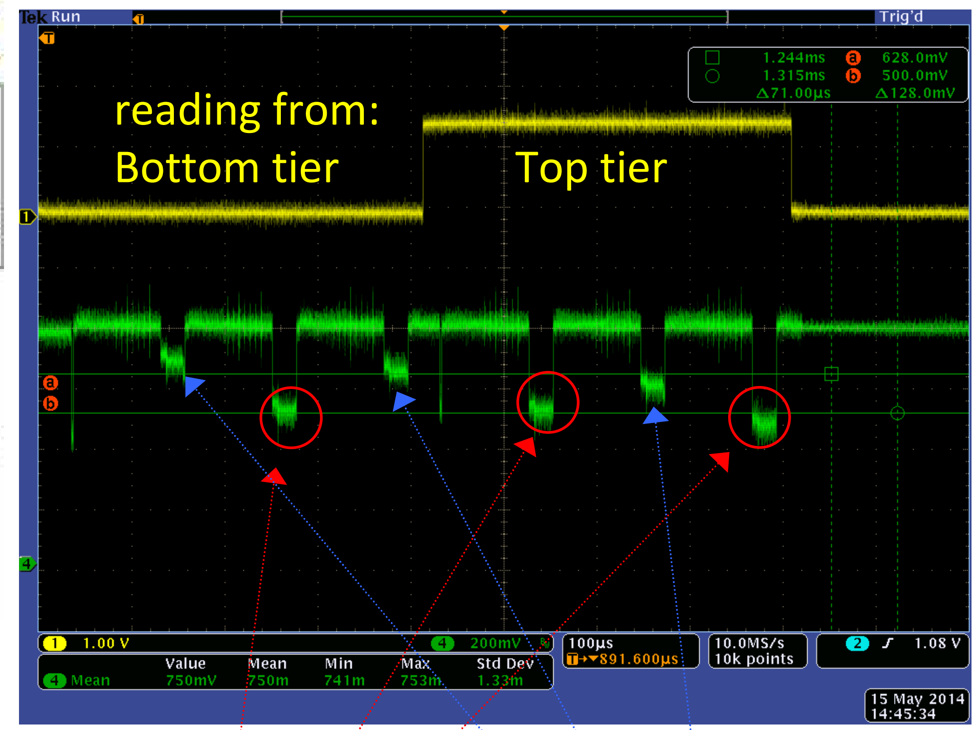




x-ray tomography (F. Beckmann, DESY) also suggest better alignment

Single pixel write-read example





precharge cells

write voltage on cell blocks on Bottom, Top tier

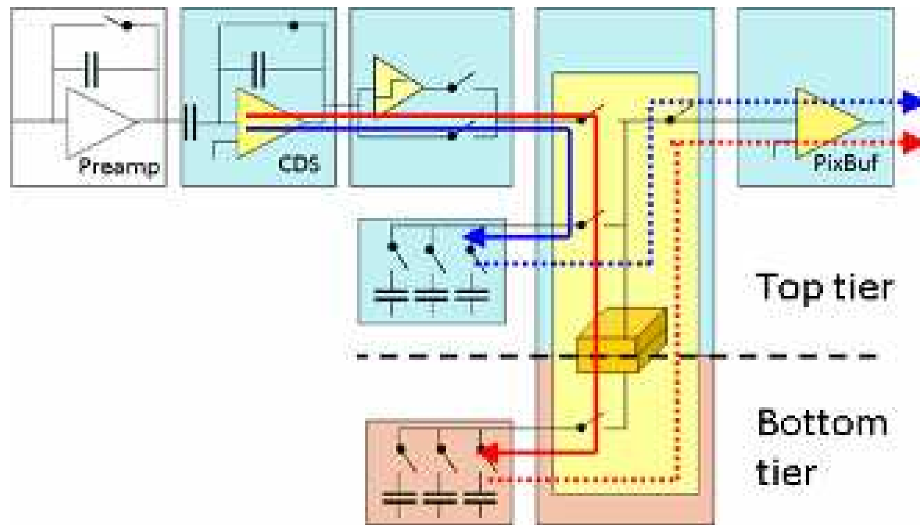
connect cell group to memory bus and probe voltage

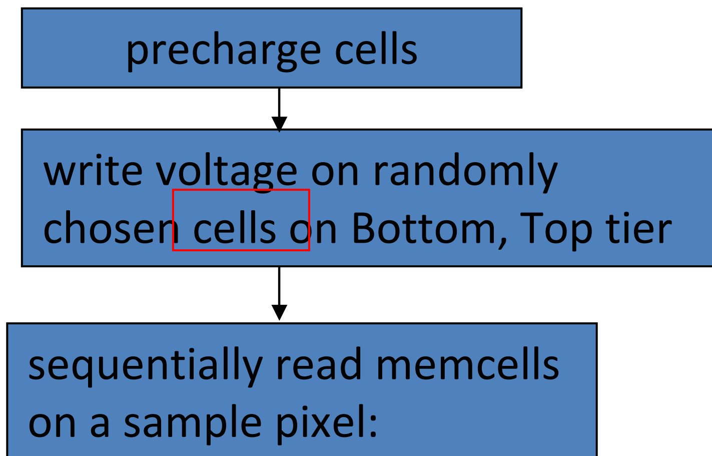
sequential readout of storage cells:

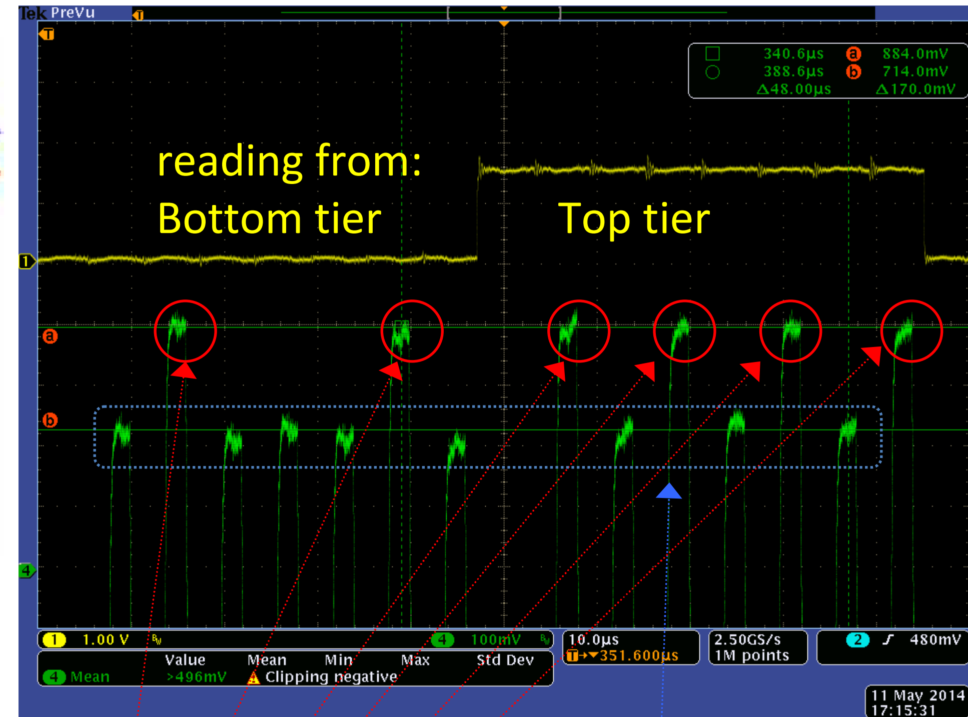
storing a voltage written by CDS stage

storing the precharged voltage

Pixel matrix write-read example





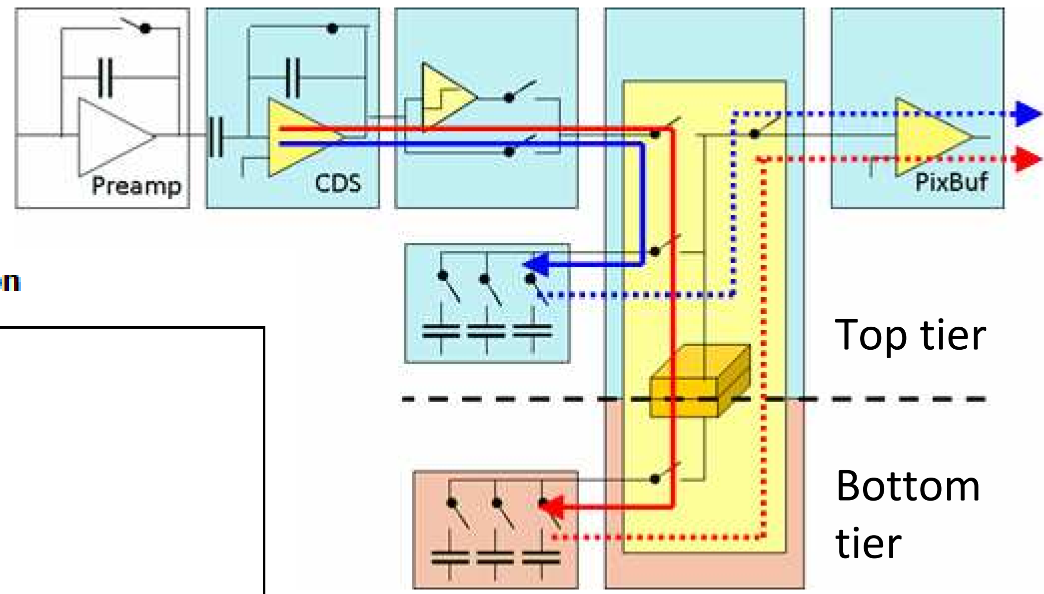


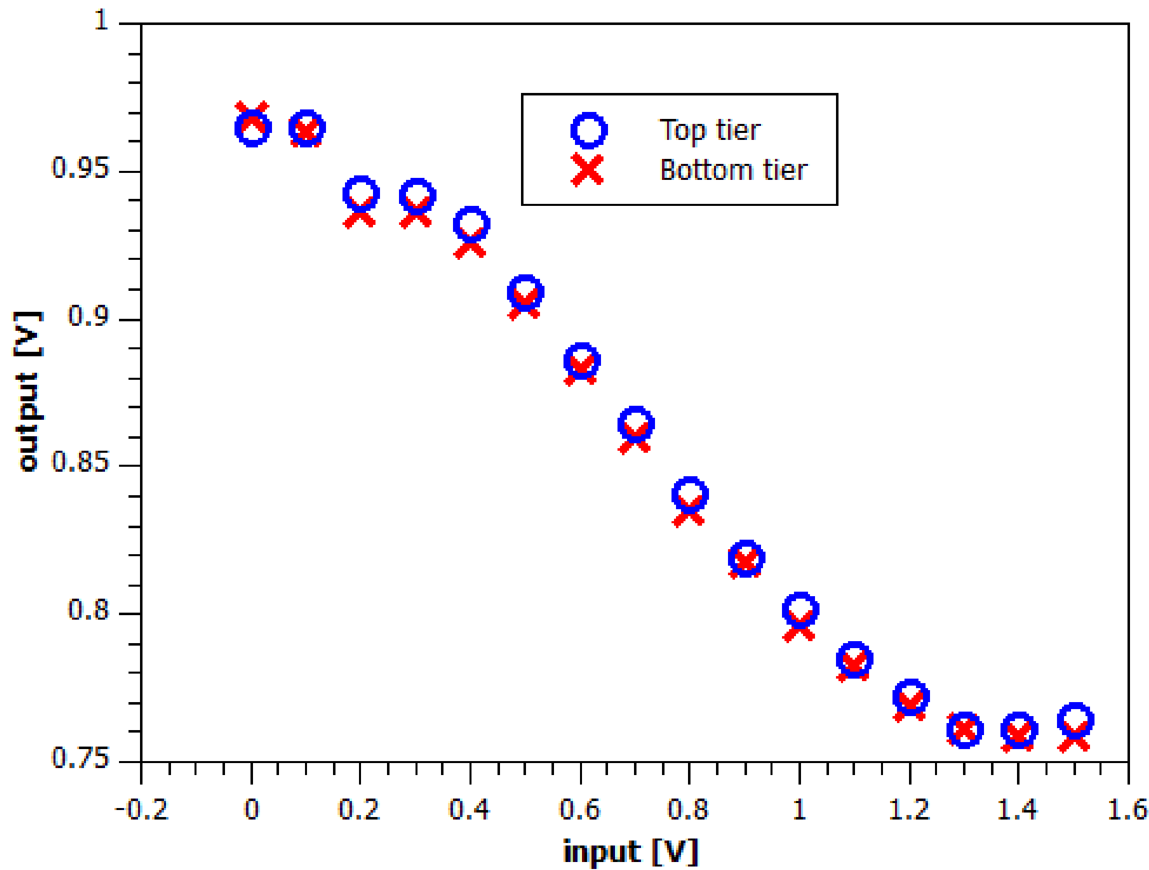
sequential readout of storage cells:

storing a voltage written by CDS stage

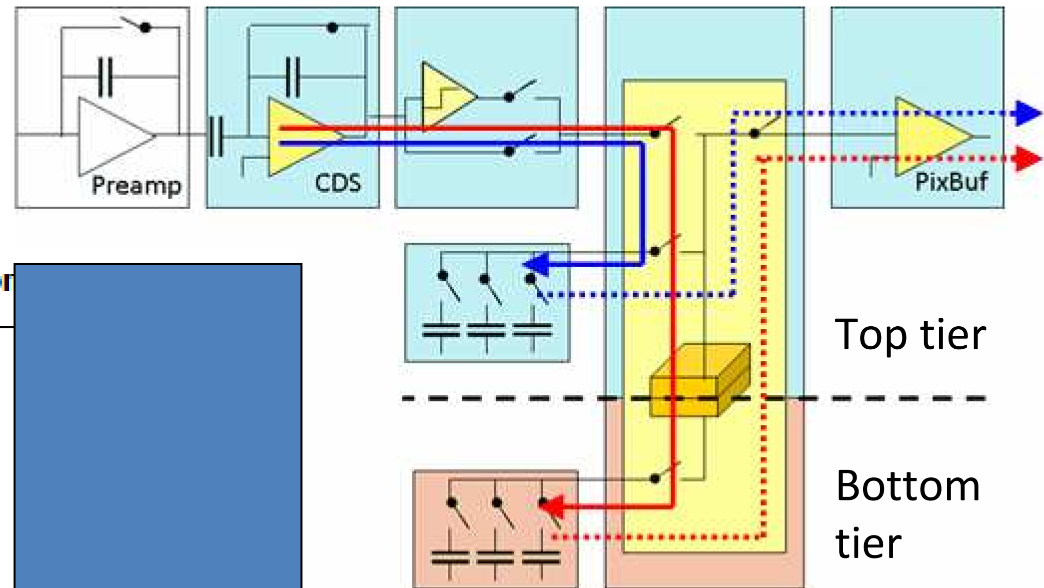
storing the precharged voltage

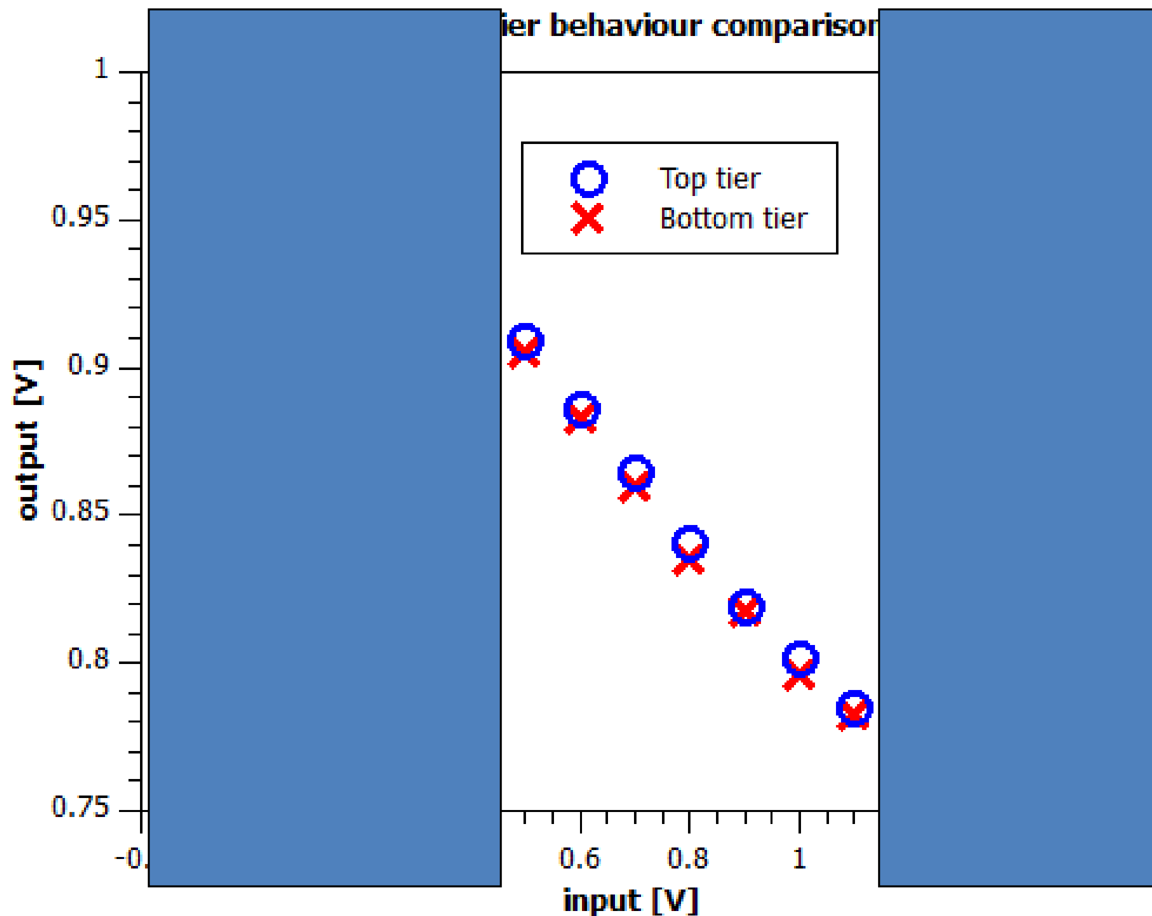
Behaviour comparison of Top/Bottom tier storage cells





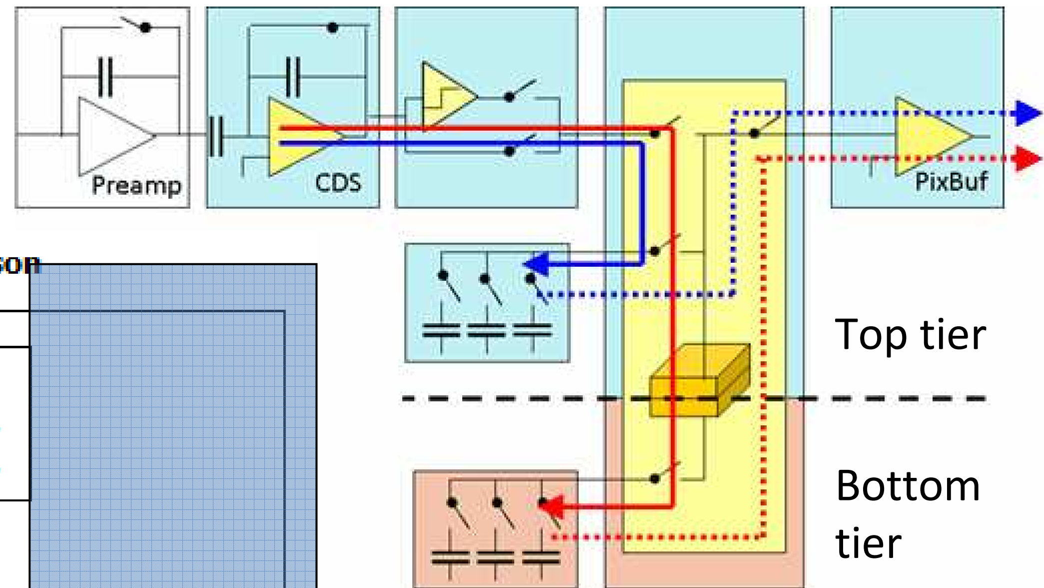
Behaviour comparison of Top/Bottom tier storage cells

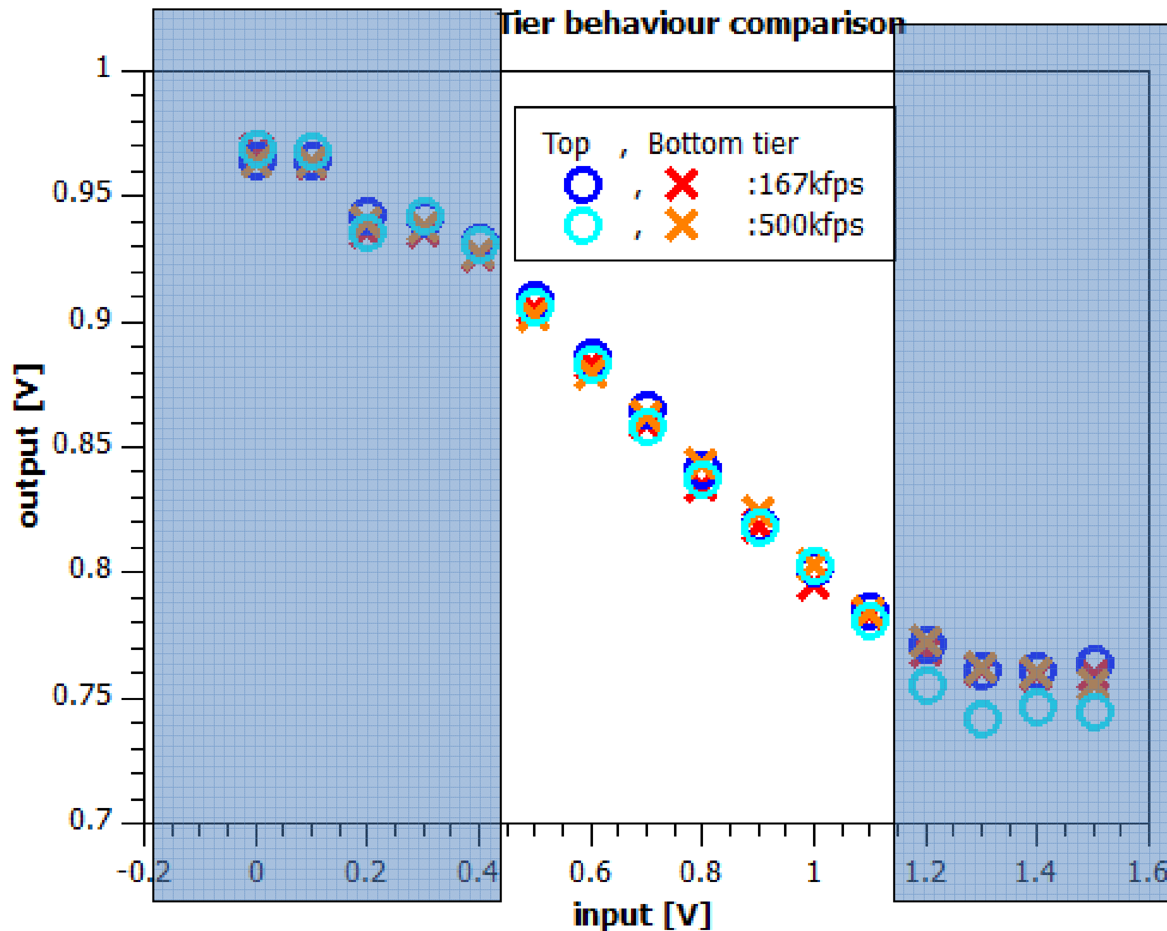




expected operation region of the circuit: comparable (linear) behaviour of the detector output, whether the charge is stored in/read from storage cells located on the Top tier or Bottom tier

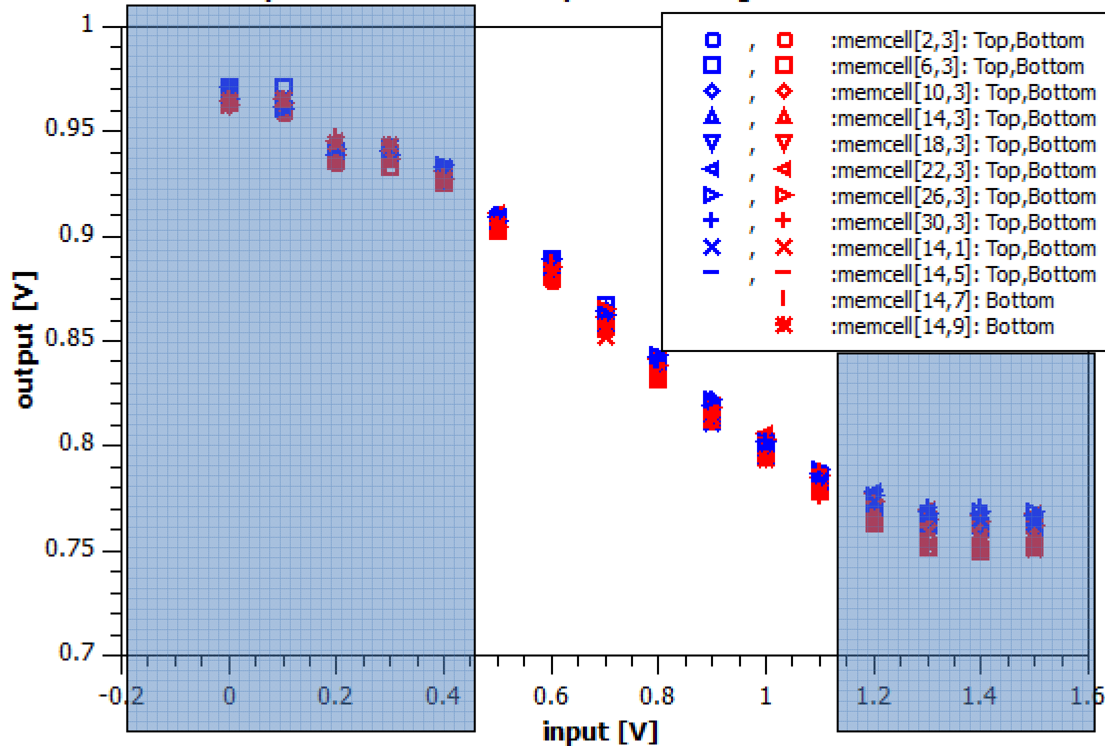
Behaviour comparison of Top/Bottom tier storage cells



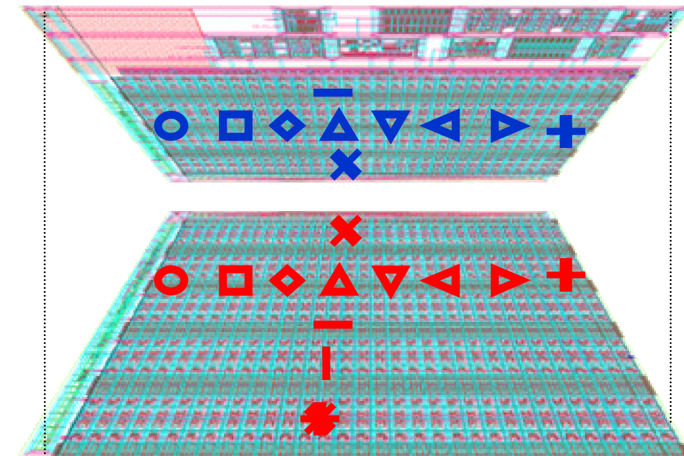


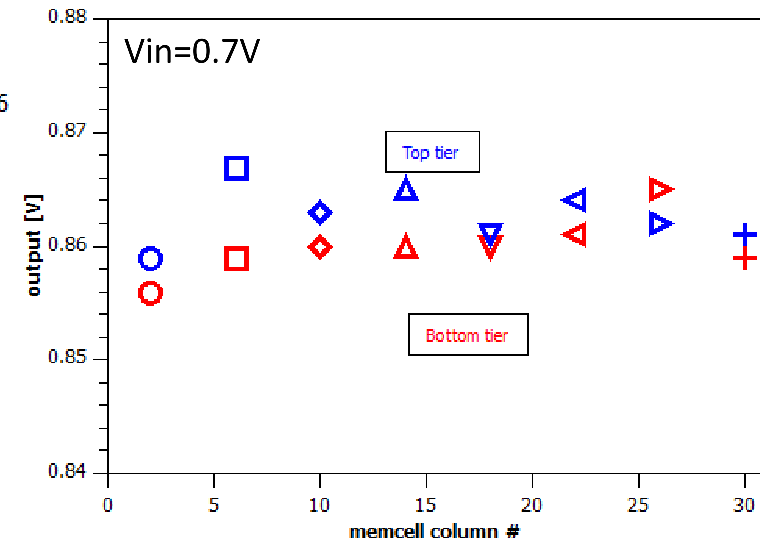
tested up to 500kfps (limit of current test setup, to be improved for 4.5Mfps test)

Top/Bottom tier: memory cell-to-memory cell variations



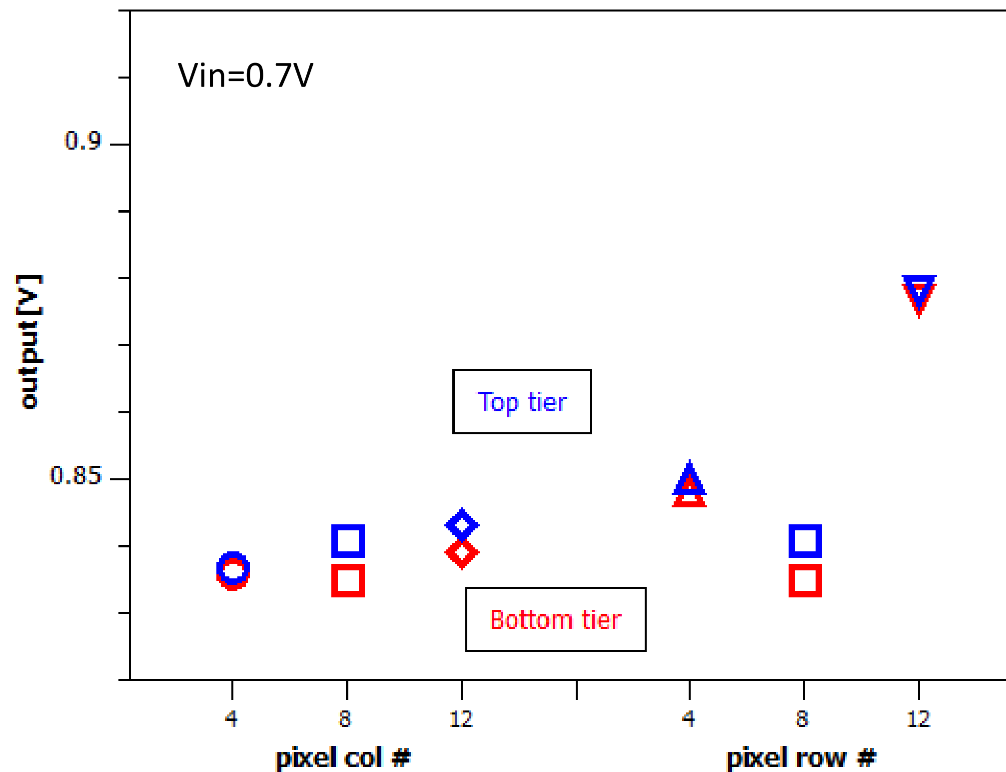
1 pixel in the array

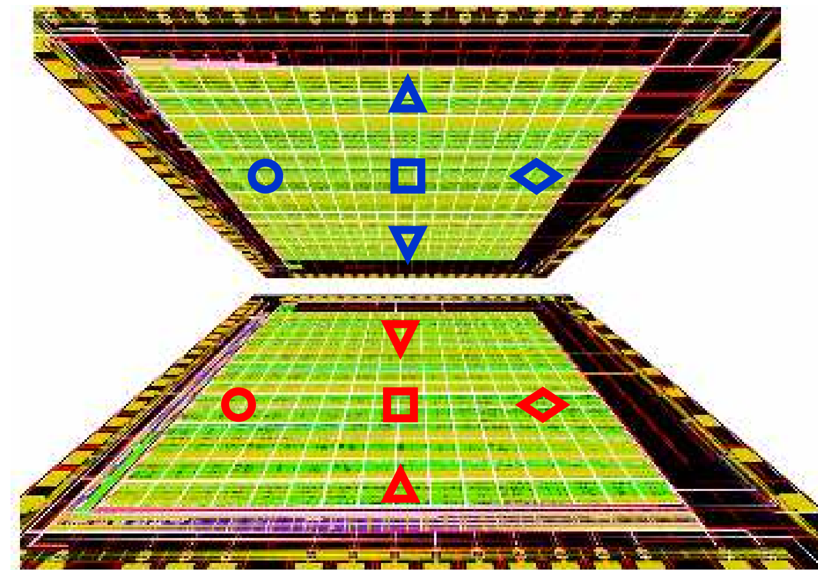




Similar trend (comparable linear behaviour) observed for different memory cells in the same pixel, independently from their location.
There seems, however, to be a slight pedestal offset between the two sets.
To be investigated further

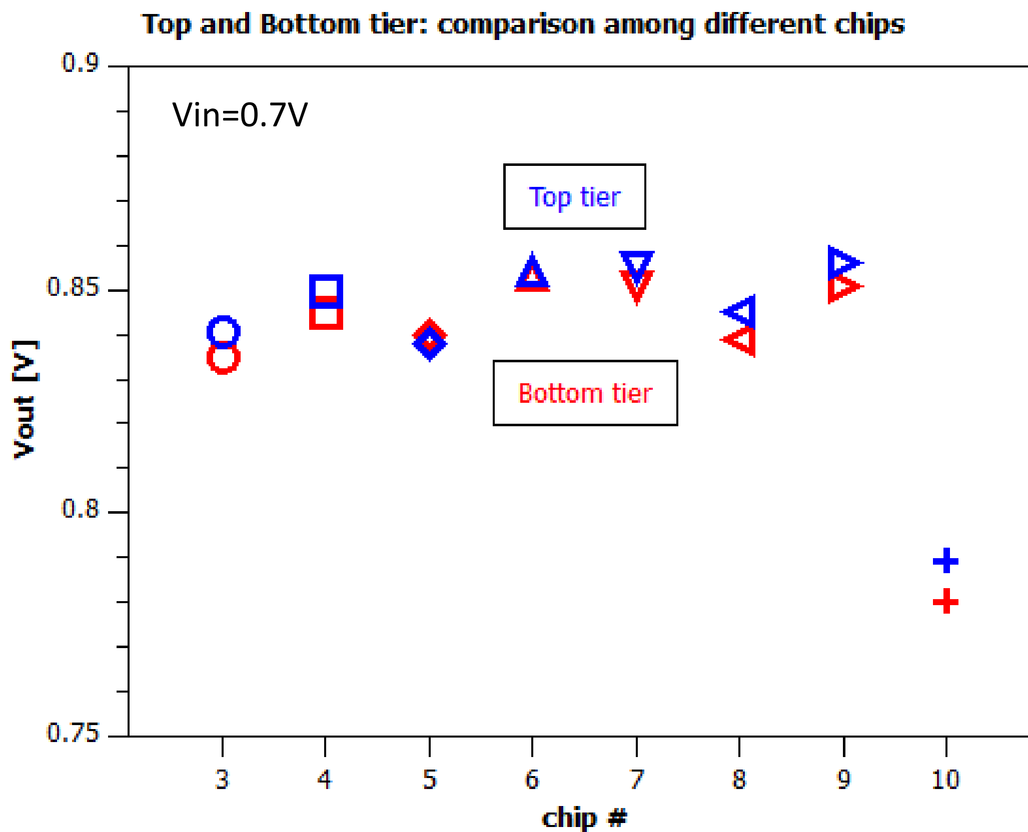
Top/Bottom tier: pixel-to-pixel variations

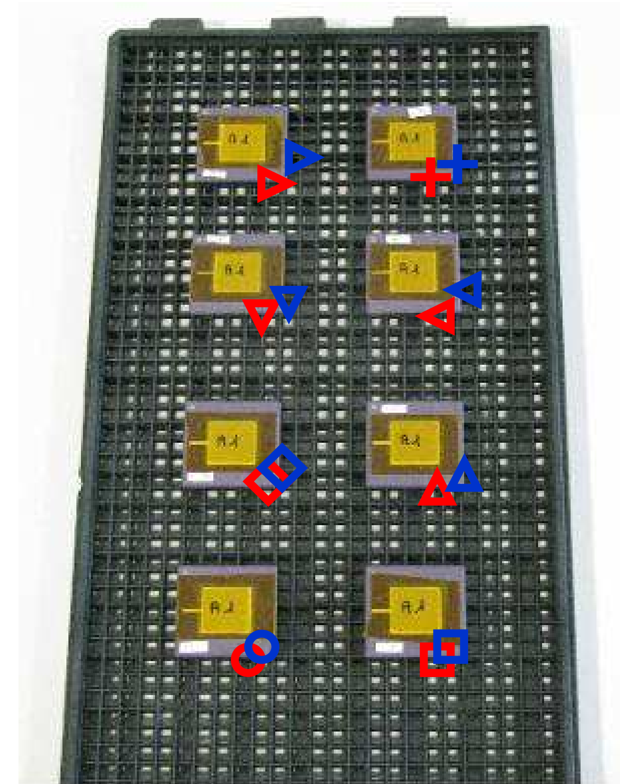




Output coming from different pixels may have more marked variations.
However, outputs from memory cells in the Top/Bottom tier of the same pixel remain similar. Process parameter dispersion in the active pixel circuitry is suspected.
Per-pixel calibration will in any case be needed

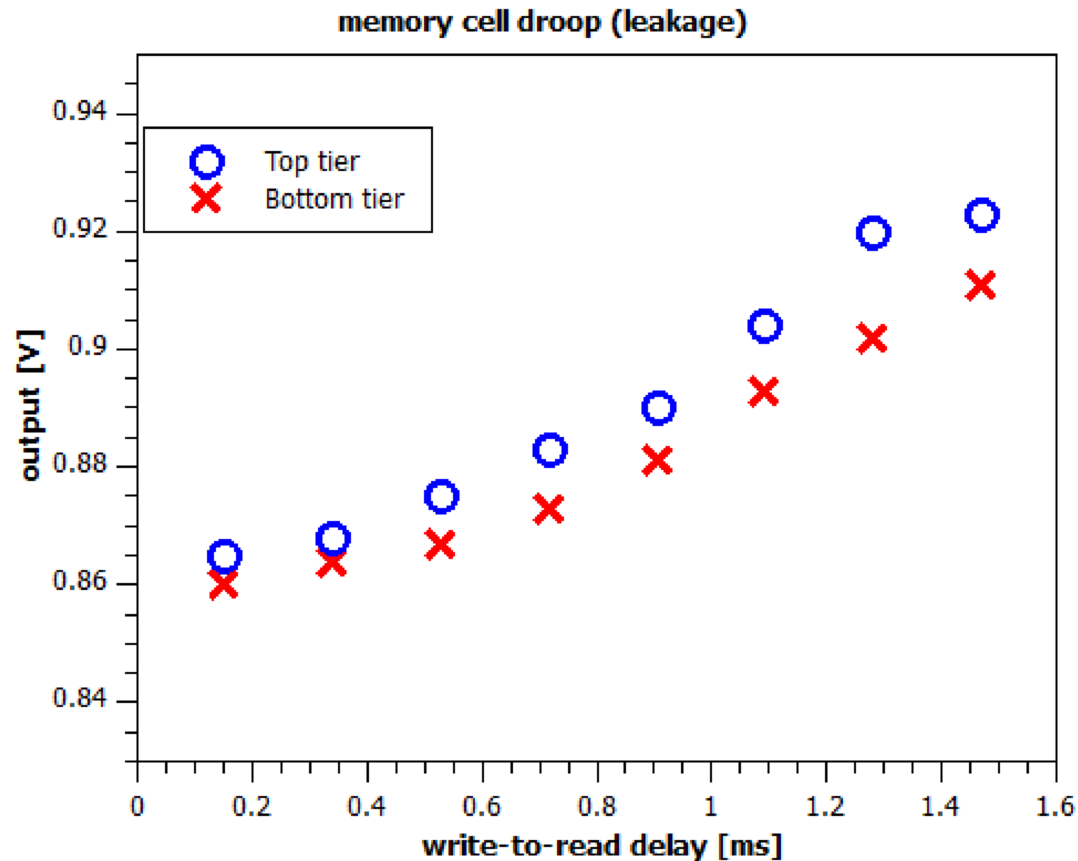
Top/Bottom tier: chip-to-chip variations





Comparison between outputs coming from different chips follows the same trend
Output coming from different chips may have marked variations, but outputs from memory cells in the Top/Bottom tier of the same pixel/chip remain similar.
Process parameter dispersion in the active pixel circuitry is suspected.
Per-chip calibration will in any case be needed

Open issue: charge leakage



significant parasitic leakage of charge stored in memory cells

Memory cell layout to be optimized
Temperature dependence to be investigated

Conclusions and future work

Extending photon science detectors in the third dimension:

- the 3D-AGIPD case

Prototype produced: T13C11 3DIC MPW run (through CMP)

- GF130nm tech, Tezzaron 3D-process, 2 tiers, face-to-face
- 256 pixel array (200um, 544 images memory depth) + test structures

First evaluations

- good TSV, tier-to-tier contact characteristics
- 7(8)/10 working samples
- pixel array working
- able to store/recover info both Top/Bottom tiers

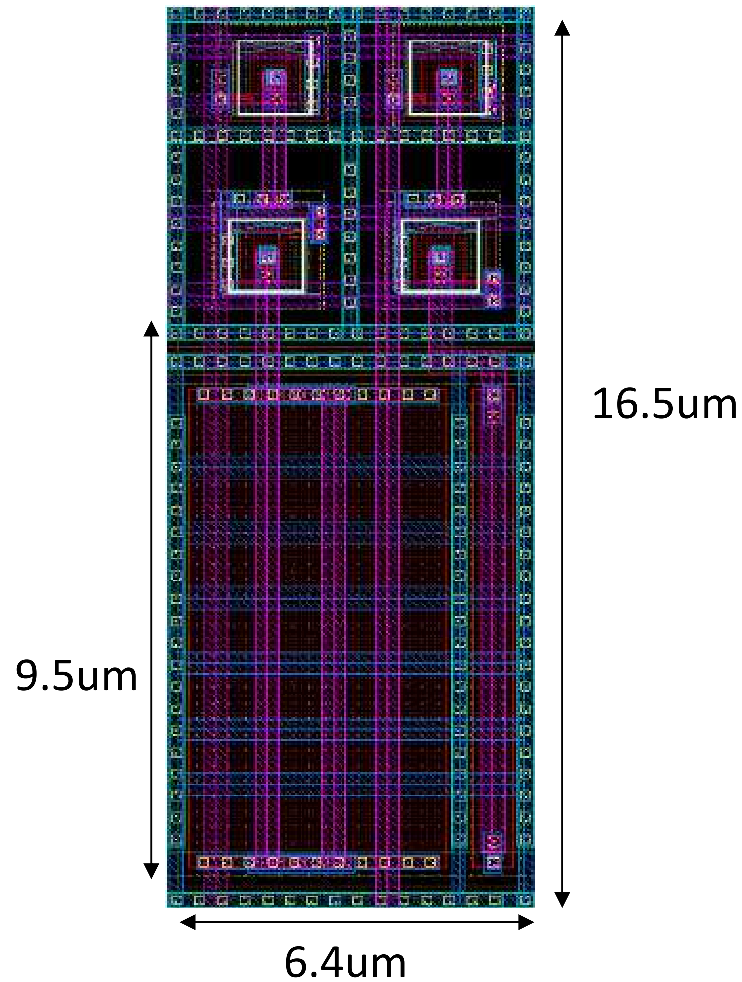
Open issues:

- investigation/mitigation of performance dispersion among different cells/circuits/chips
- investigation/mitigation of storage cell leakage

Backup

memcell comparison

AGIPD1.0 (2D)



3D-Agipd investigation 01