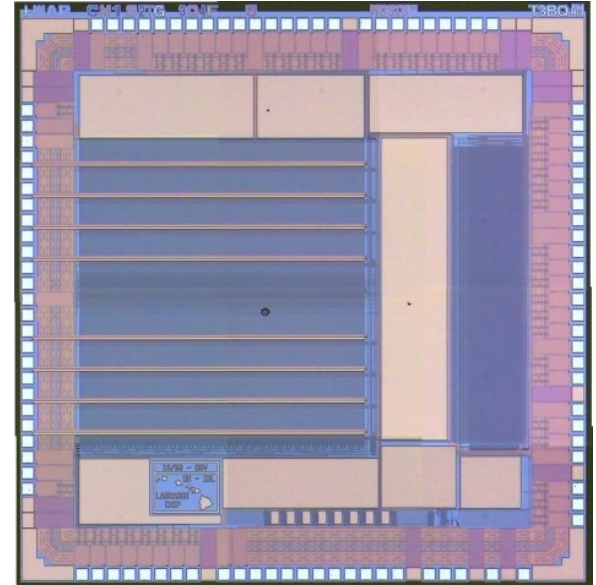


Deep-Sampling CMOS Digitizers



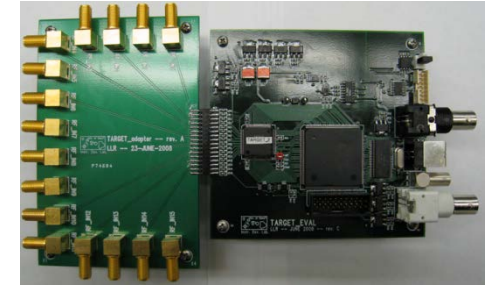
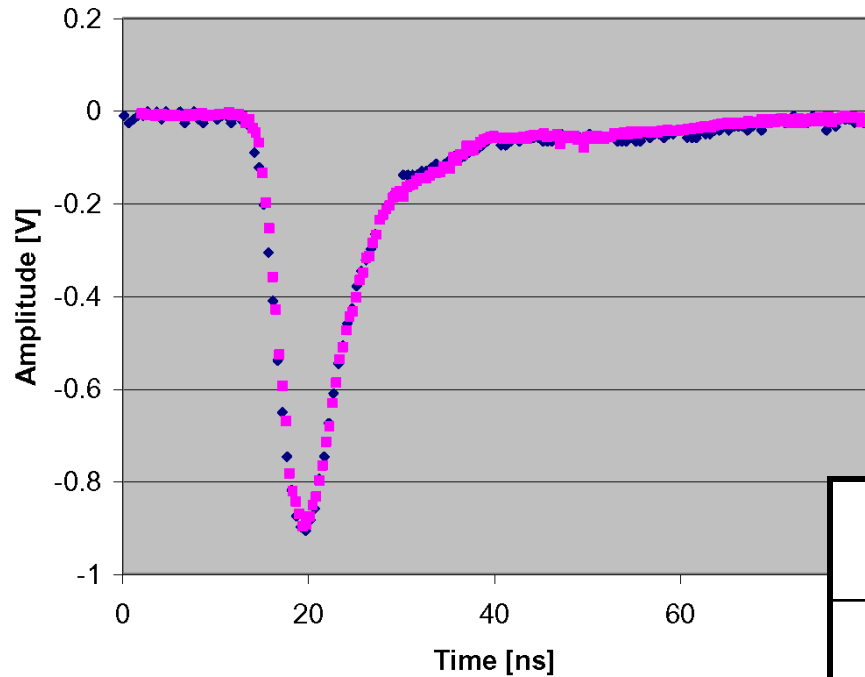
Gary S. Varner
University of Hawai'i
22 MAY 2014



Front End Electronics (FEE 2014)

The Initially Selling Point

PMT pulse comparison



- 2 GSa/s, 1GHz ABW
- Tektronics Scope
- 2.56 GSa/s LAB

	WFS ASIC	Commercial
Sampling speed	0.1-15 GSa/s	2 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	$\leq 0.05W$	Few W
Cost/Ch.	$< \$10$ (vol)	$> 100\$$

“oscilloscope on a chip”

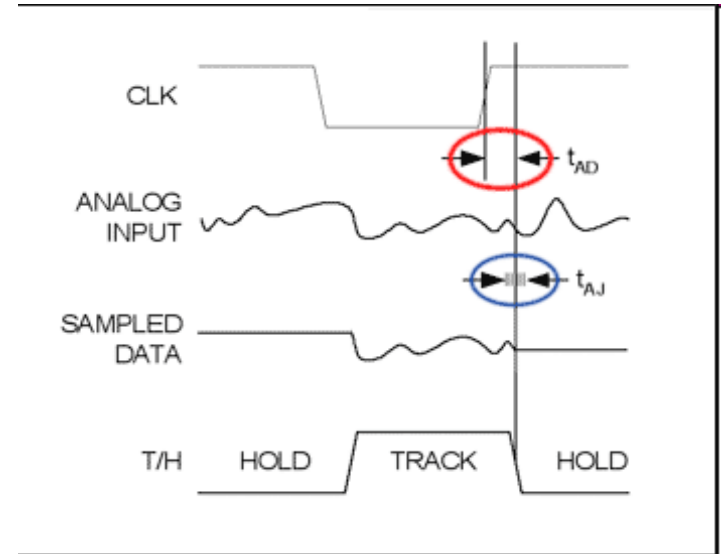
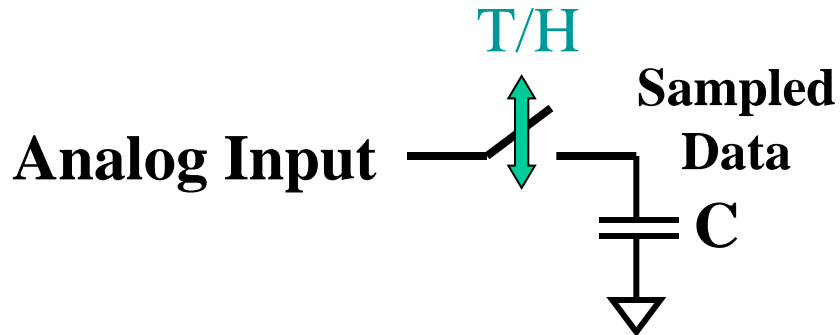


Overview

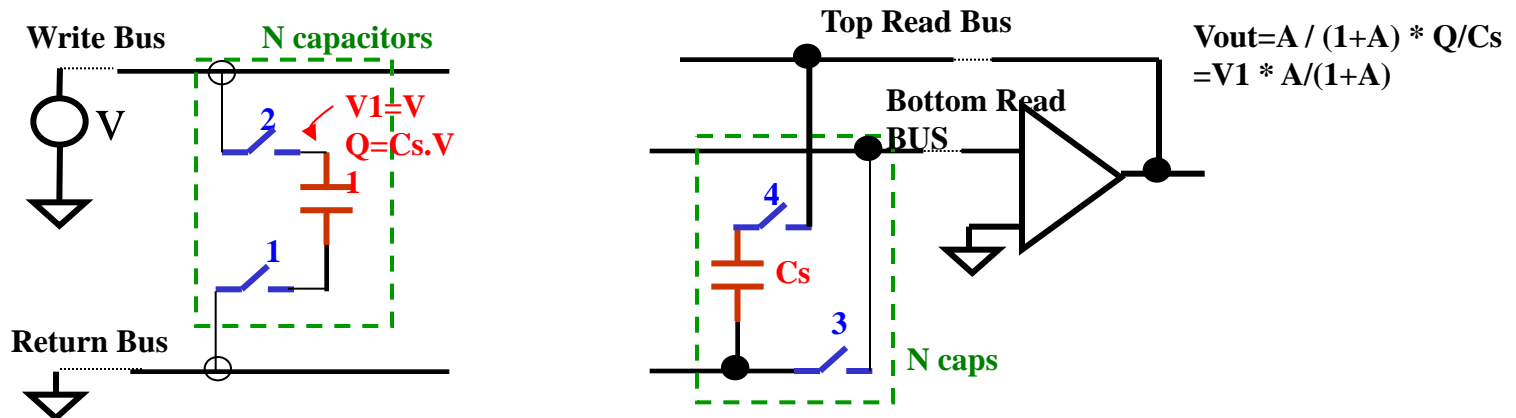
- Further advances at the Discovery Frontier
 - Depends upon developing new instruments and techniques
 - Exploit commodity resources
- The “easy” experiments are being completed
 - Can’t necessarily scale up (\$\$\$, $T > N * t_{\text{gradstudent}}$)
 - Innovation fuels new opportunities
- What I hope to convey:
 1. Very general architectures – limits
 2. Active area of development
 3. Merely a snapshot

Underlying Technology

- Track and Hold (T/H)

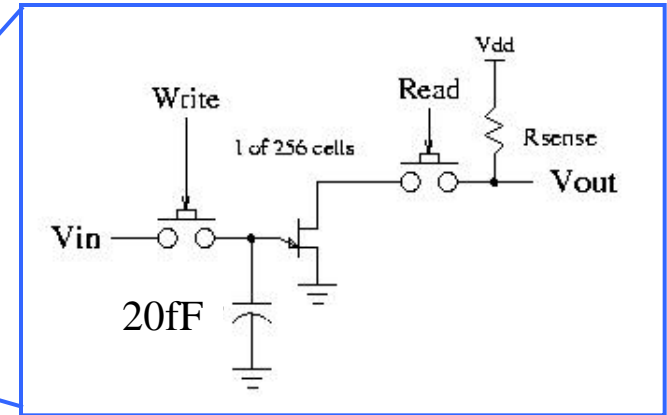
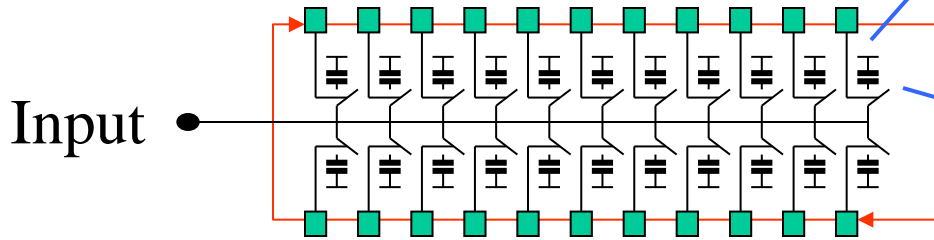


- Pipelined storage = array of T/H elements, with output buffering



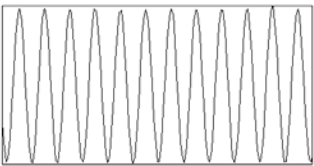
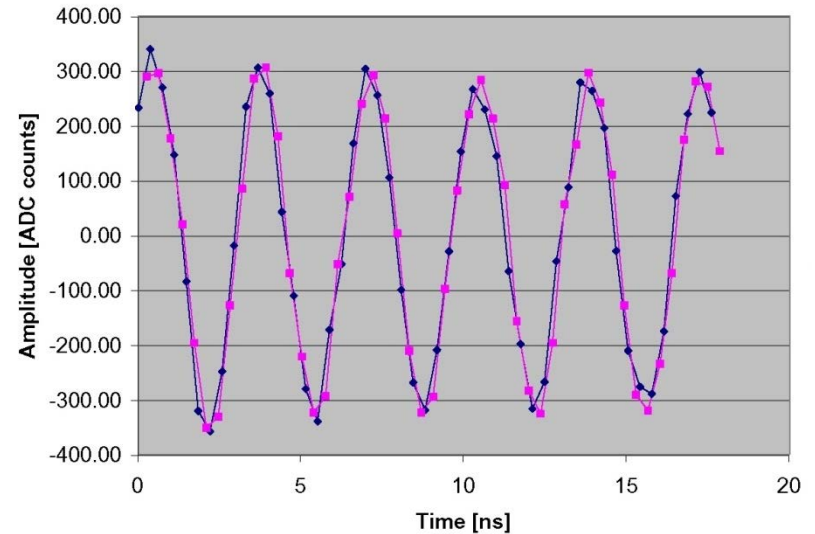
Switched Capacitor Array Sampling

- Write pointer is ~few switches closed @ once

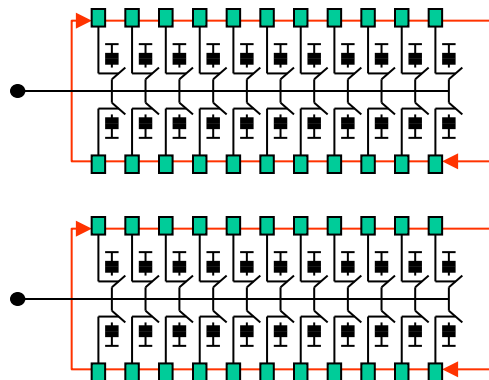


Tiny charge: $1\text{mV} \sim 100e^-$

300MHz RF Sine [50mV amplitude]



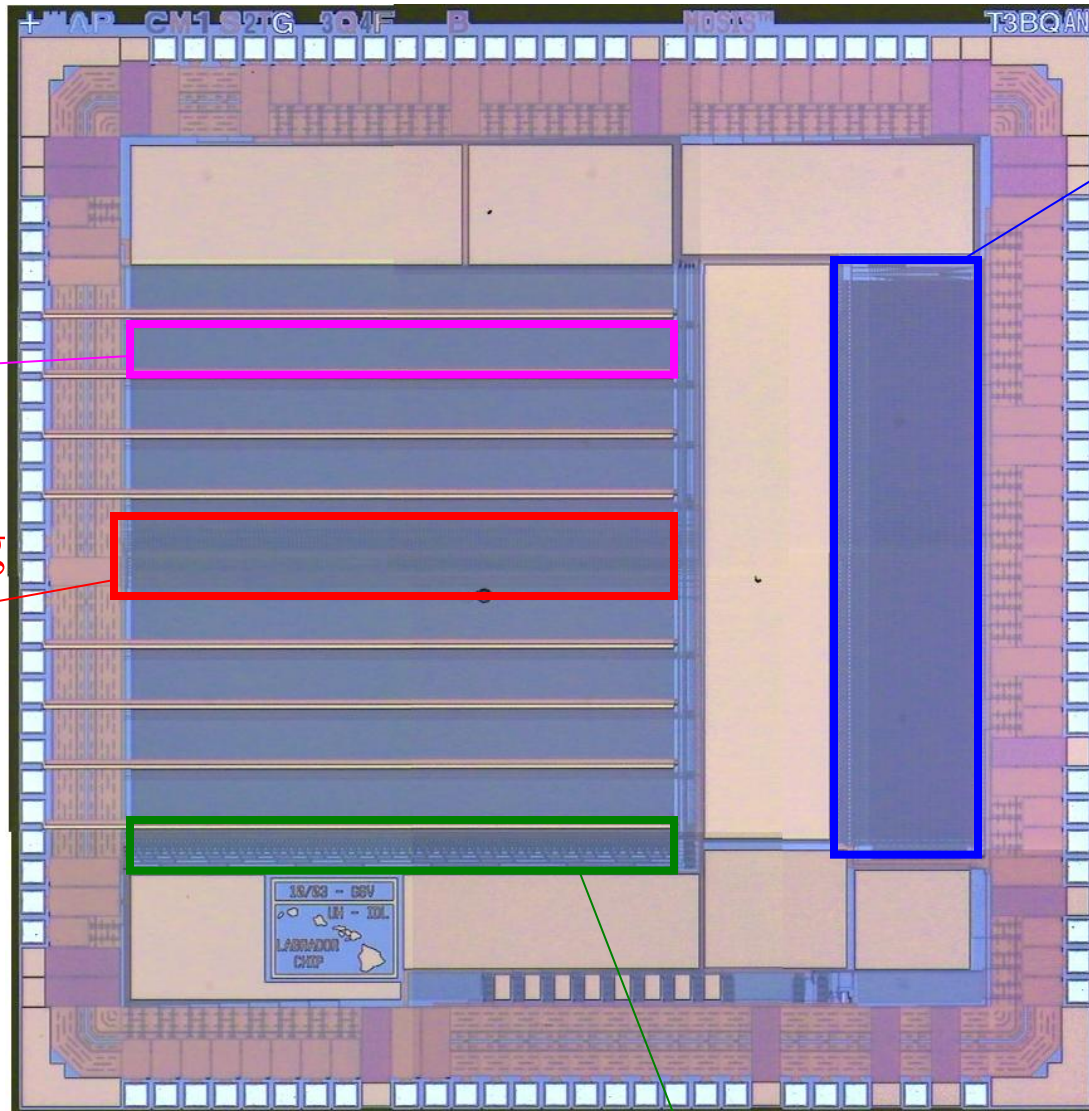
Few 100ps delay



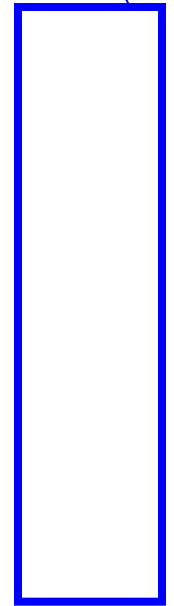
Channel 1

Channel 2

Basic Functional components



On or off-chip ADC



Single storage Channel

Sample timing Control

Few mm x
Few mm
in size

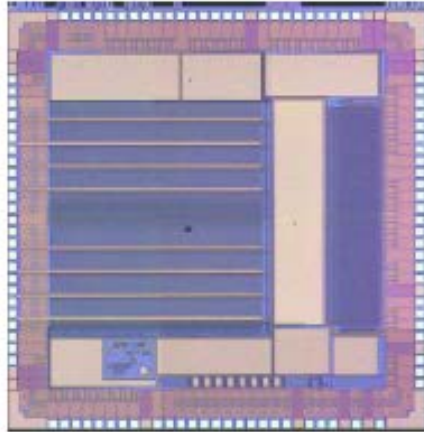
Readout Control

Just a subset of Waveform samplers

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2/3	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
RITC	no.	3	Continuous	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

Gen 2 Enabling Technology (ATWD Gen 1)

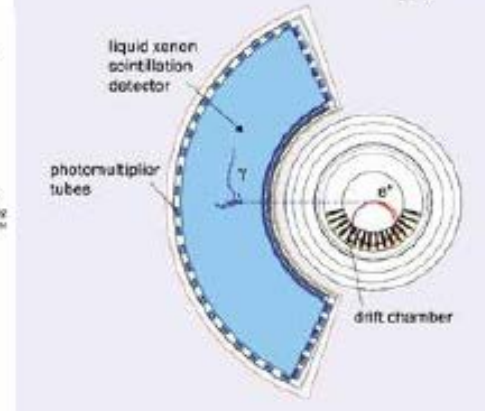
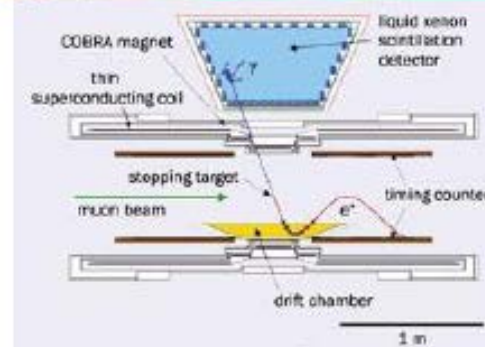
- Already in use in many experiments...



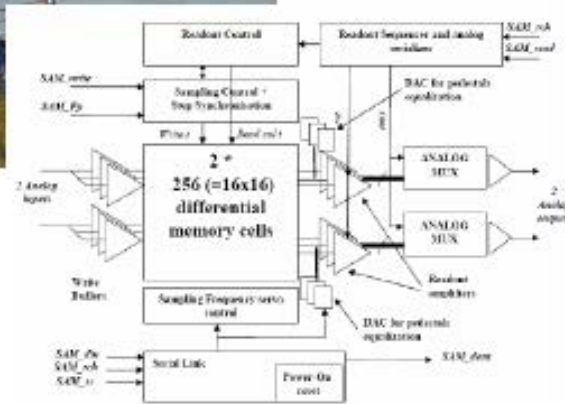
LABRADOR3,
ANITA Experiment



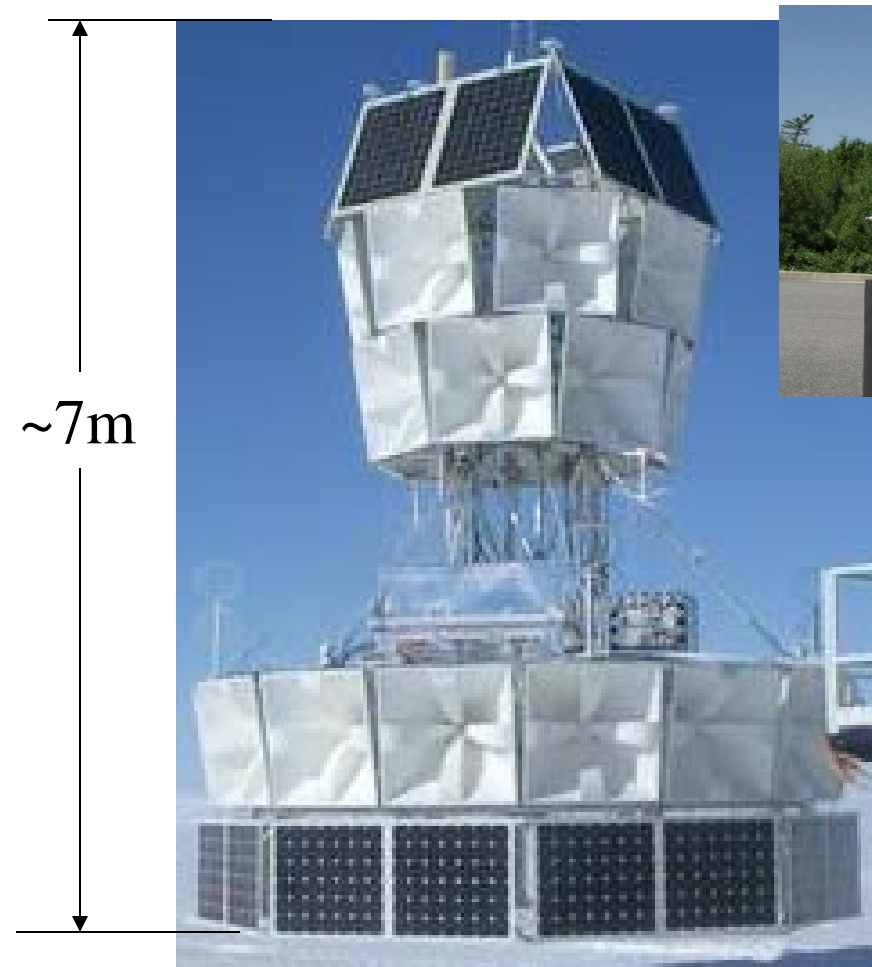
DRS4,
MEG Experiment



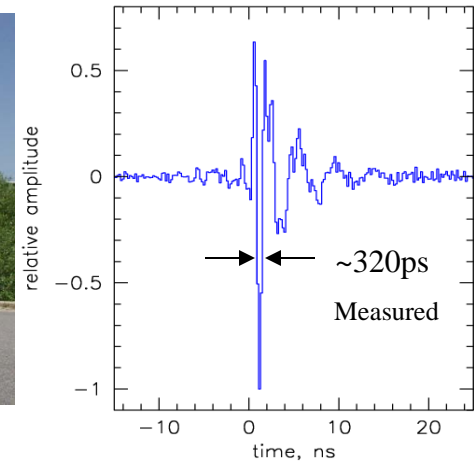
SAM,
H.E.S.S.-II



To be explicit, a demanding Application



Antarctic Impulsive Transient Antenna
(ANITA-I)



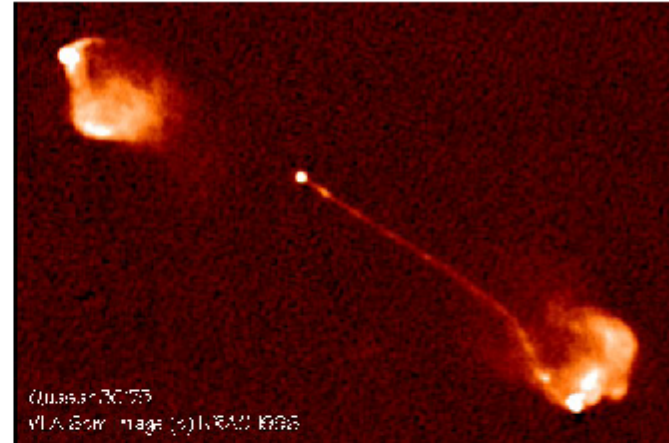
- RF Transient (impulsive) Events (200-1200 MHz)
- 324 chan. @ 2.6GSa/s
- **Completely solar powered** (tight demands on power, few hundred W total)
- Need full waveforms

Pulse Phase interferometry

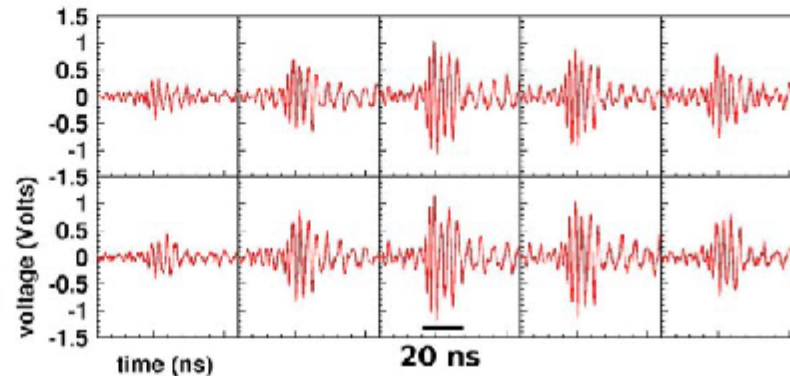
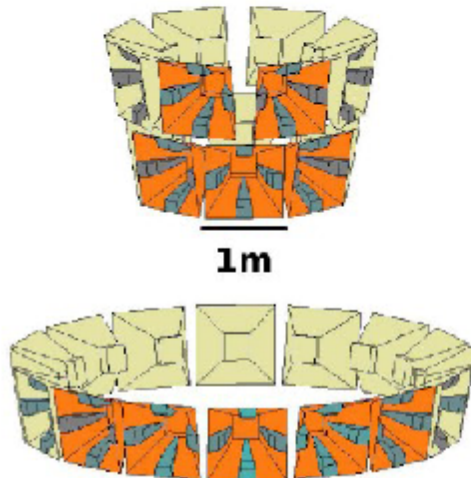
A. Romero-Wolf (Hawaii)

Ultrawide-band Interferometry

- Interferometric technique applied by radio astronomers.
- They use single narrow band frequency.
- More interested in source imaging rather than point source direction reconstruction.

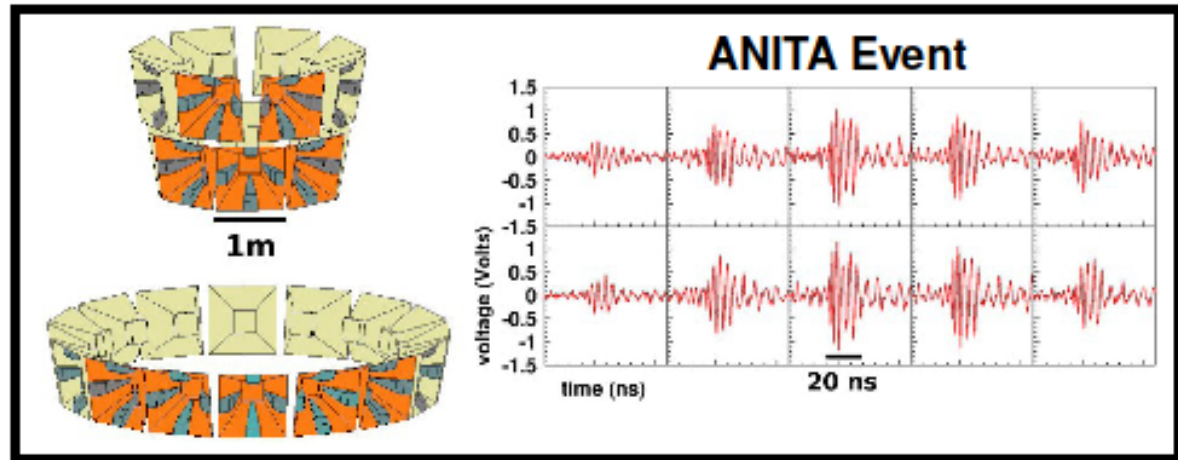


Produce Ultrawide-band Interferometric Images with ANITA

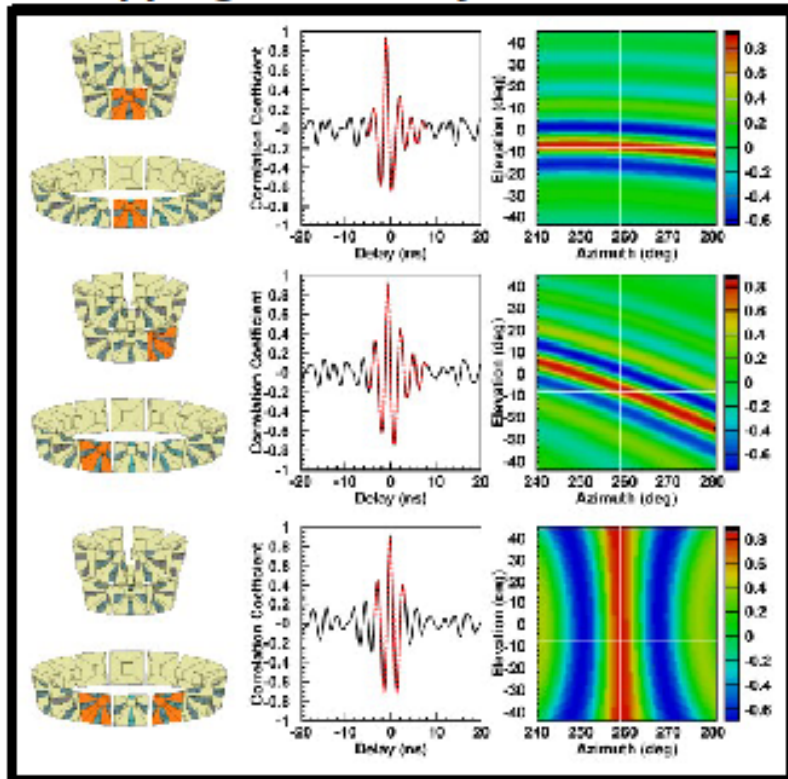


~30ps (16ps) resolution between channels

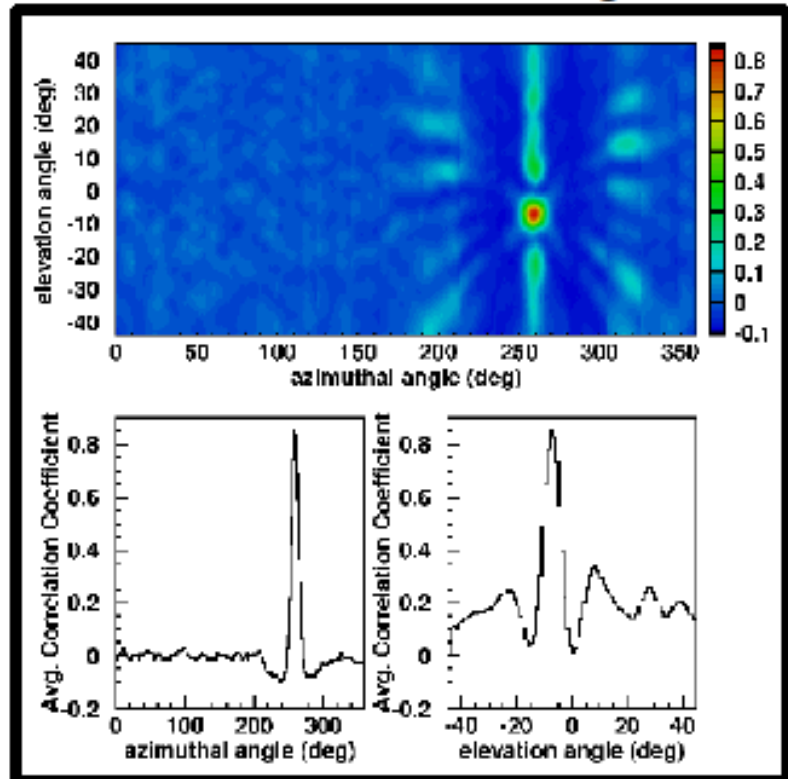
Mapping Waveforms to Interferometric Images



Mapping Time Delay Correlations



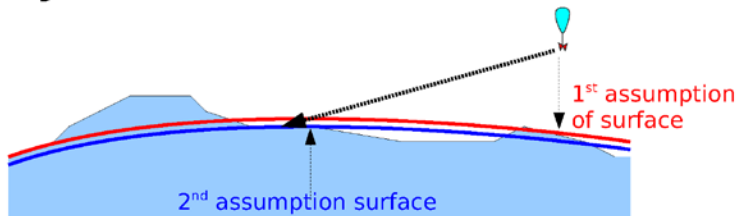
Interferometric Image



After full calibration – 100's km

<30ps timing

RF Projection onto the surface

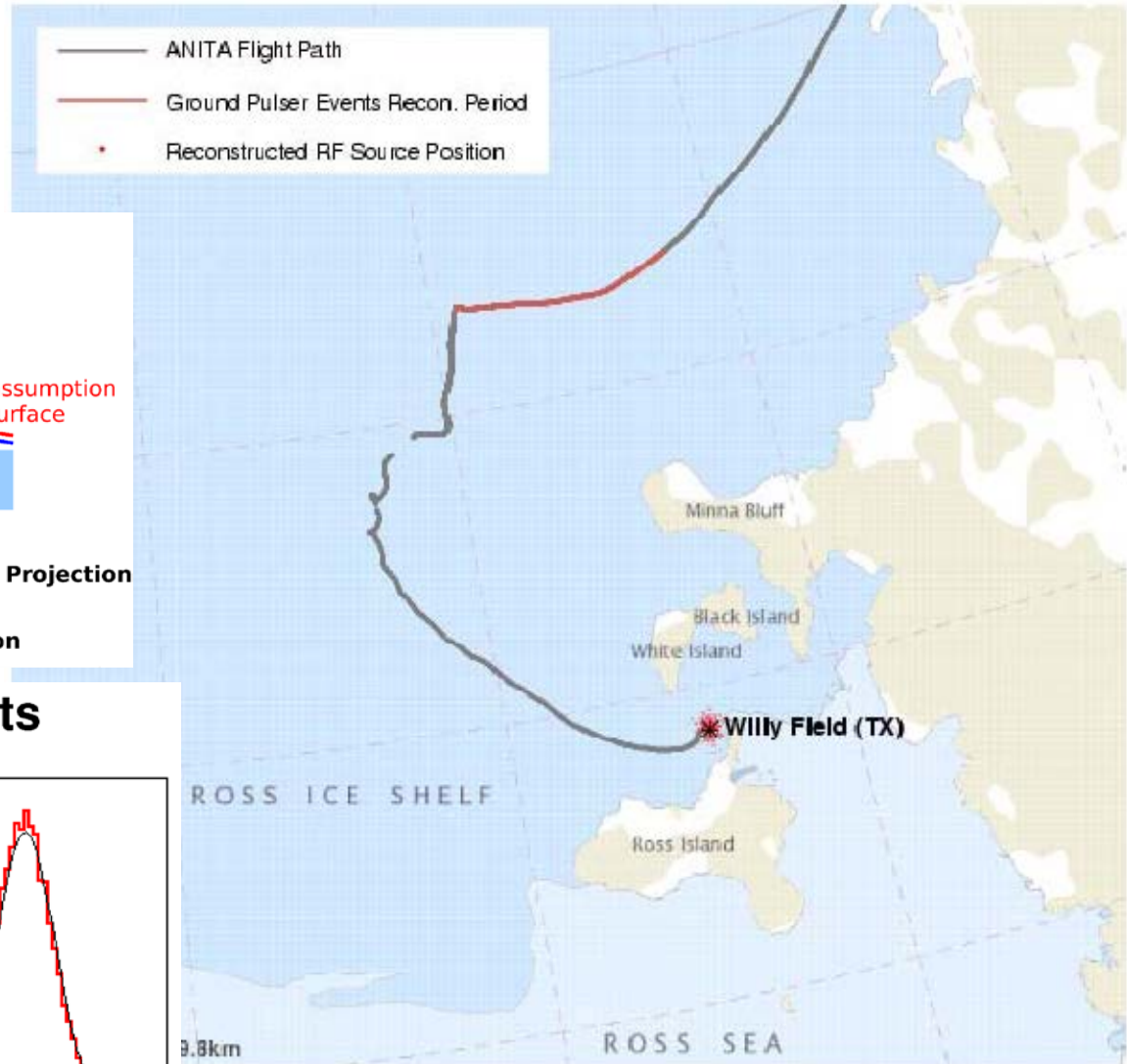
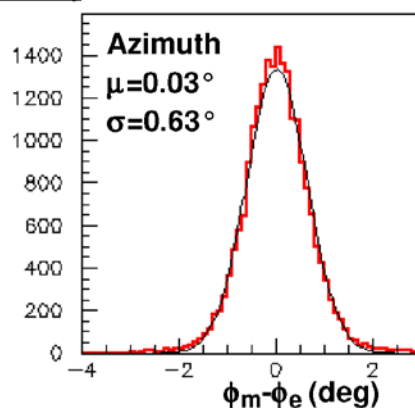
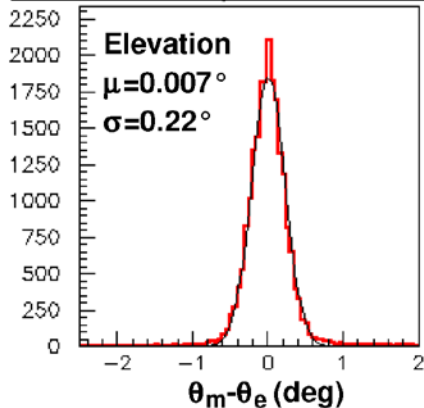


Fast Algorithm: Line Sphere intersection

- 1st $R_{\text{earth}} = \text{Geoid} + \text{Surface @ Ballon position} \rightarrow \text{Rough Projection}$
- 2nd $R_{\text{earth}} = \text{Geoid} + \text{Surface @ (position from 1st)}$
- 3rd: one more iteration \rightarrow converged after 2nd iteration

V-pol results

Borehole Data (used for calibrations)



The “no free lunch” Theorem

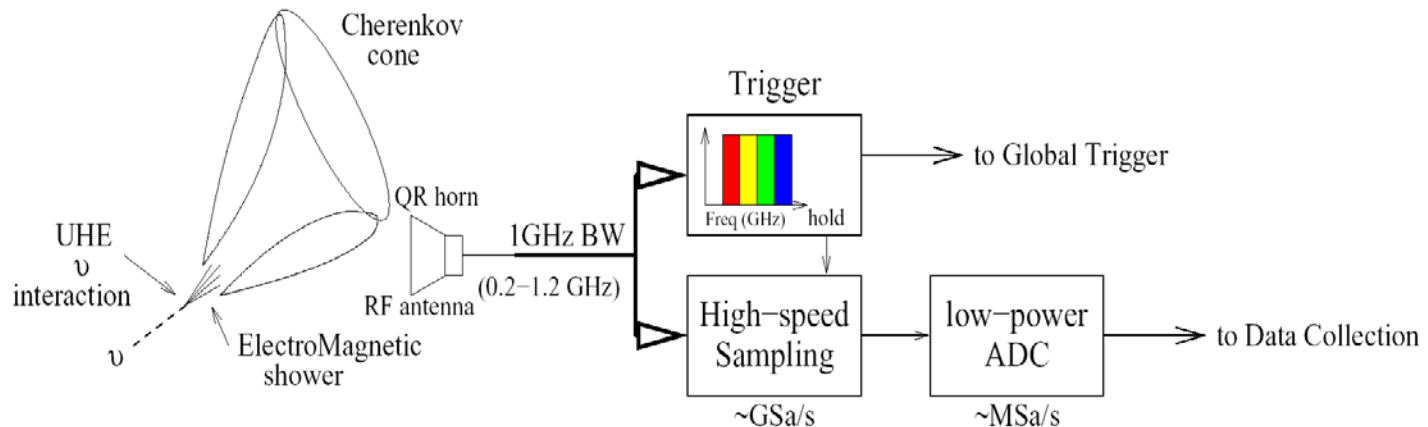
- Excellent results obtained
 1. Has made ANITA and other projects possible & highly successful
 2. Similar architectures being studied for new and upgraded experiments
 3. Minimize costs for large systems
- Not a magic solution
 - Significant/important constraints
 - Technology in its adolescence – will continue to improve
- Limits and future directions

First, the technology, in a bit more detail

Constraint 0: An Intrinsic Limitation

No power (performance savings) for
continuous digitization

Won't displace Flash ADCs

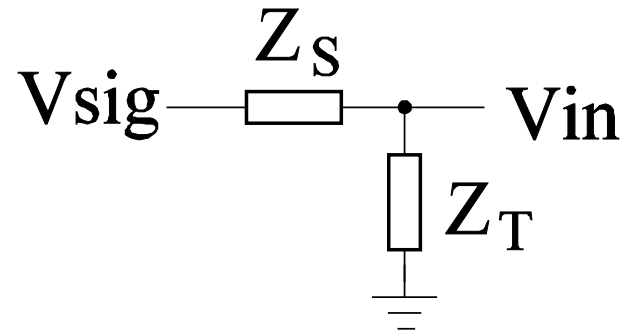
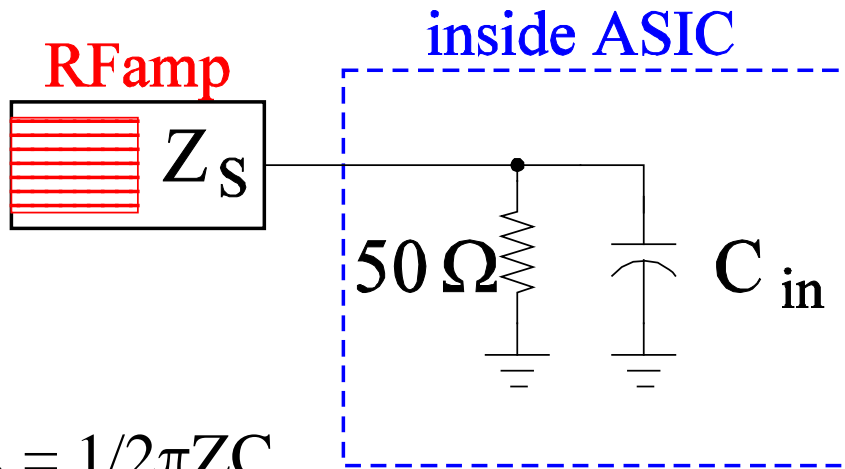


“down conversion”

→ For most “triggered” ‘event’ applications,
not a serious drawback

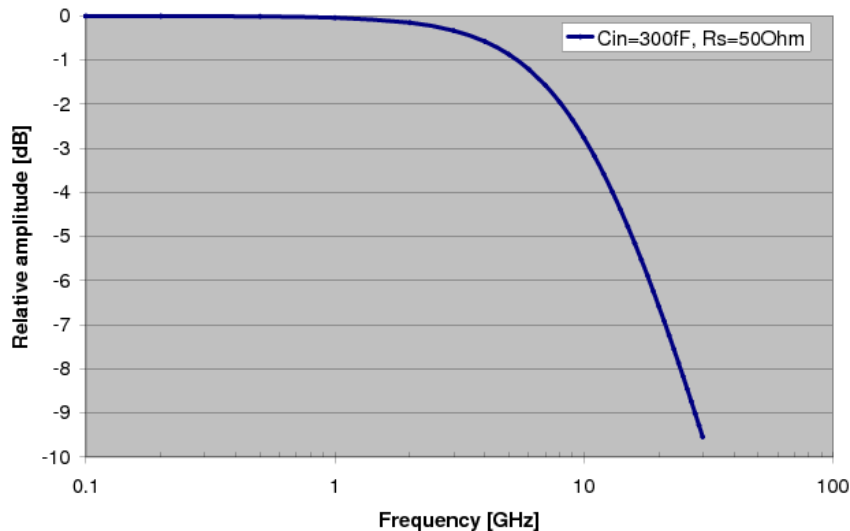
Constraint 1: Analog Bandwidth

Difficult to couple in Large BW (C is deadly)

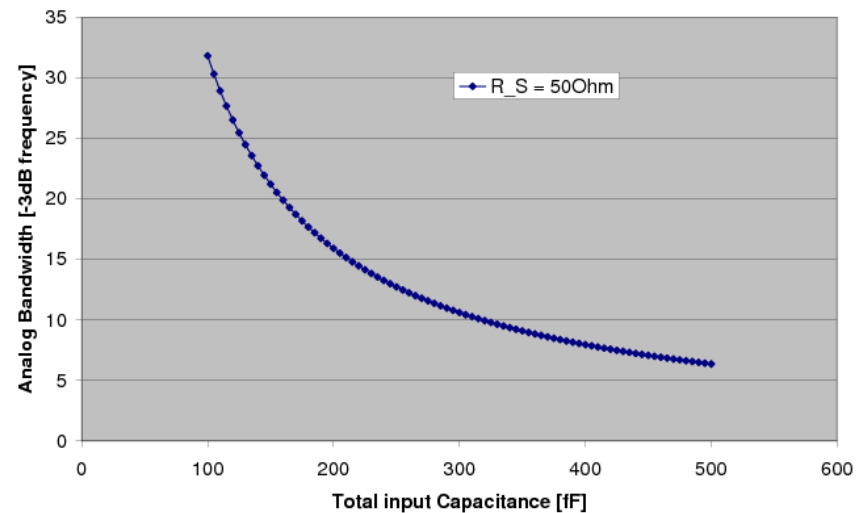


$$f_{3dB} = 1/2\pi ZC$$

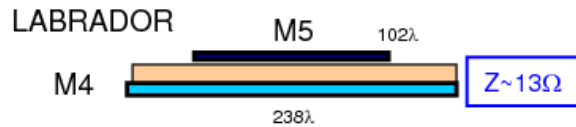
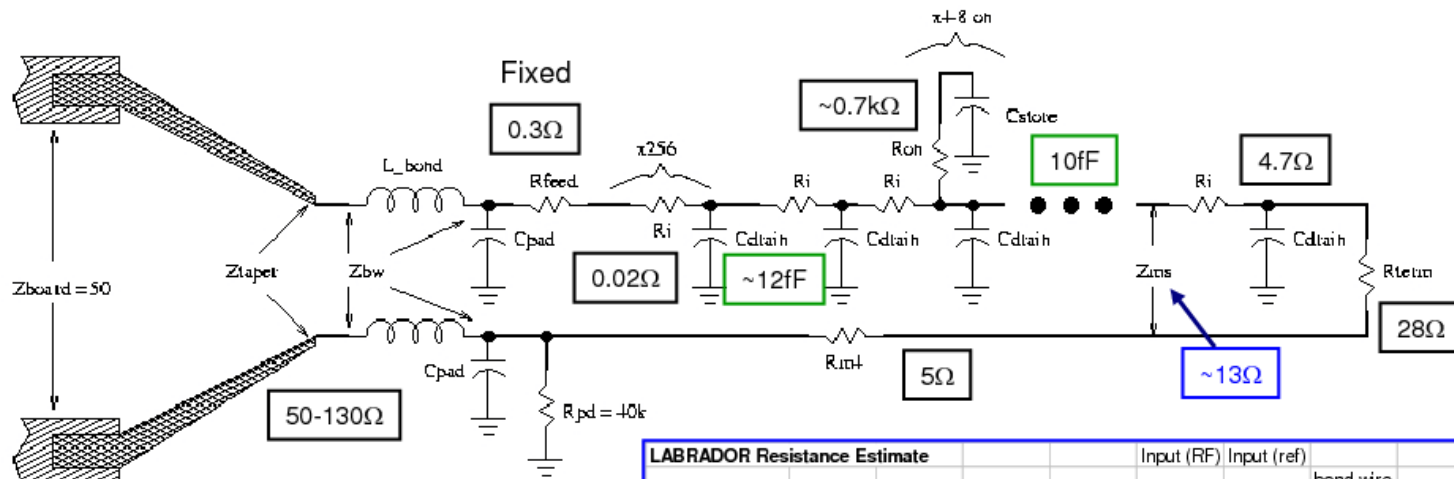
Input coupling versus frequency



Input Coupling versus total input Capacitance



Constraint 2: Storage Depth



LABRADOR Resistance Estimate				Input (RF)	Input (ref)	
Length	17000 λ			0.0	0.1	bond wire
		70			0.2	pad
Metal 4(sheet) =	0.07 Ohm/sq		71.42857		5.0	M5-M4
Metal 5(sheet) =	0.03 Ohm/sq	166.6667		5.0		typ length (sq.)
						typ length (sq.)
Poly contact =	5.1 Ohm	6	6	0.9	0.9	
via 1=	2.7 Ohm	6	3	0.5	0.9	
via 2=	5.35 Ohm	6	3	0.9	1.8	
via 3=	8.26 Ohm	6	3	1.4	2.8	
via 4=	11.34 Ohm	6		1.9		
				10.5	11.5	Total per feed
						28 Rterminator
Measured:	Ohm				50.0	Grand Total

(LAB1 example)

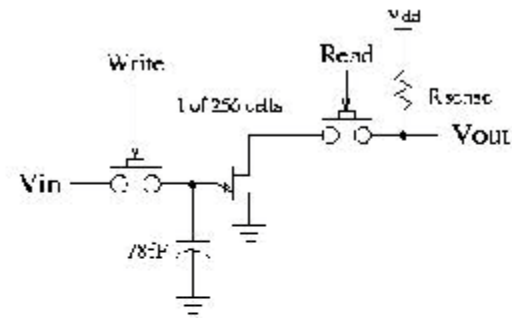
$$f_{3dB} = 1/2\pi ZC$$

Would like smallest possible C_{store}

- For 1.2GHz, $C < \sim 2\text{pF}$ (NB input protection diode $\sim 10\text{pF}$)
- Minimize C , (C_{drain} not negligible x260)

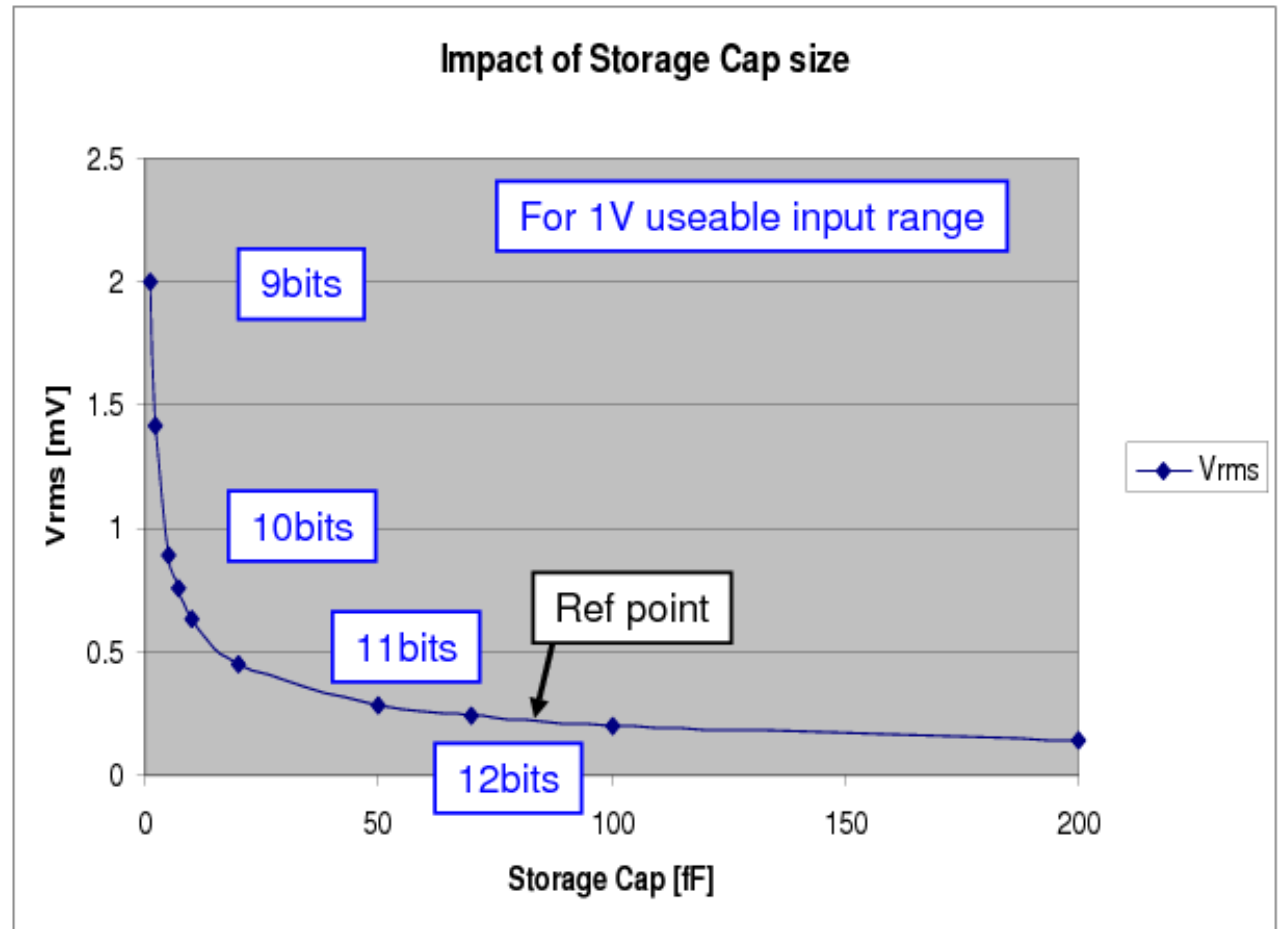
Constraint 3: kTC Noise

Want small storage C, but...



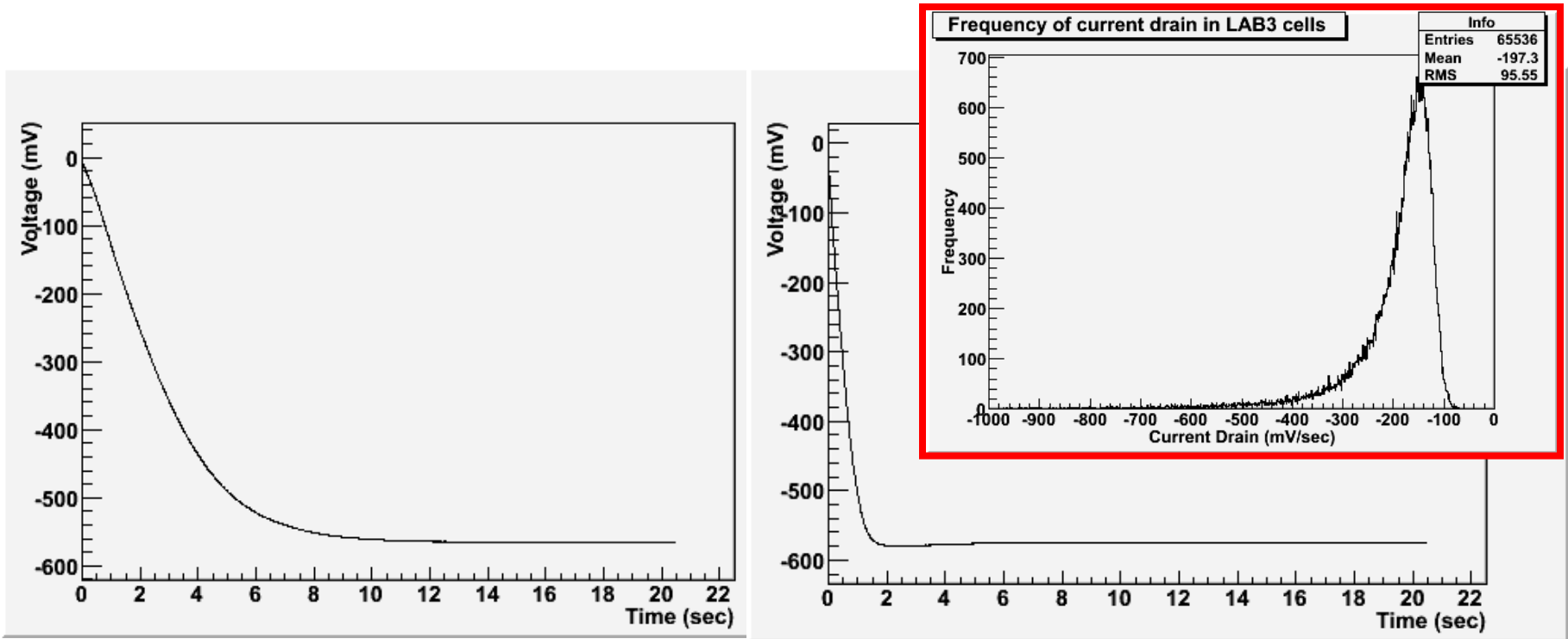
$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

$$C_{store} = 78fF$$



Similar Constraint 3b: Leakage Current

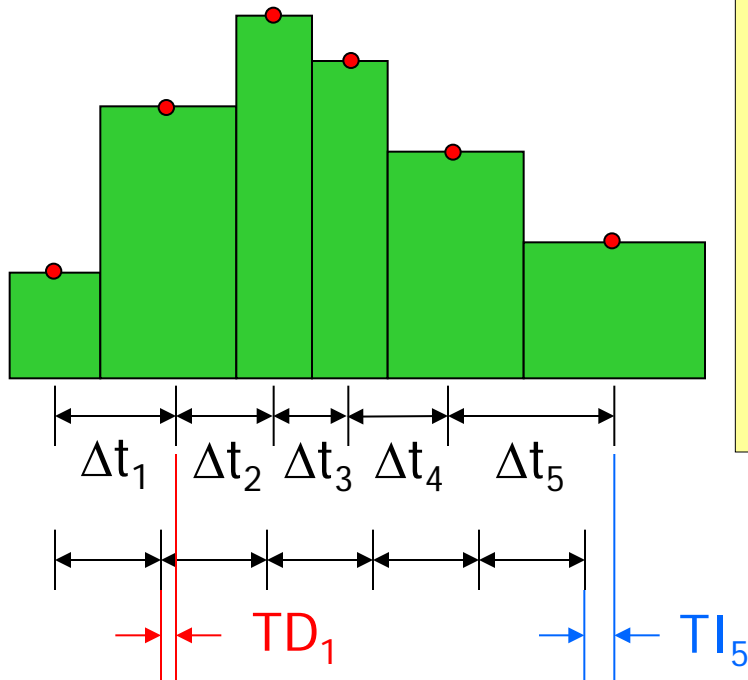
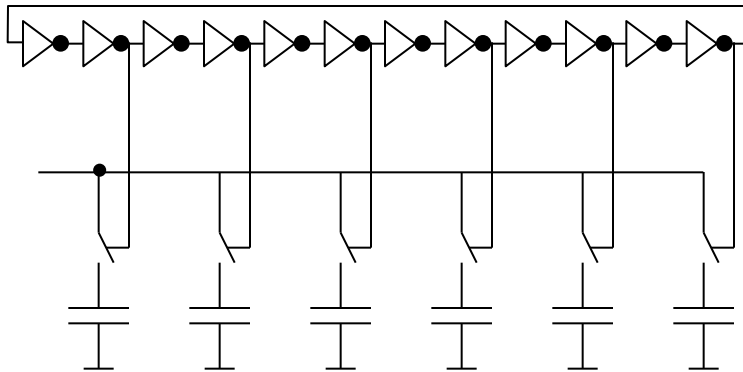
Increase C or reduce conversion time $\ll 1\text{mV}$



Sample channel-channel variation $\sim \text{fA}$
leakage typically (0.25um process)

Becomes much worse in faster (digital) processes

Constraint 4: Sample Aperture Variance

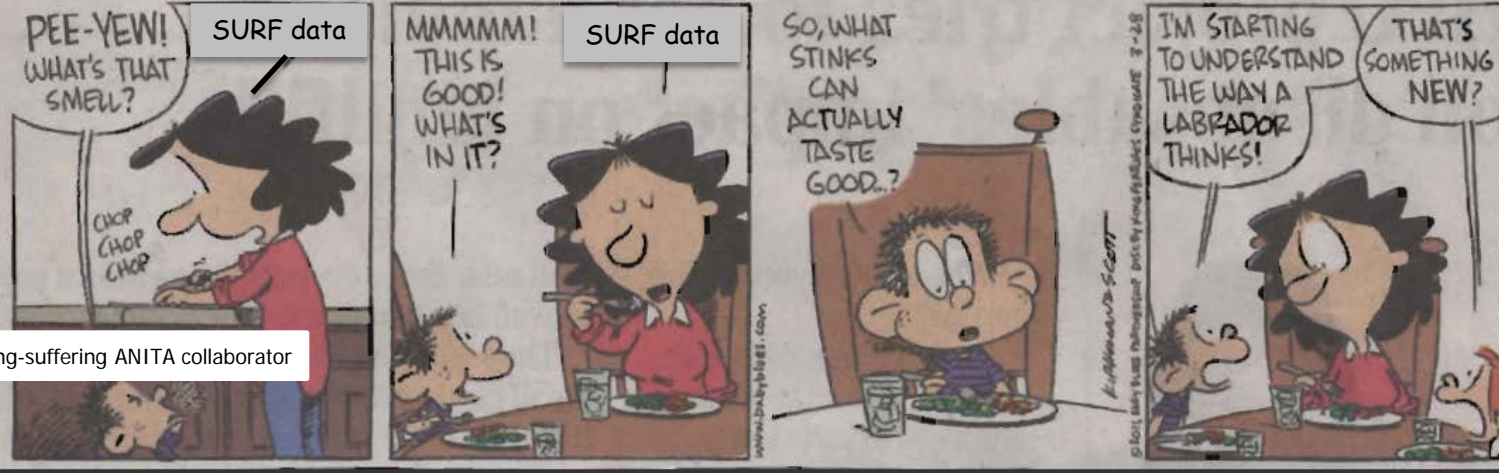


- Inverter chain has transistor variations
→ Δt_i between samples differ
→ "Fixed pattern aperture jitter"
- "Differential temporal nonlinearity"
 $TD_i = \Delta t_i - \Delta t_{\text{nominal}}$
- "Integral temporal nonlinearity"
 $TI_i = \sum \Delta t_i - i \cdot \Delta t_{\text{nominal}}$
- "Random aperture jitter" = variation of Δt_i between measurements

Non-uniform sampling timebase



Baby Blues >> Kirkman & Scott



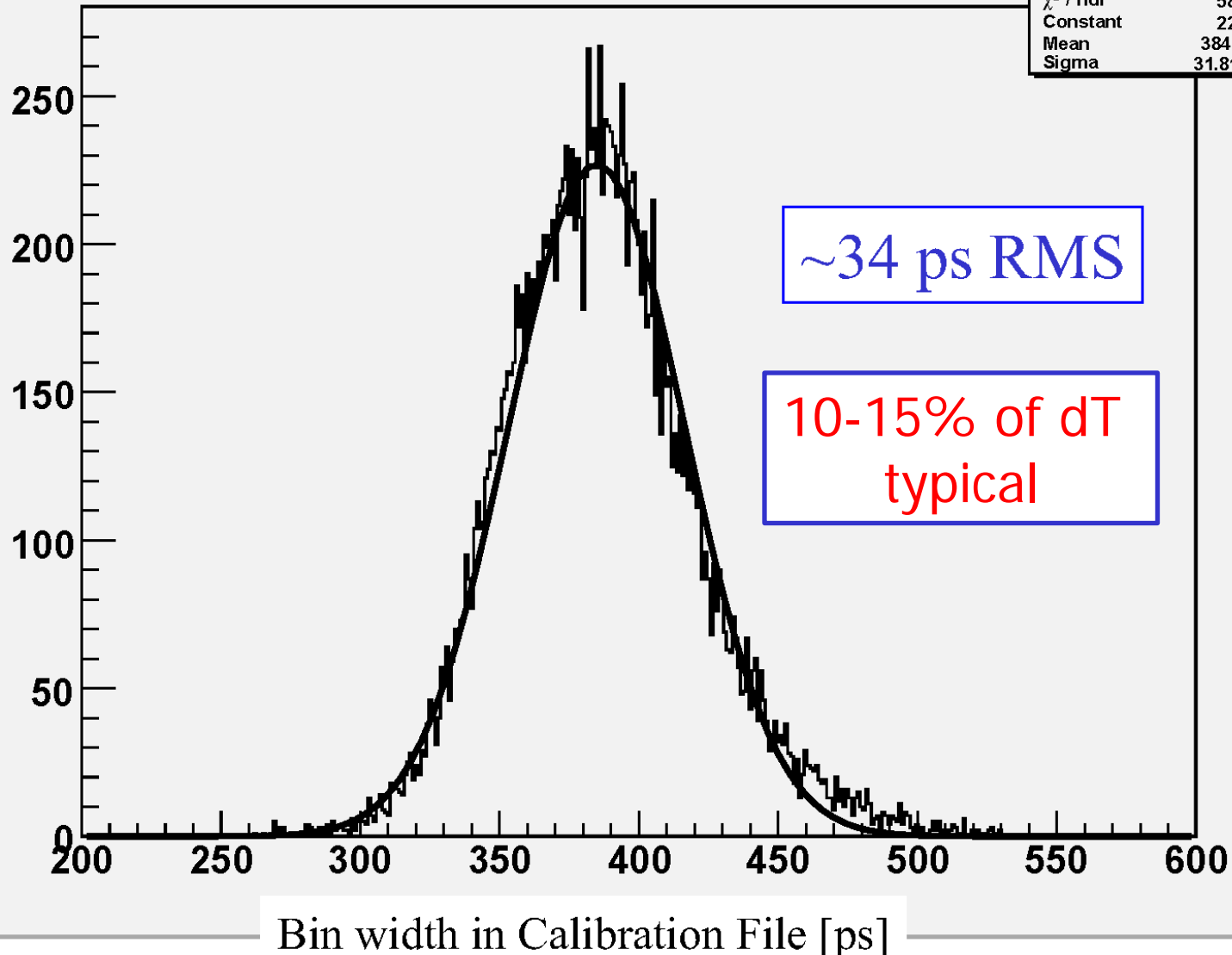
Long-suffering ANITA collaborator



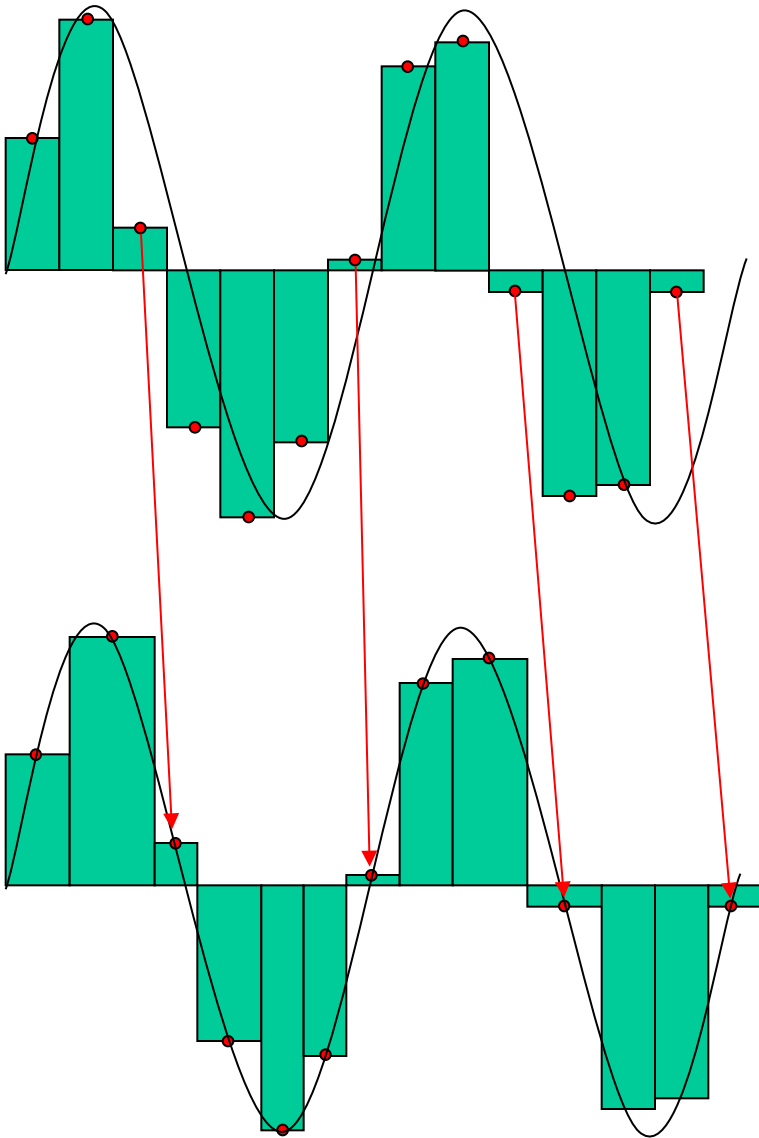
dT Spread

2.6 GSa/s [LABRADOR3]

Bin Interval	
Entries	18720
Mean	386
RMS	34.3
χ^2 / ndf	582 / 253
Constant	227 ± 2.2
Mean	384.8 ± 0.2
Sigma	31.81 ± 0.19



Average aperture calibration



- Fixed aperture offsets are constant over time, can be measured and corrected
- Several methods are commonly used (sine fit [left], zero-crossing)
- Most use sine wave with random phase and correct for TD_i on a statistical basis

Great progress in improved algorithms:

<http://arxiv.org/abs/1405.4975>

However still computationally expensive (e.g. resampling for FFTs)

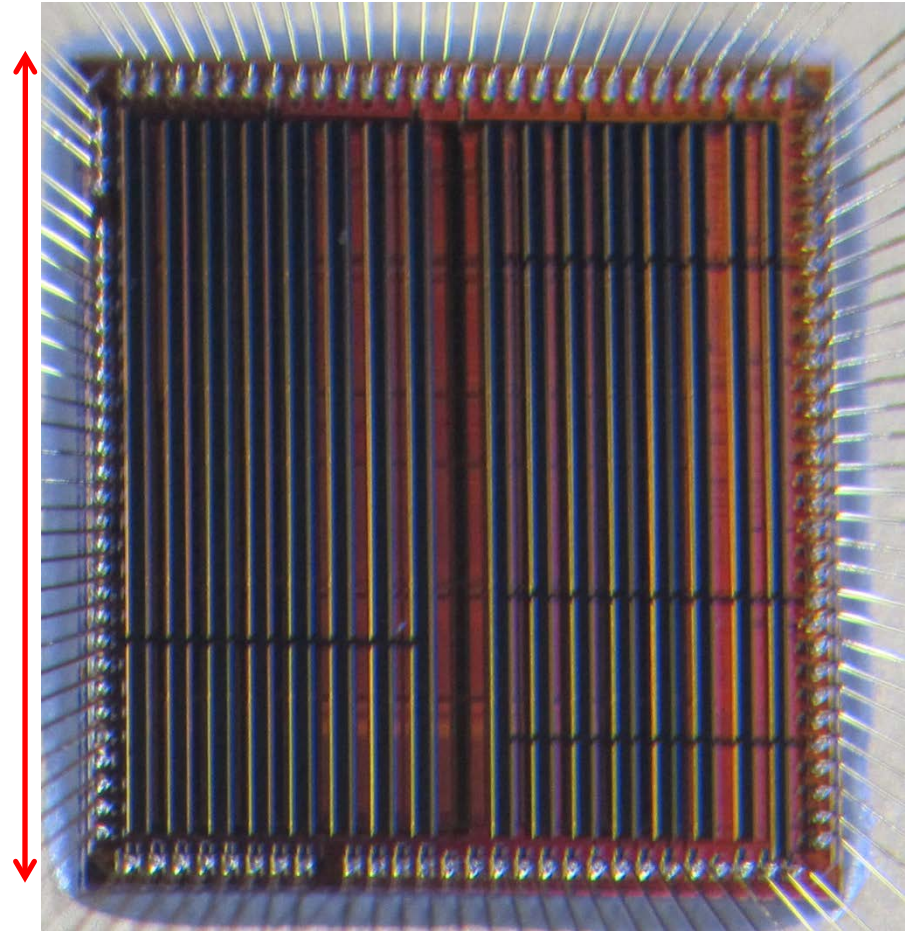
“3rd Generation” (arbitrary)

- Raw performance of 2nd Generation devices
 - Have proven themselves
 - Somewhat general purpose – therefore each adopter wants to change something
- Next generation addressing these constraints
 1. Analog bandwidth
 2. Storage depth
 3. System requirements (clock, flow control, multi-hit, etc.)
 4. Calibration overhead
- Merely a snapshot:
 1. This talk is a moving target
 2. Highly dynamic field
 3. A lot of cross-pollination

1) Analog bandwidth (sampling, readout speed)

PSEC-4 ASIC

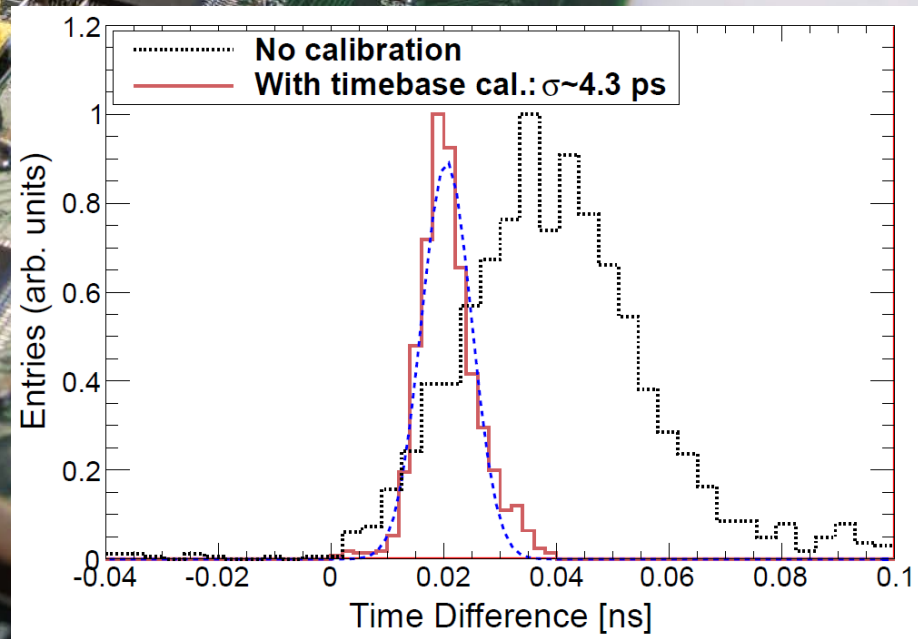
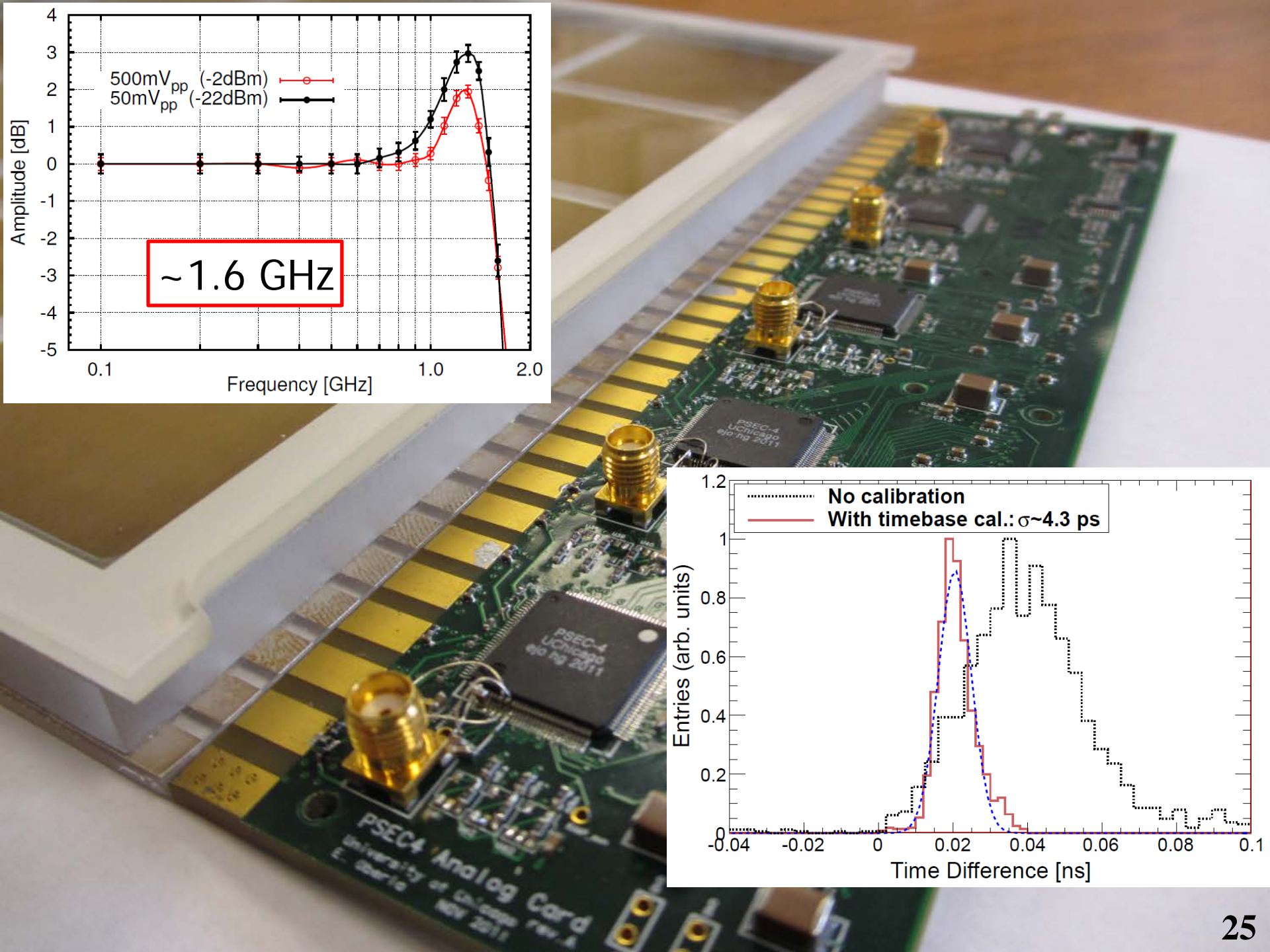
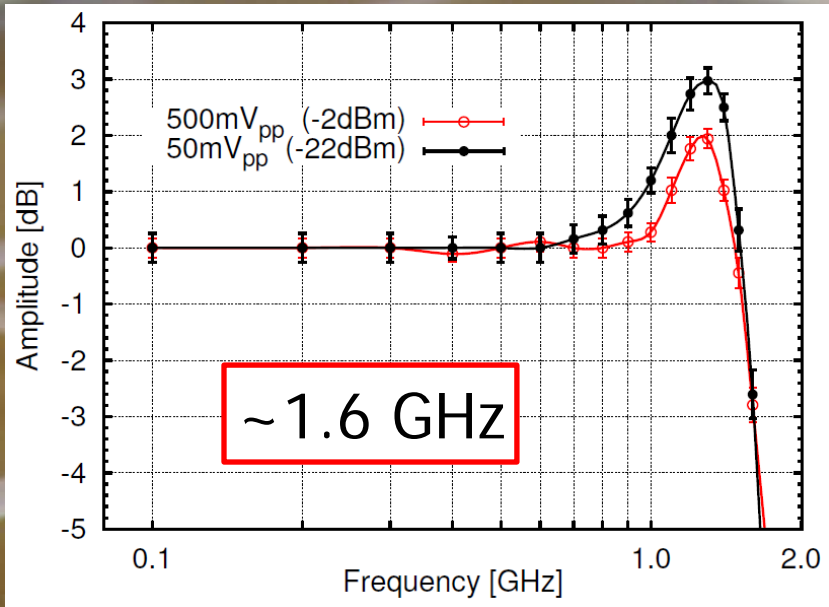
Sampling Rate	2.5 GSa/s-17GS/s	4.3mm
# Channels	6 (or 2)	
Sampling Depth	256 (or 768) points	
Sampling Window	Depth*(Sampling Rate) ⁻¹	
Input Noise	<1 mV RMS	
Analog Bandwidth	1.6 GHz	
ADC conversion	Up to 12 bit @ 2GHz	
Latency	2 μs (min) – 16 μs (max)	
Internal Trigger	yes	



**130nm process – sampling speed,
Conversion rate**

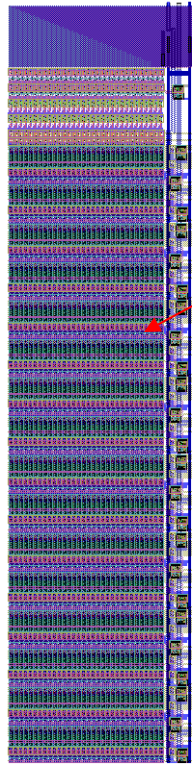
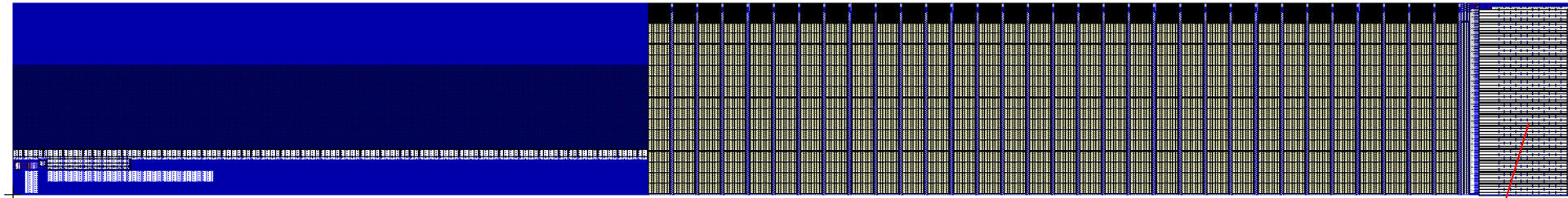
[E. Oberla, U. Chicago]

4.0mm



2) Storage Depth

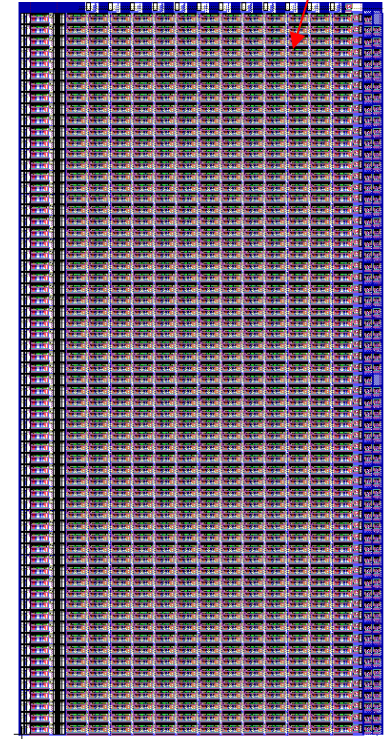
- **Sampling: 128 (2x 64) separate transfer lanes** Recording in one set 64, transferring other (“ping-pong”)



- **Concurrent Writing/Reading**

- **Only 128 timing constants**

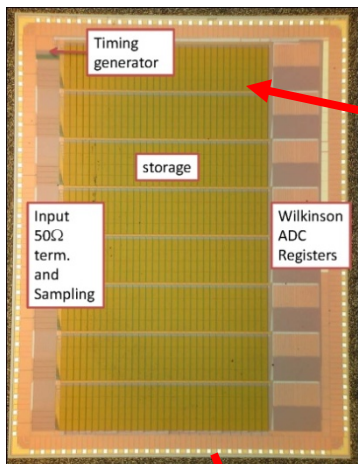
- **Storage: 64 x 512 (8 ch. IRS)**
(32x512 16 ch. [TARGET – CTA])
- **Wilkinson (64x1): was (32x2)**
 - **64 conv/channel**



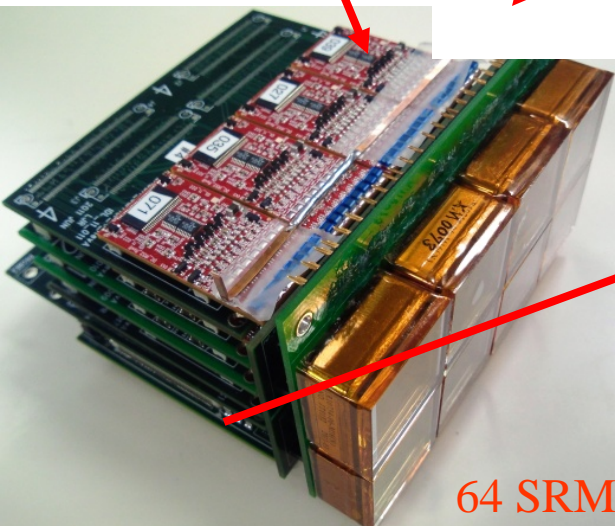
3a) Ex. Belle II TOP Readout Architecture

16 COPPER

Waveform sampling ASIC

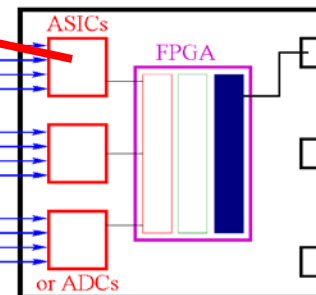


8k channels
1k 8-ch. ASICs



64 SRM

Subdetector Readout Module



- FPGA firmware consists of 3 parts:
- 1) ASIC/ADC driver (common)
 - 2) Trigger feature extract (subdet. specific)
 - 3) Unified DAQ transport protocol

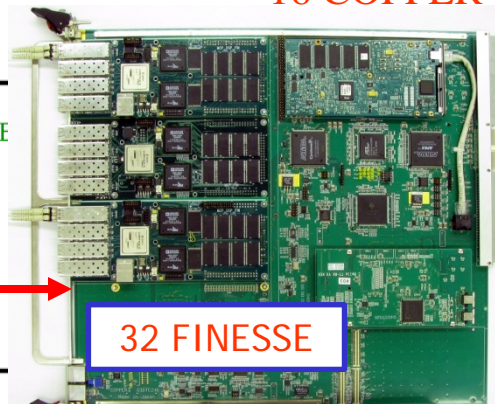
Clock jitter cleaners



SRM Control "SCROD"

COPPER

FINESSE



32 FINESSE

Global Decision Logic

9 TRGmod



Clock/Event Timing Distribution

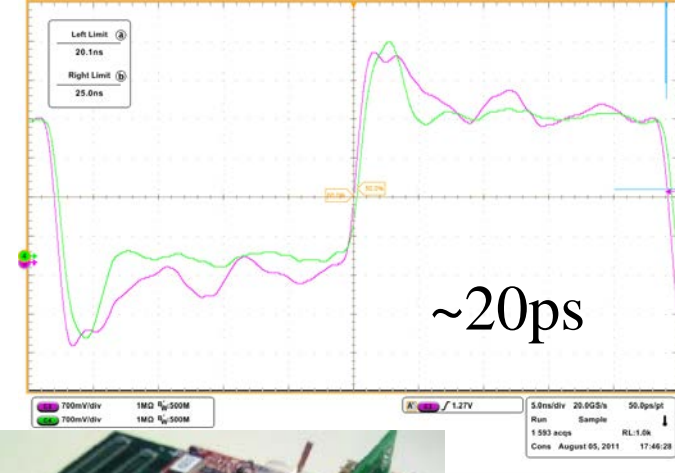
FTSW clock, trigger, programming



16 FTSW

System Synchronization

Crucial to obtain required performance



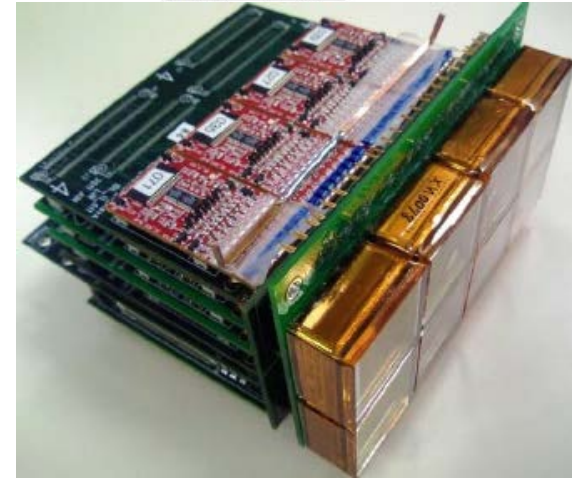
FTSW (Timing & Trigger Distribution board)



127 MHz clock



**Serial data
(trigger & synchronization)**



- **127 MHz clock is divided by 6 on front-end module to ~21 MHz**
 - **This corresponds to sampling rate of ~2.7 GSa/s**
 - **FPGA uses serial data stream to determine clock phase**

127 MHz



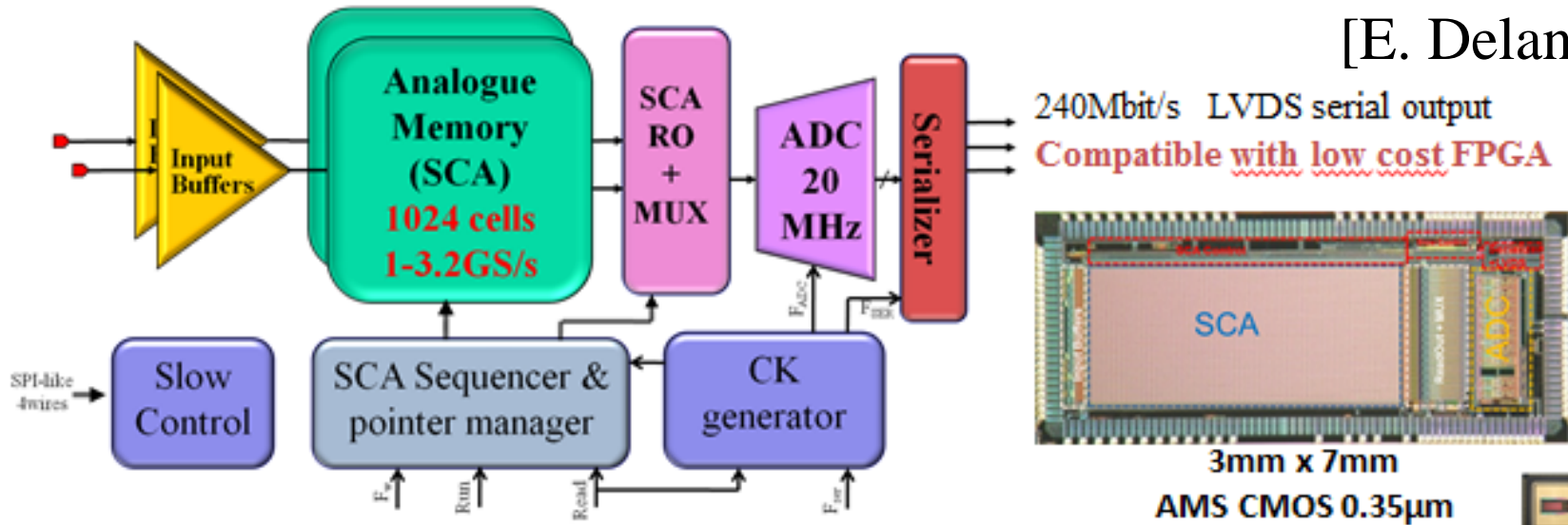
21 MHz



3b/4) Multiple TeV-gamma telescopes

The NECTAR chip for the Cerenkov Telescope Array

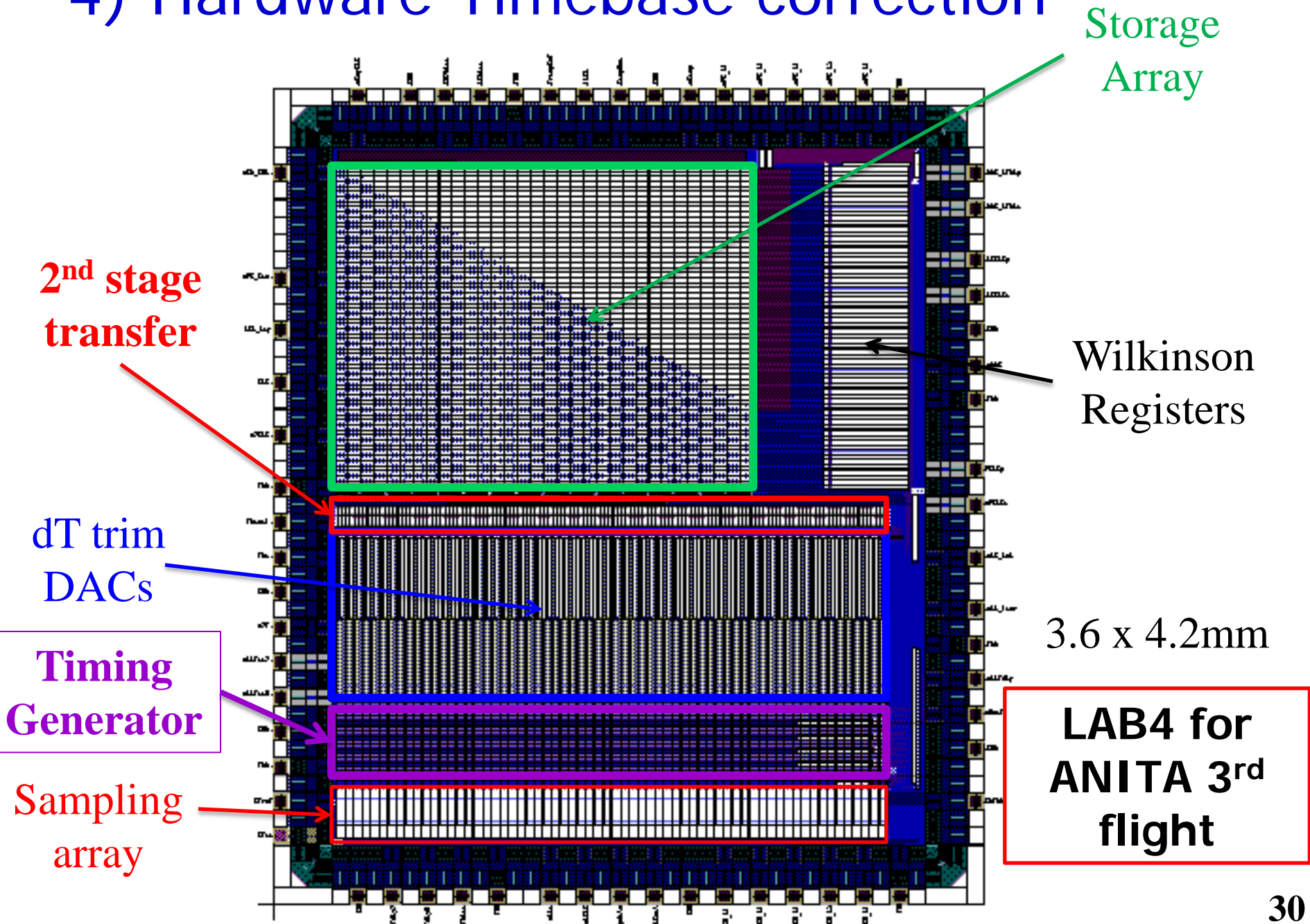
[E. Delange]



- Evolution of the SAM(LONG) chip (HESS-2 telescope)
- 4 SCA channels => 2 fully differential channels
- 1024 cells/SCA channel (64 x 16 matrix)
- 0.5 to 3.2 GSPS => 1μs max latency @ 1GSPS, 0.5μs @ 2GSPS
- On chip 12 bit pipeline 20MSPS ADC
- Output data directly usable for calculation (without need for pedestal or gain spread correction)
- Low input capacitance < 4pF including package thanks to input buffers
- 4000 chips used for the upgrade of the HESS experiment (Namibia)



4) Hardware Timebase correction



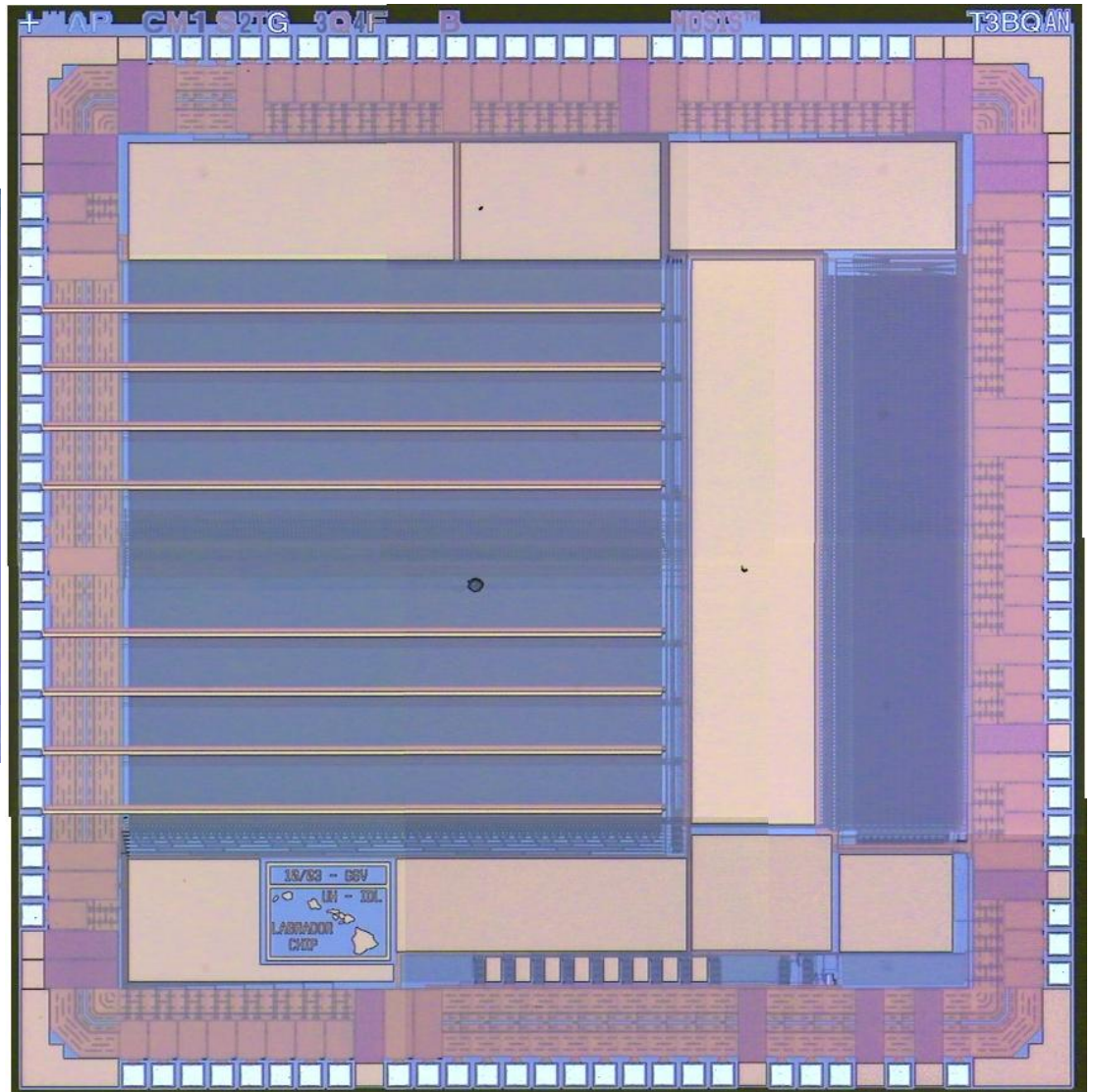
Summary

Deeper SCA Sampling and improvements

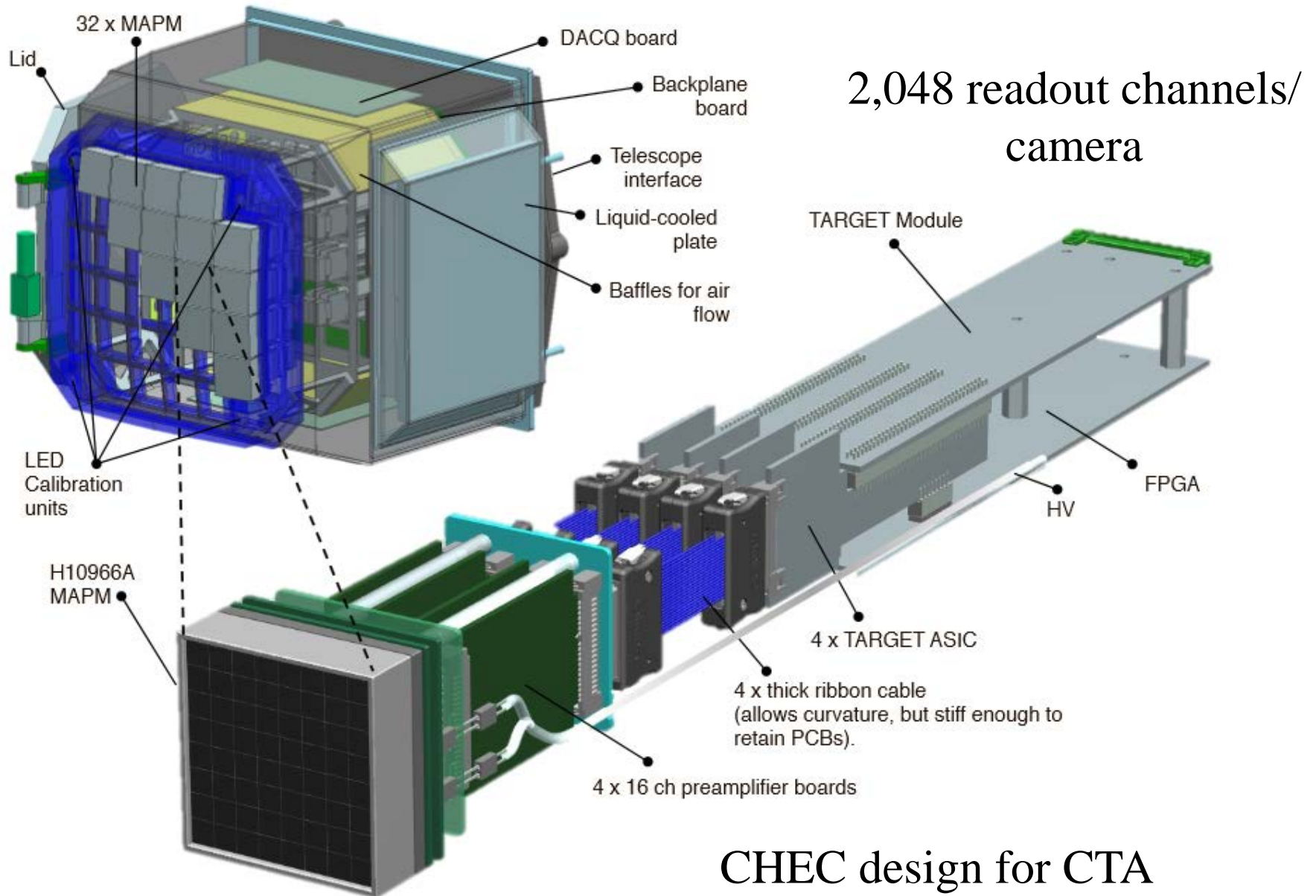
- Enables new ways of instrumenting detectors
- SCA ASIC designs evolving to address system issues
- Much room to integrate processing for further data reduction



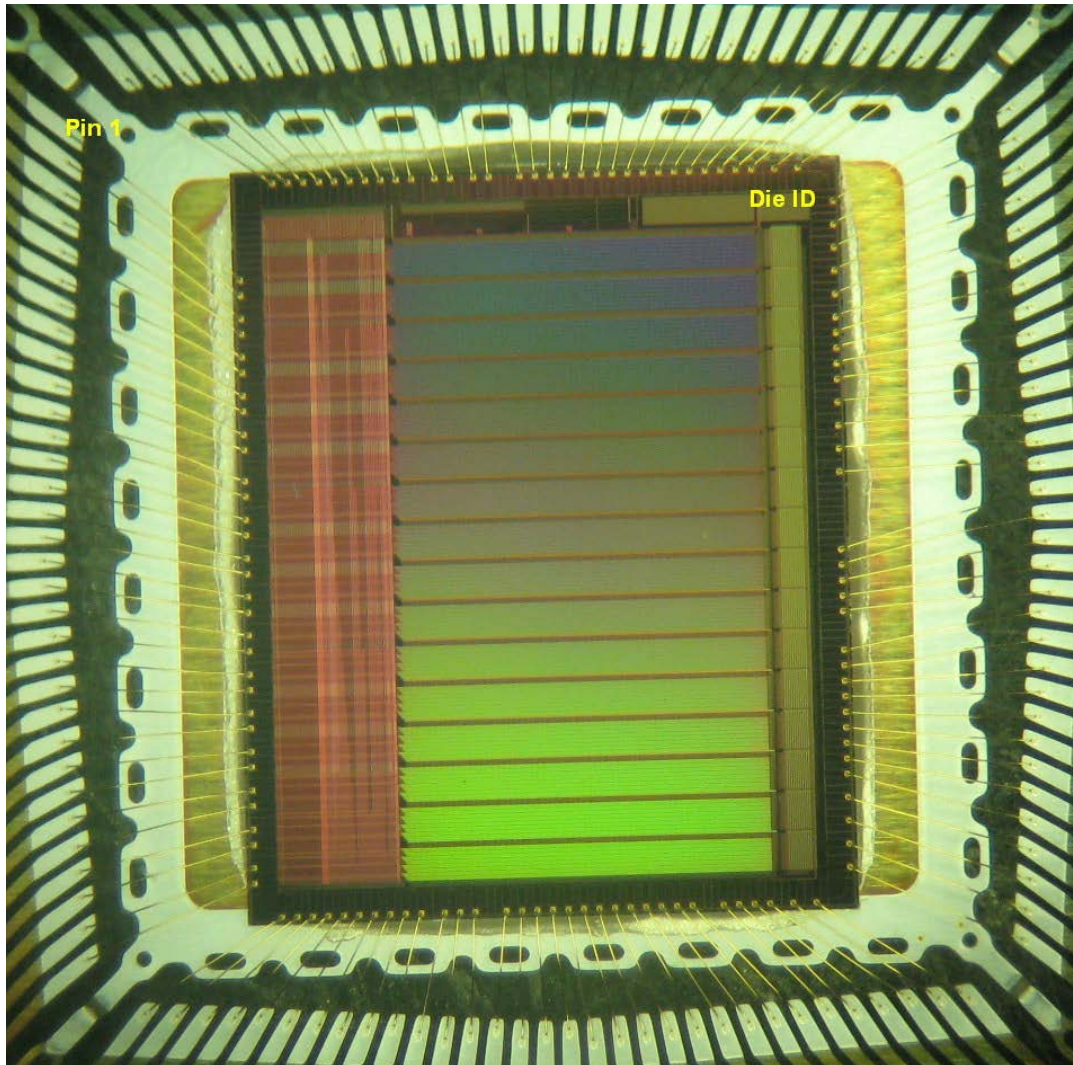
Back-up slides



Some further information on TARGET7



Some further information on TARGET7 the “final” TARGET ASIC for CTA (TARGET5 first camera, TARGETX Belle II)

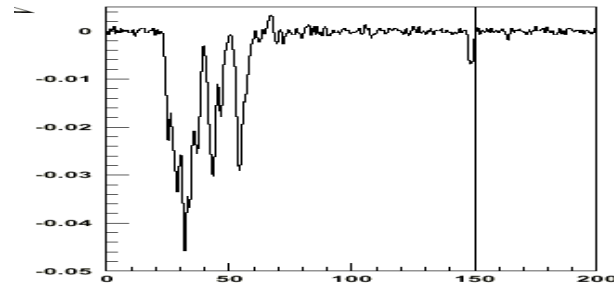
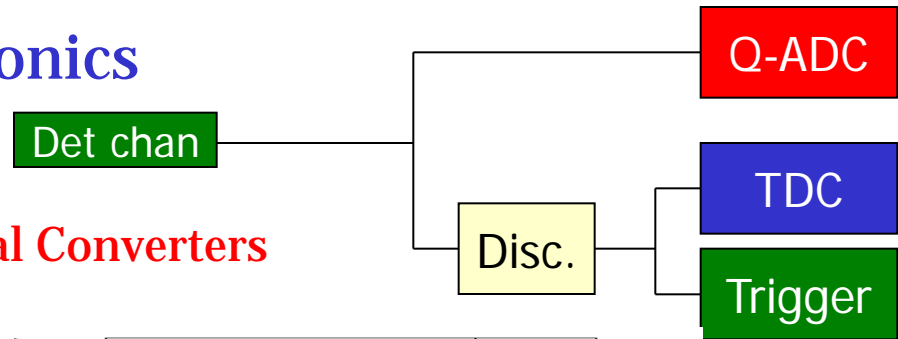


- 0.25um TSMC CMOS*
- 16 channels
- 16,384 samples/channel
- Individual channel discriminators (trigger forming and zero suppression)
- Individual trigger threshold DACs
- All precision timing via programmable timing generators

Detector Instrumentation Evolution

- Traditional “crate based” electronics

- Gated Analog-to-Digital Converters
- Referenced “triggered” Time-to-Digital Converters

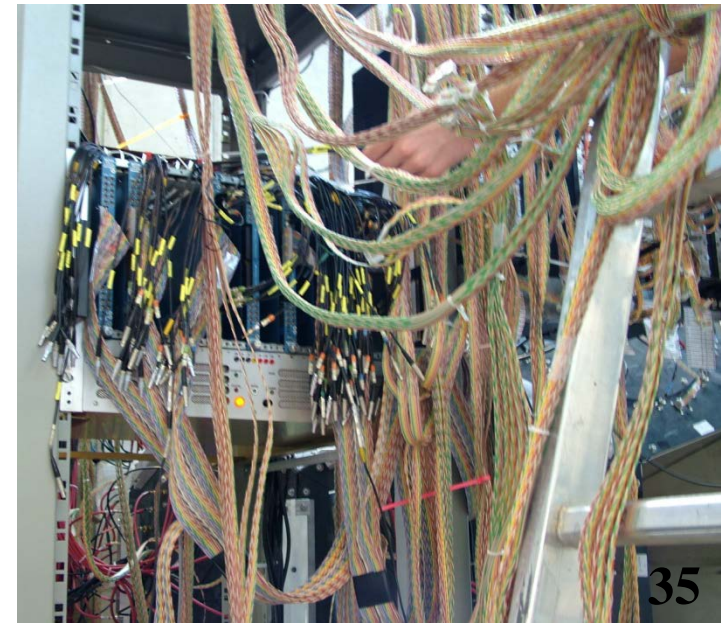
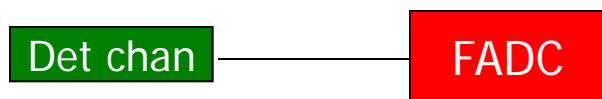


- High-rate applications

- “pipelined operation”
- Low-speed, low-resolution sampling

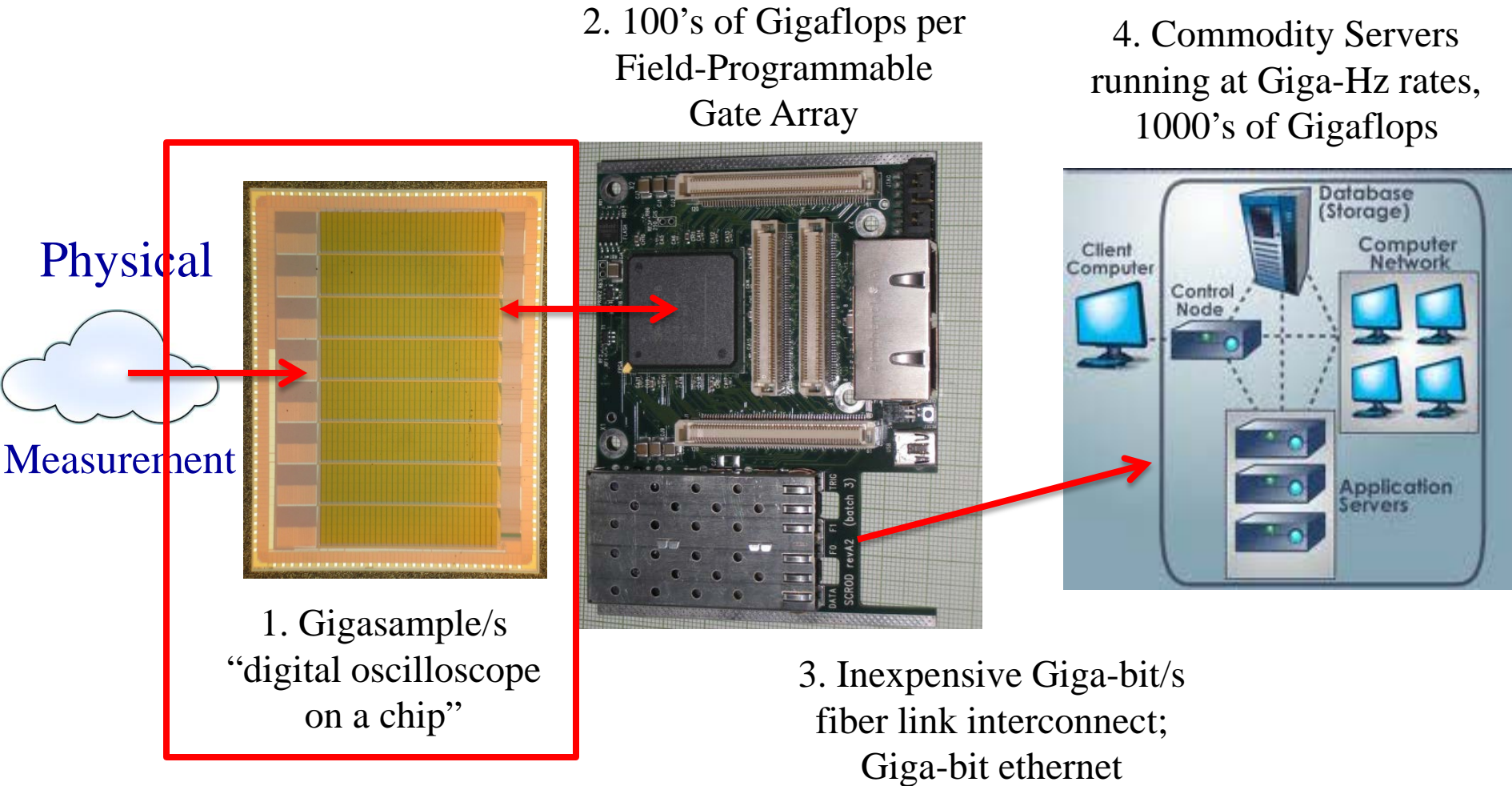
- High channel counts

- Motivation to reduce cabling
- Integrate electronics onto detector elements



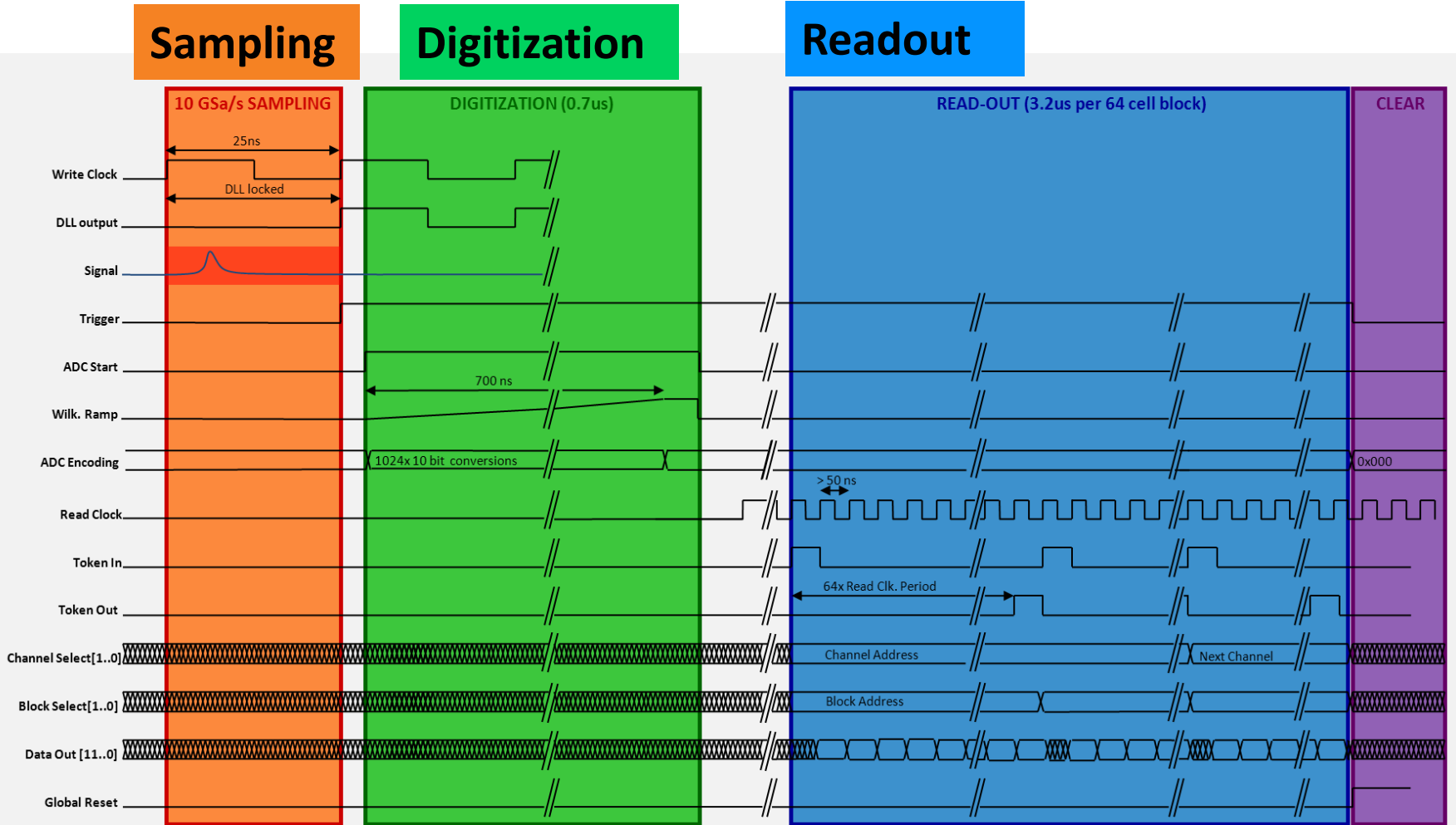
Issues: cost, power, resolution, data volume

Focus on the first of these



- Defines limit of the physical measurement

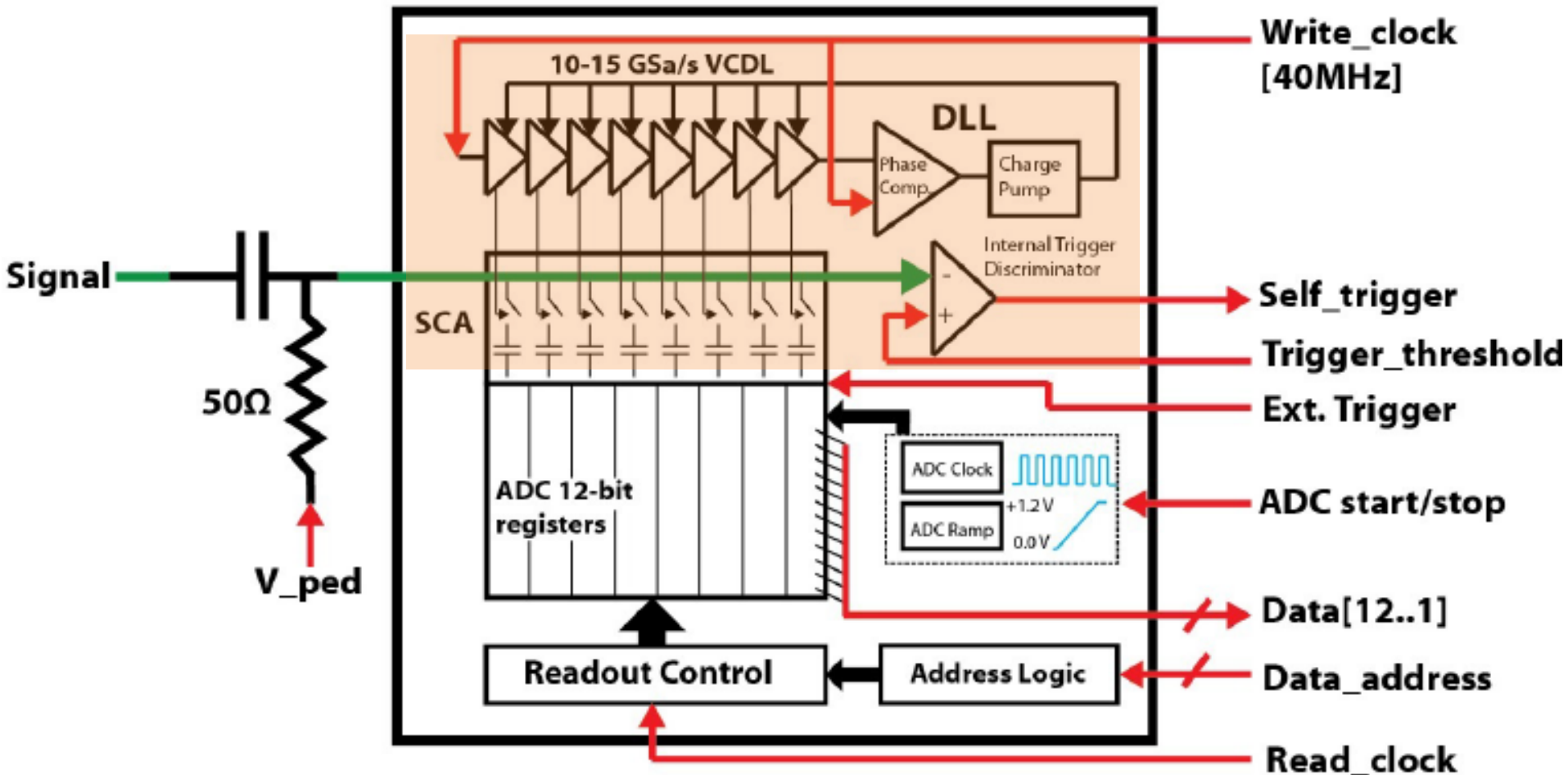
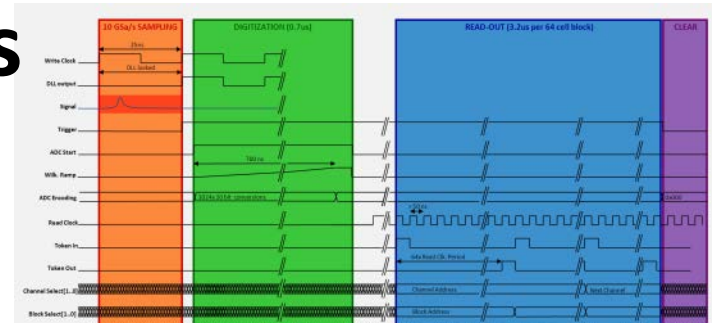
1) Design: How PSEC4 works



- *PSEC-3 timing shown (roughly the same), though PSEC-4 can run readout 2x faster – highly serial...

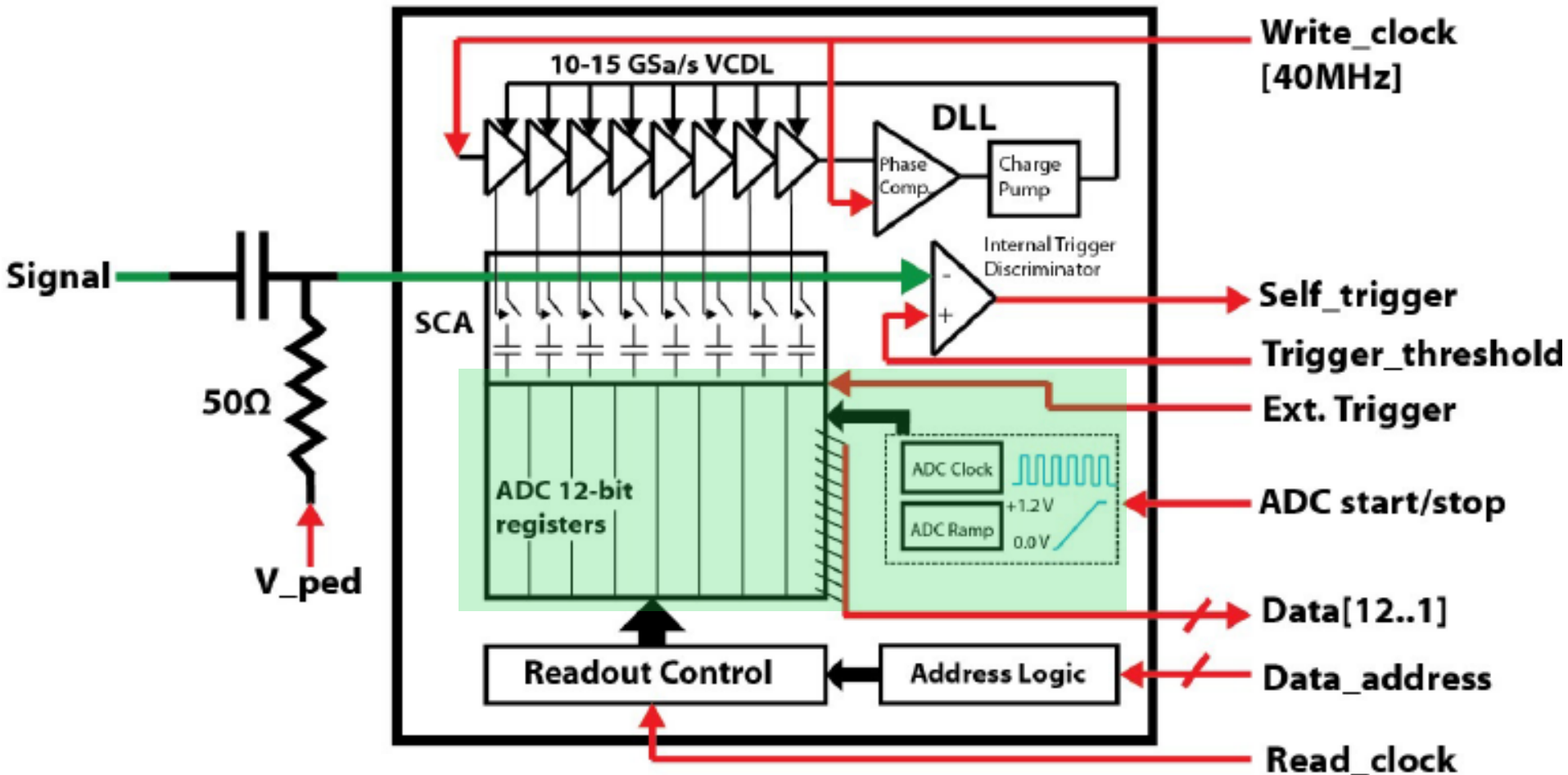
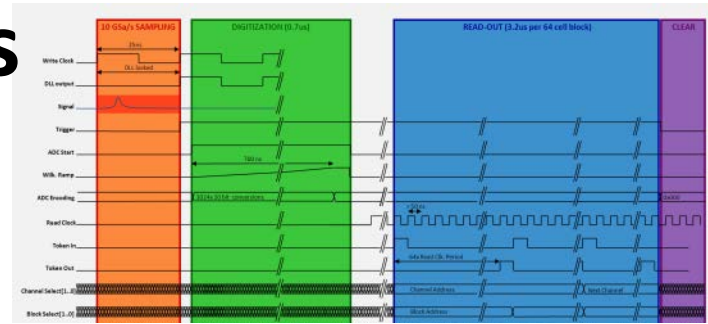
1) Design: How PSEC4 works

Sampling



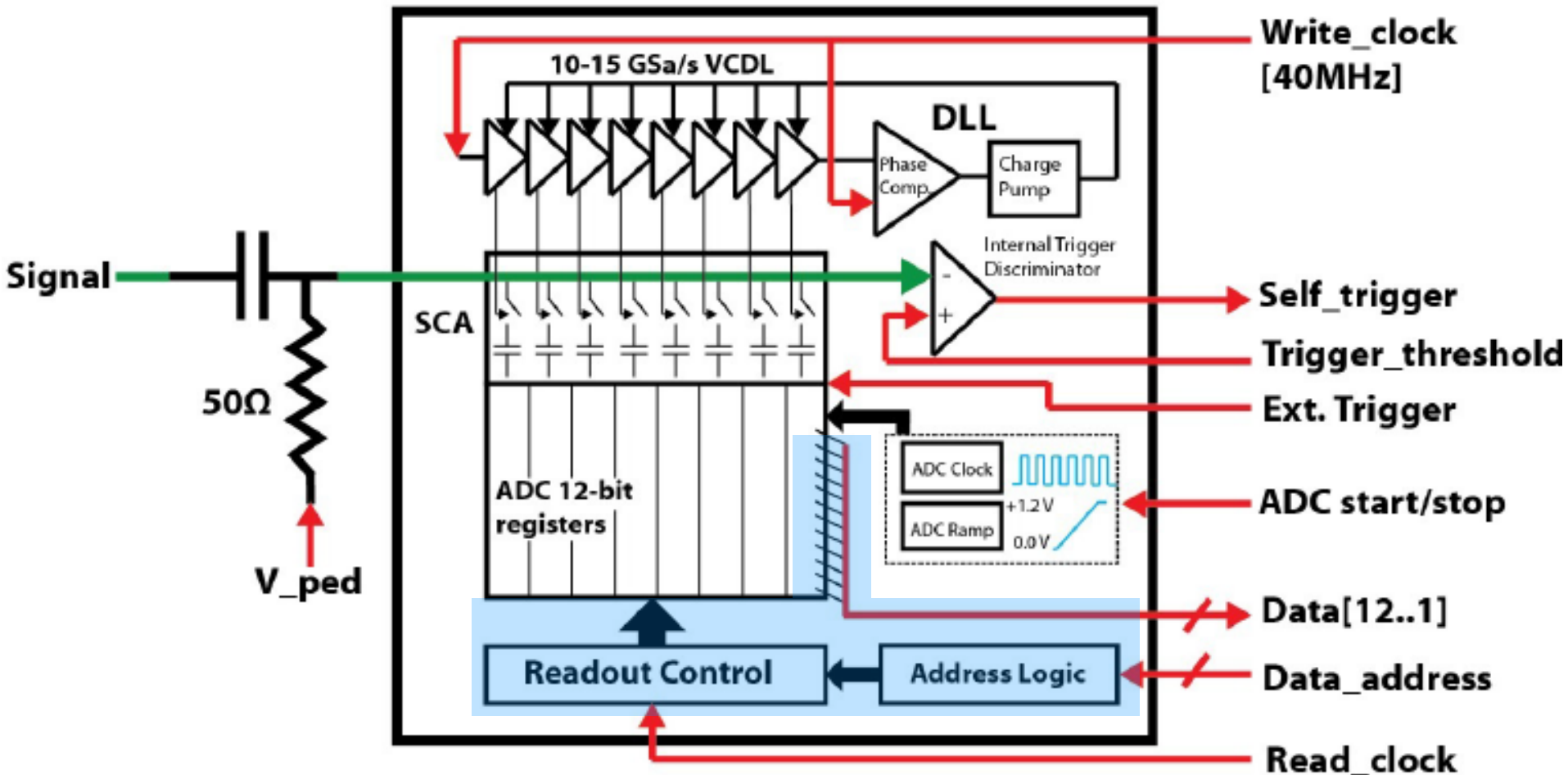
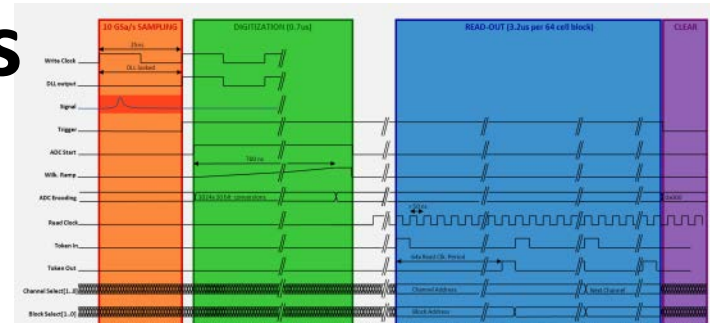
1) Design: How PSEC4 works

Digitization



1) Design: How PSEC4 works

Readout

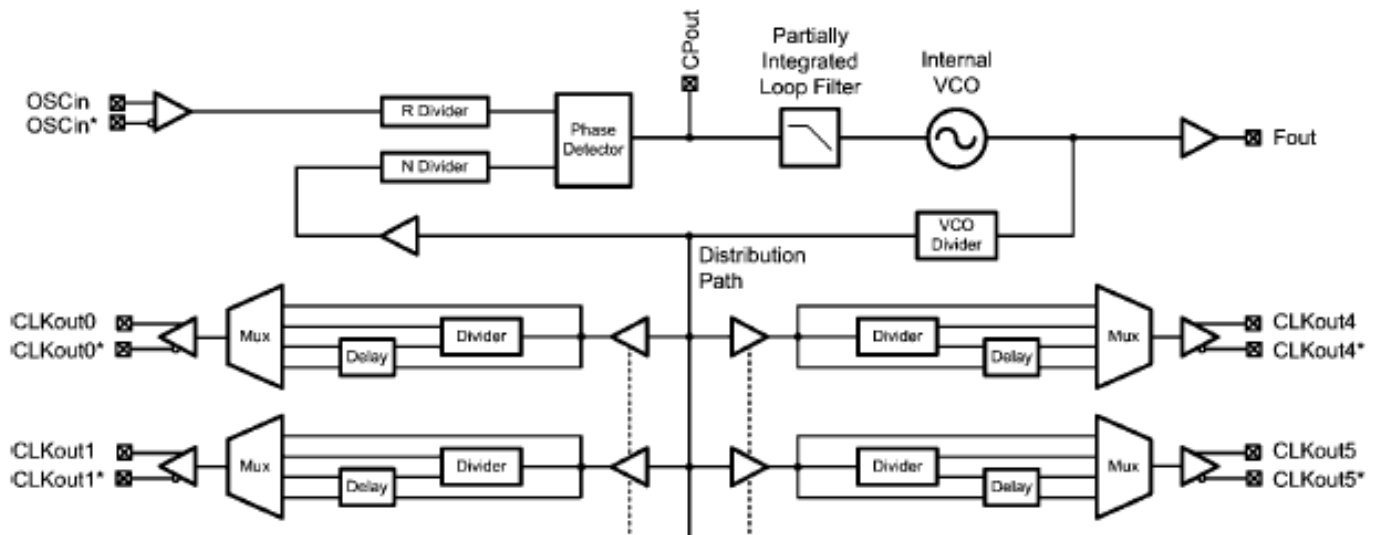


Timing Big Systems I

LMK03000 Clock Conditioner
(National Semiconductor)

Jitter: 400 fs

Global Clock
~20 MHz



Reference Clock for
DRS4 PLL
2.5 MHz



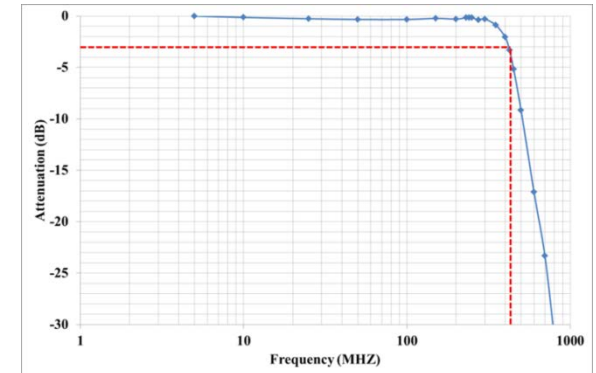
Reference Clock for
timing
channel



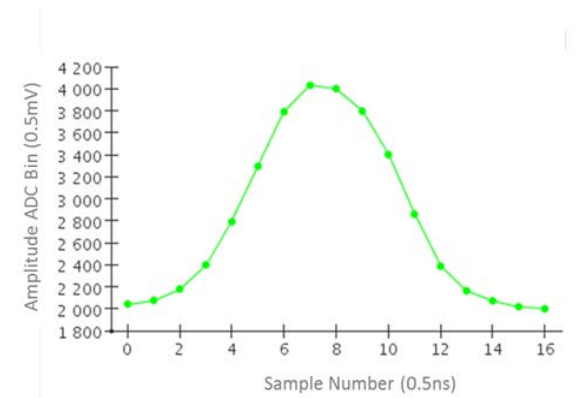
The NECTAR chip: summary

NIM A, vol639, issue 1, p 62-64, 2011

	NECTAR0 Features or Performance	Unit
Technology	AMS CMOS 0.35 μ m	
Number of Channels	2 full differential	Channels
Memory depth	1024	Cells
Power Consumption	< 300	mW
Sampling Freq. Range	0.5 - 3.2	GSPS
Analog Bandwidth	400	MHz
Read Out deadtime time for an event (2 ch, 16 cells)	2	μ s
Deadtime @ 10 kHz trigger rate	<2%	
ADC LSB	0.5	mV
Total noise (unchanged with freq.)	< 0.8	mV RMS
Maximum signal (limited by ADC range)	2	V
Dynamic Range	>11.3	Bit RMS
Crosstalk	0.4	%
Relative non linearity (integral)	<3%	%
Sampling Jitter	< 30 (estimated from charge measurement)	ps rms



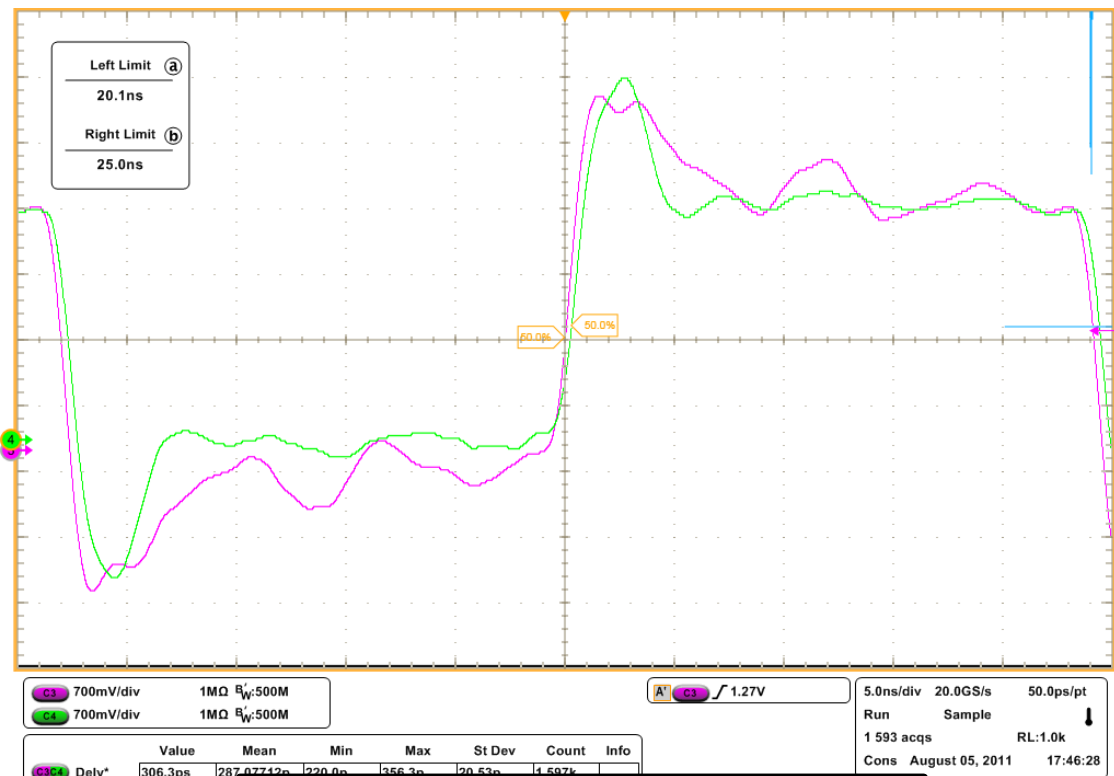
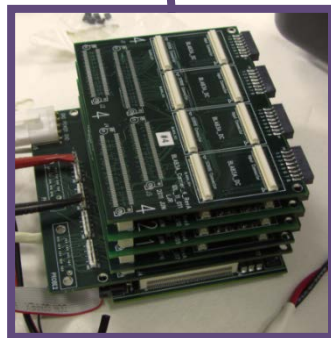
Bode Plot: 400 MHz Bandwidth



PMT signal digitized @ 2GSPS

Clock Distribution Performance

- Test results performed as part of the cosmic ray test stand integration at Nagoya Univ in August 2011:



**Measured phase and jitter of
21.2 MHz clock from two
modules
(on oscilloscope)**

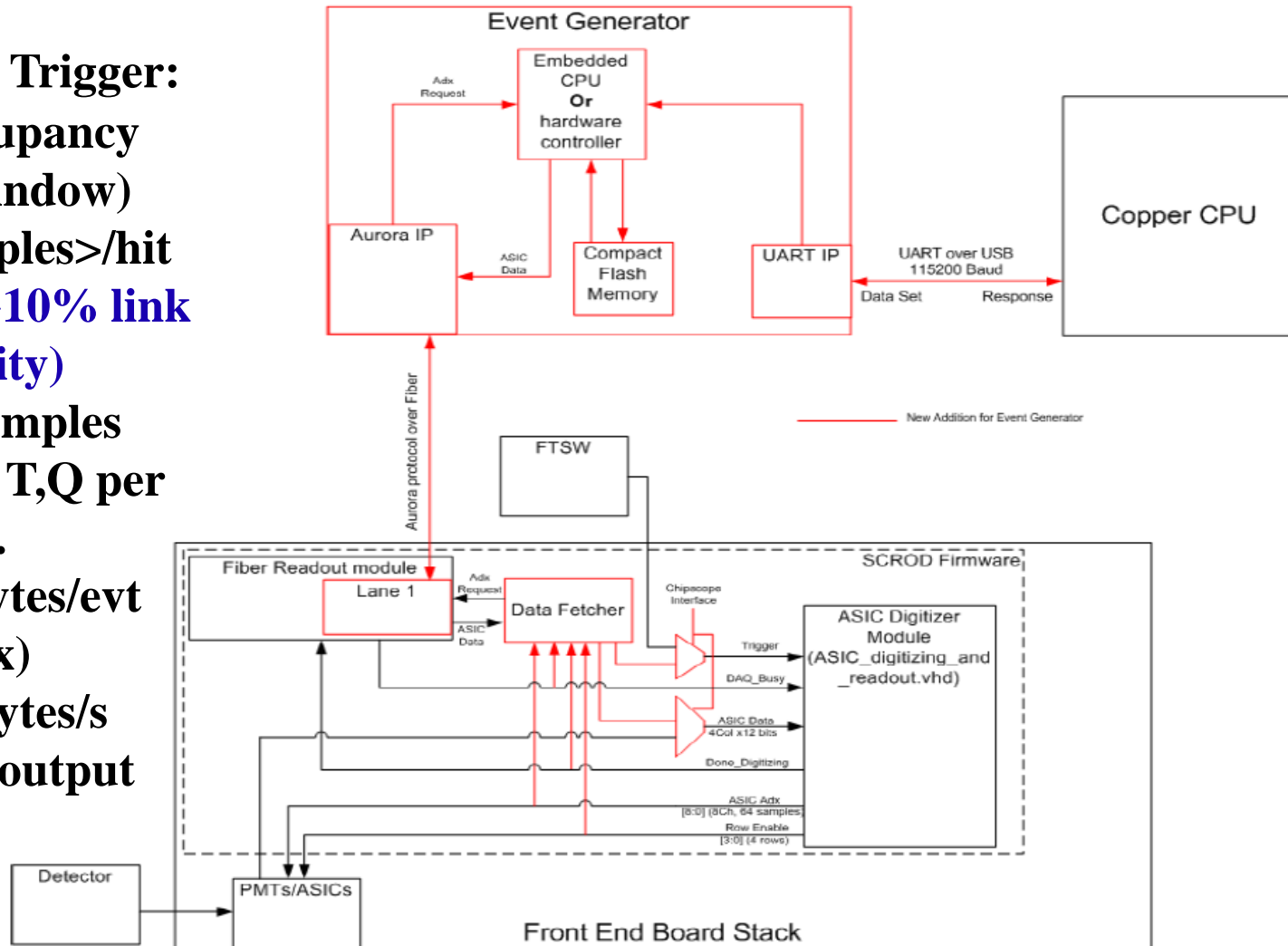
**Clocks are phase-aligned.
→ Measured jitter: 20 ps
RMS.**

Data Reduction Exercises

Event Generator Design

“full speed” testing

- 30kHz L1 Trigger:
2.5% occupancy
(100ns window)
- <100 samples>/hit
- 0.3Gbps (~10% link capacity)
 - ~100 samples reduced to T,Q per p.e.
- Few kBytes/evt (max)
 - 13 Mbytes/s expected output



THINKING
BACK
LOOKING
FORWARD

ALICE, I'VE NOTICED A
DISTURBING PATTERN.
YOUR SOLUTIONS TO
PROBLEMS ARE ALWAYS
THE THINGS YOU TRY LAST.



S. Adams

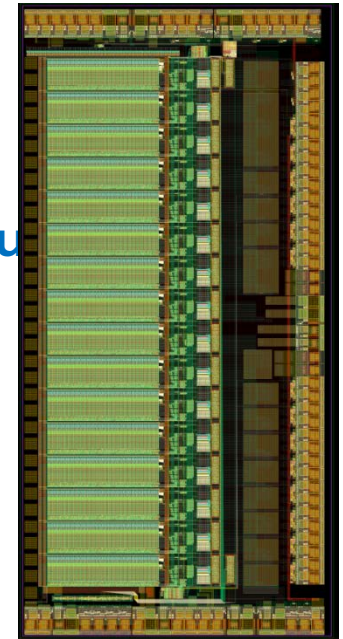
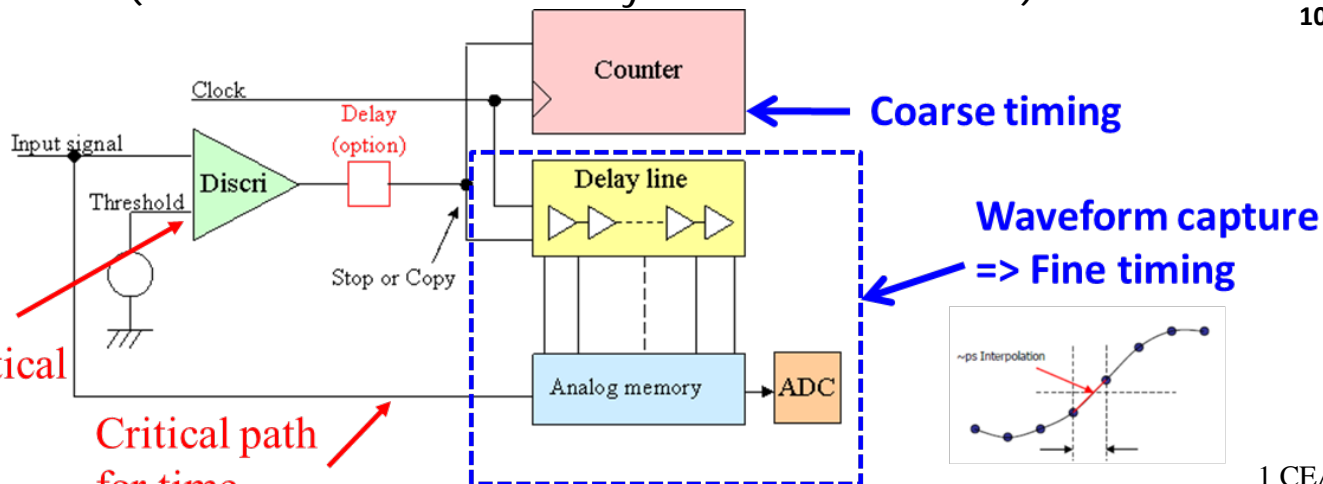
SAMPIC0: a Waveform based TDC chip

SAMPIC0 : a 16 channel WTDC

- proof of concept chip **already usable with detectors**
- Test of CMOS **AMS0.18 μm** (**low cost**, low leakage, 1.8V technology)
- Compatible with buffered architecture (deatime free) => future chips

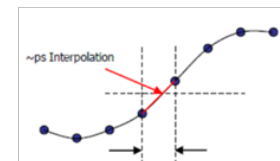
Each channel Self-Triggerable to catch parameters of fast pu

- **Timing :**
 - Coarse = timestamp counter
 - Middle = DLL based TDC *also defining a Zone of Interest for sampling*
 - Fine = few samples in the ZOI of the sampled waveform
- **Waveform Shape, Charge, Amplitude** available through samples
- **No need for high-end discriminator** => low power, versatility
- **Short SCA** (to accommodate the delay of the discriminator)



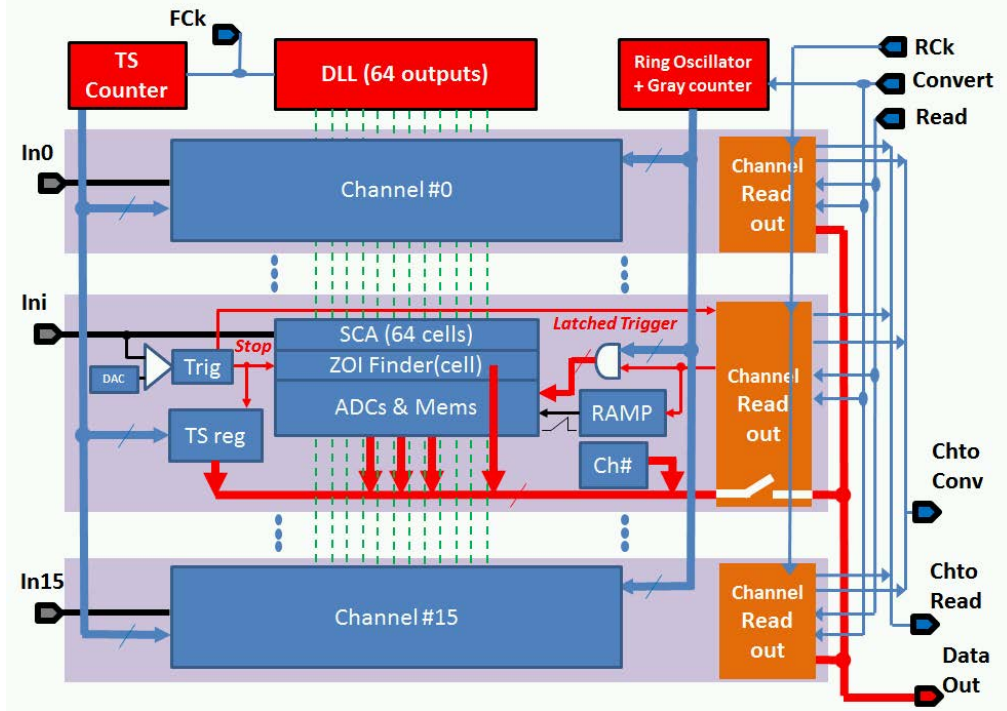
AMS CMOS 0.18 μm
10 mm²

- H. Grabas¹
- E. Delagnes¹
- D. Breton²
- J. Maalmi²



SAMPIC0 Architecture

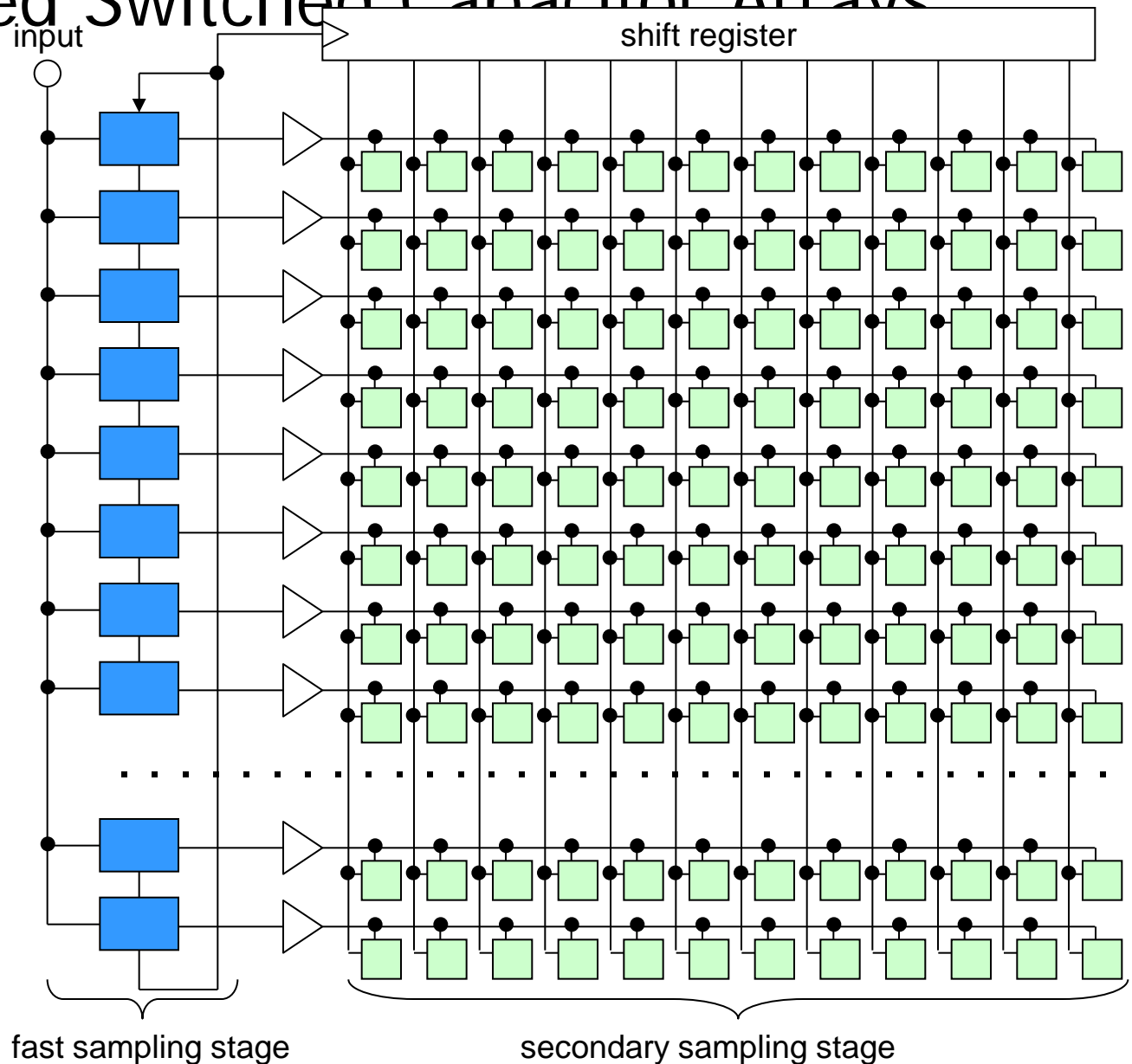
- Common "Slow" (160MHz) 12-bit Gray Counter = **Coarse Timestamping/ch**
- Common Timing generator:** servo-controlled DLL: (1-10 GHz) used for **middle precision timing** & analog sampling commands
- 16 (short) SCA self-triggerable channels:
 - No analog input buffer
 - 64 cells, ~ 50fF capacitor
 - 1.5 GHz Bandwidth
- Several modes of triggering: discri on threshold (+/-), External, Or...
- On-chip fast Wilkinson digitization :
 - 1.3 GHz common gray counter.
 - tunable ramp slope=> trade-off conversion time/precision
1.6µs/11bit to 200ns/8bit
 - Simultaneous conversion of all the SCA cells of the triggered channels



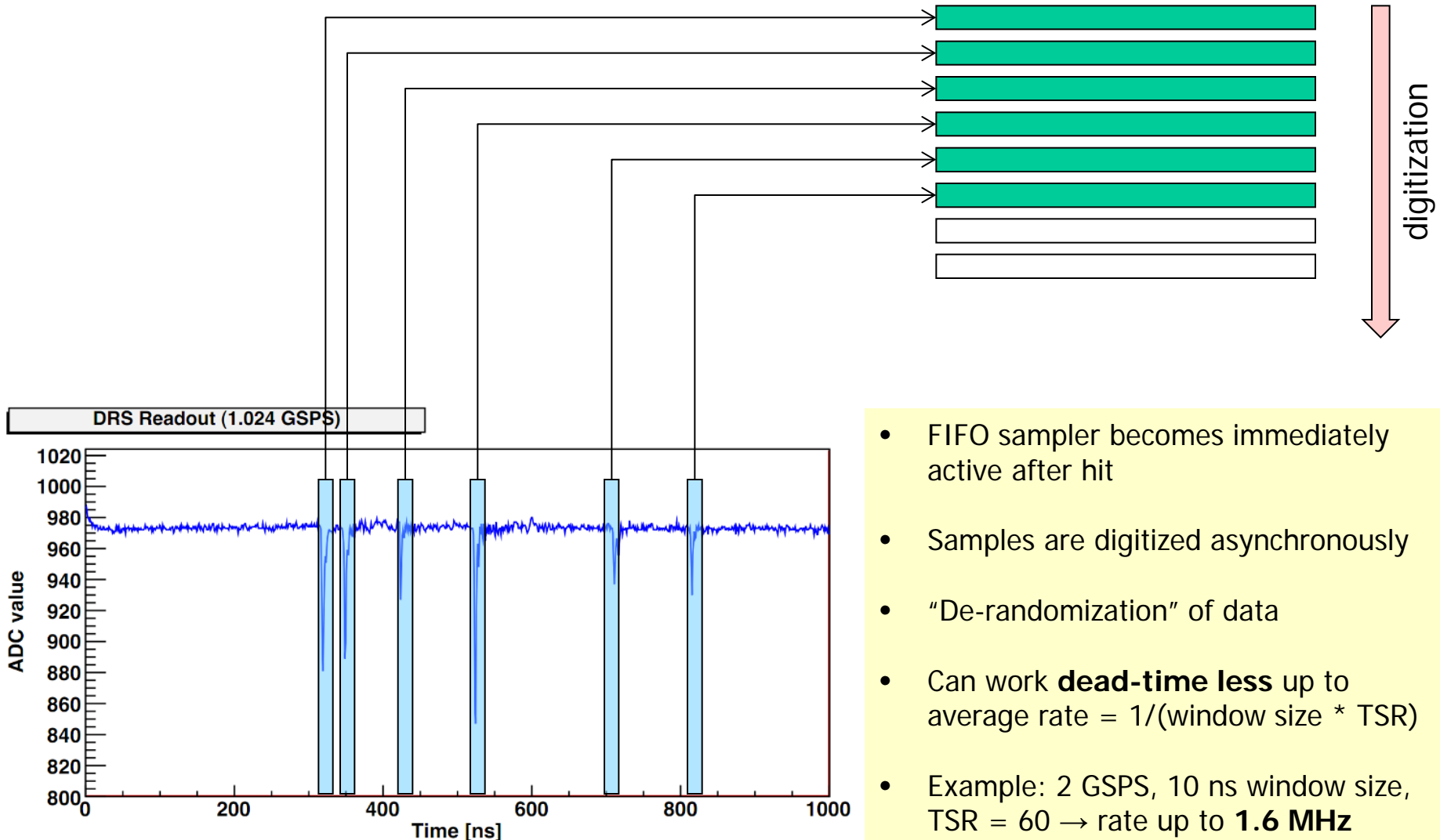
- Deadtime** = only for triggered channels waiting or in conversion => **independent DEADTIME** (can be common if required)
- Read-Out through a 12 bit/160 MHz (up to 400) LVDS bus: negligible readout deadtime
- SPI for configuration (Trigger modes, discriminator thresholds (1/ch),...)

Cascaded Switched Capacitor Arrays

- 32 fast sampling cells (10 GSPS)
- 100 ps sample time, 3.1 ns hold time
- Hold time long enough to transfer voltage to secondary sampling stage with moderately fast buffer (300 MHz)
- Shift register gets clocked by inverter chain from fast sampling stage



FIFO-type analog sampler

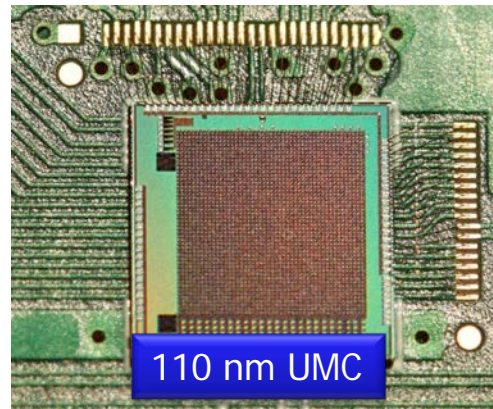
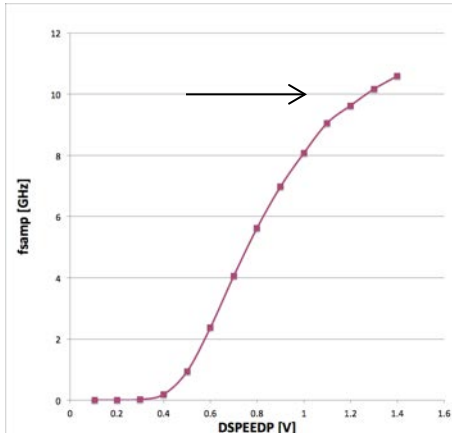
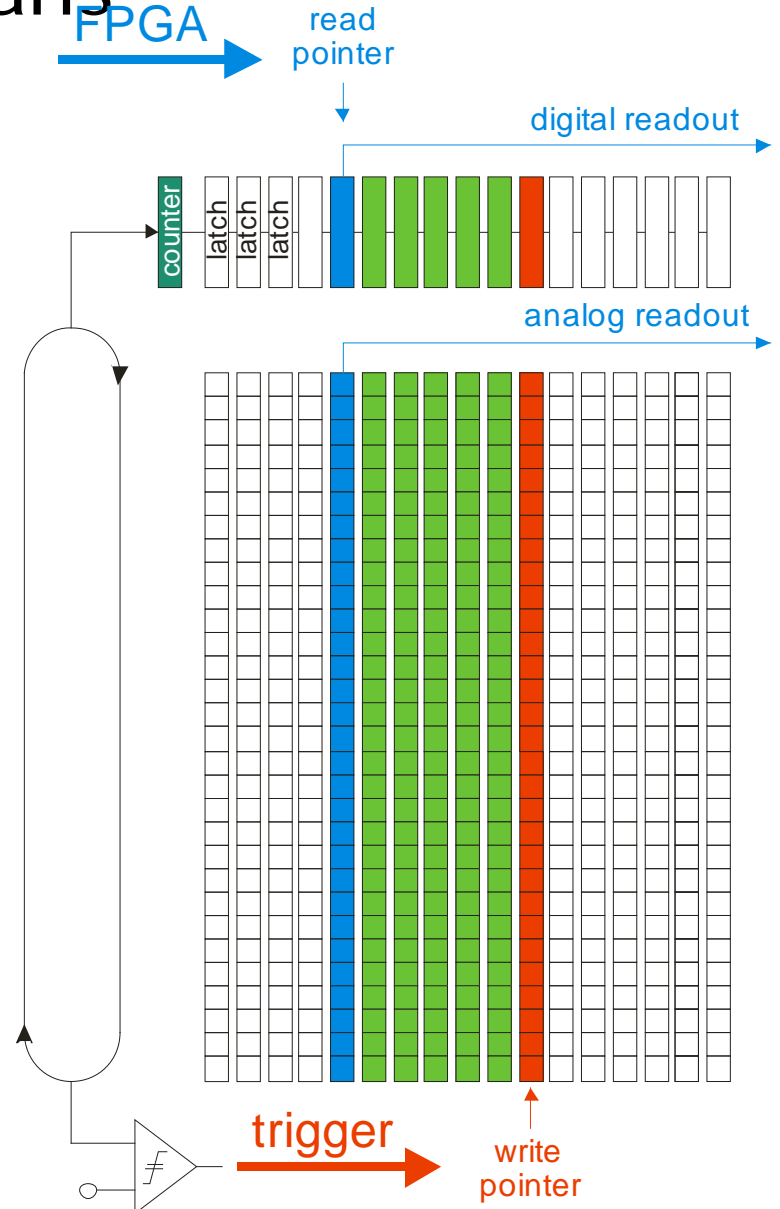


- FIFO sampler becomes immediately active after hit
- Samples are digitized asynchronously
- “De-randomization” of data
- Can work **dead-time less** up to average rate = $1/(\text{window size} * \text{TSR})$
- Example: 2 GSPS, 10 ns window size, TSR = 60 → rate up to **1.6 MHz**

DRS5 Plans

- Self-trigger writing of 128 short 32-bin segments (4096 bins total, 3 GHz analog bandwidth)
- Storage of 128 events
 - Accommodate long trigger latencies
 - Quasi dead time-free up to a few MHz,
 - Possibility to skip segments
→ second level trigger
- Attractive replacement for CFG+TDC
- First tests: > 10 GSPS @ 4 mA, first full version planned for 2014

FPGA

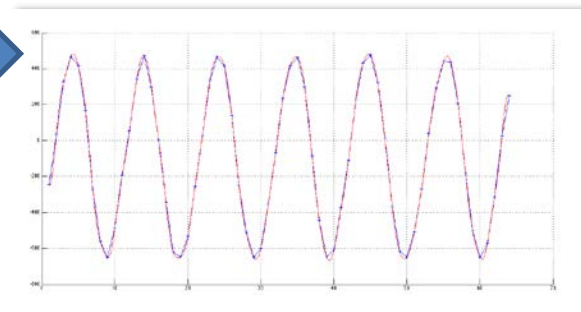


Very first measurement results

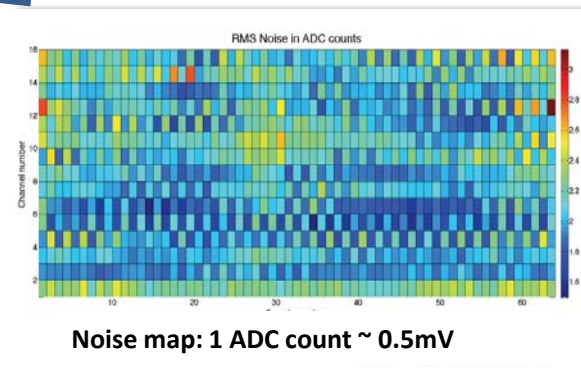
- Performed with a 16-channel mezzanine-board compatible with the system (USB/Eth/optical) previously developed for the SAMLONG chips
- Already usable for small/experiments or detector tests



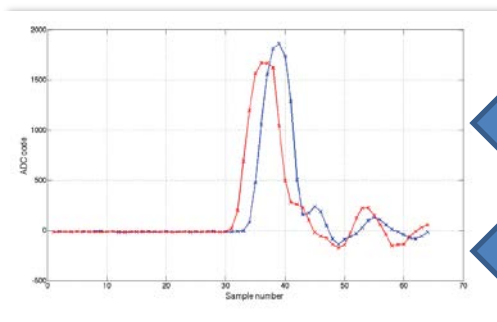
- 180mW power consumption
- Sampling **3.2GSPS- 8.4 GSPS OK** for the 16 channels, and up to **10.2 GSPS** for the 8 first channels
- Discriminator able to trigger on pulses with FWHM < 800ps
- Discriminator noise < 2mV RMS
- SCA noise < 1.3mV RMS in 11-bit mode (1.6mV in 9-bit)
- Range = 1V => **9.6 bit RMS**
- Gain spread between cells = 0.7% RMS, INL = 3% pp.
- 1.6 GHZ SCA Bandwidth (uniform on all cells/all channels)



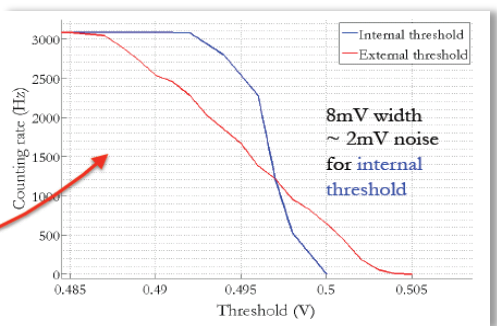
1 GHz, 0.5pp sinewave @ 10.2 GSPS (only pedestal corrections). All the 64 samples are usable.



Noise map: 1 ADC count ~ 0.5mV

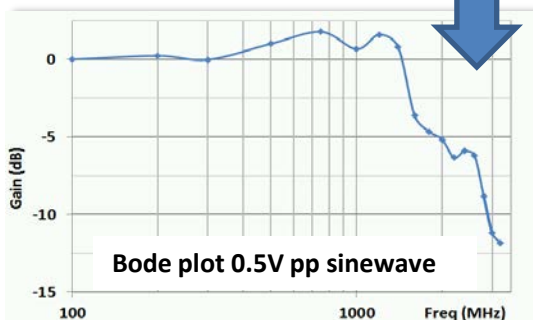


800ps FWHM pulses, self triggered & sampled @ 6.4 GSPS



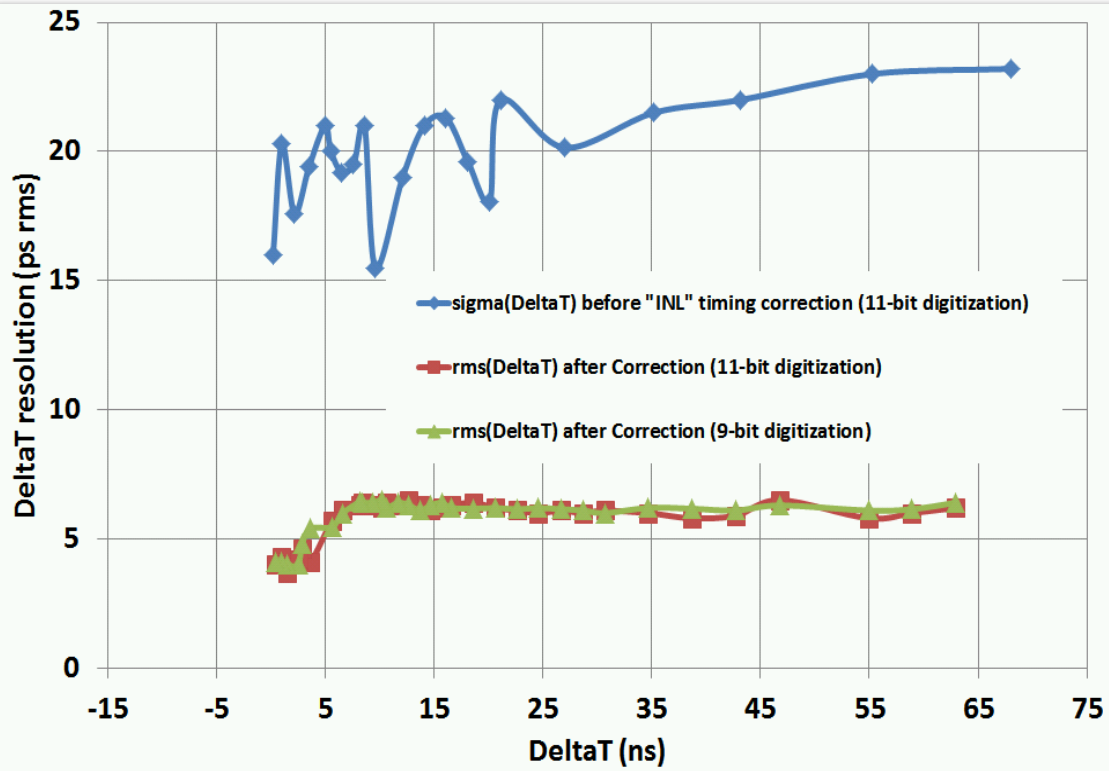
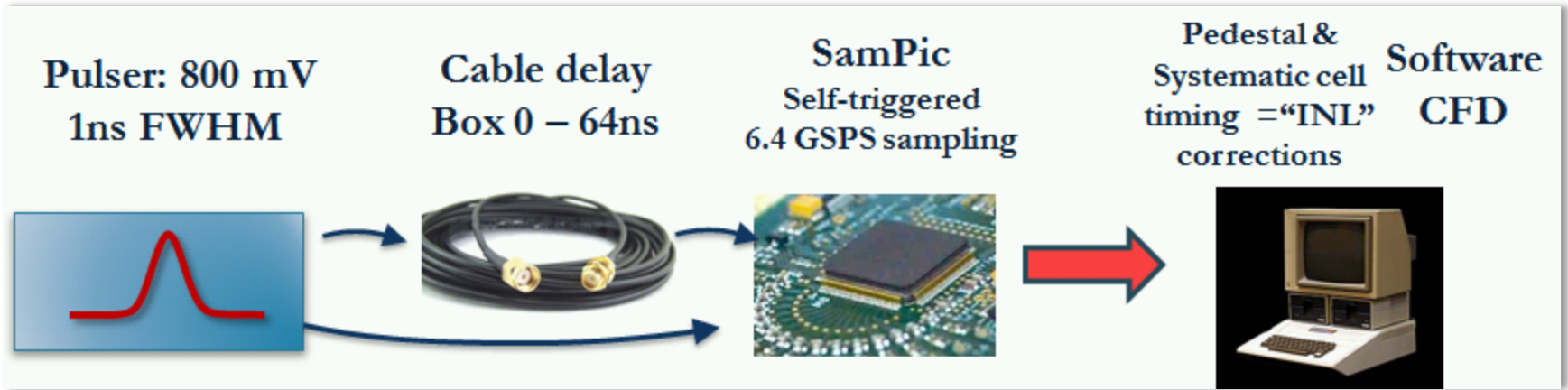
8mV width
~ 2mV noise
for internal
threshold

Discriminator S-Curve, internal & external threshold, 3kHz rate



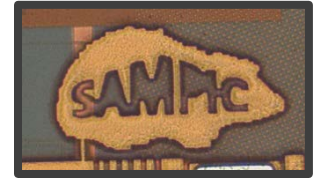
Bode plot 0.5V pp sinewave

First results on timing: DeltaT measurements



- <15 ps RMS = $(22/\sqrt{2})$ timing resolution without any timing calibration (short DLLs)
- <5 ps RMS timing resolution after timing "INL" correction
- Probably setup-limited.
- Same results in 9-bit/400ns mode
- Probably different with smaller pulses
- Correction of ADC gain spread and non-linearity not applied yet

SAMPIC0: Summary



		Unit
Technology	AMS CMOS 0.18 μ m	
Number of channels	16	
Power consumption	180 (1.8V supply)	mW
Discriminator noise	2	mV RMS
SCA depth	64	Cells
Sampling Speed	<3-8.4 (10.2 for 8 channels only)	GPS
Bandwidth	1.6	GHz
Range (Unipolar)	1	V
ADC resolution	8 to 11 (trade-off time/resolution)	bit
SCA noise	<1.3	mV RMS
Dynamic range	9.6	Bit RMS
Conversion time	0.2-1.6 (8bit-11bit)	μ s
Readout time (can be probably be doubled)	25 + 6.2/sample	ns
Time precision before correction	15	pS RMS
Time precision after timing INL correction	< 5	pS RMS

Simulated Performance vs. SNR

300MHz ABW, 5.9GSa/s

