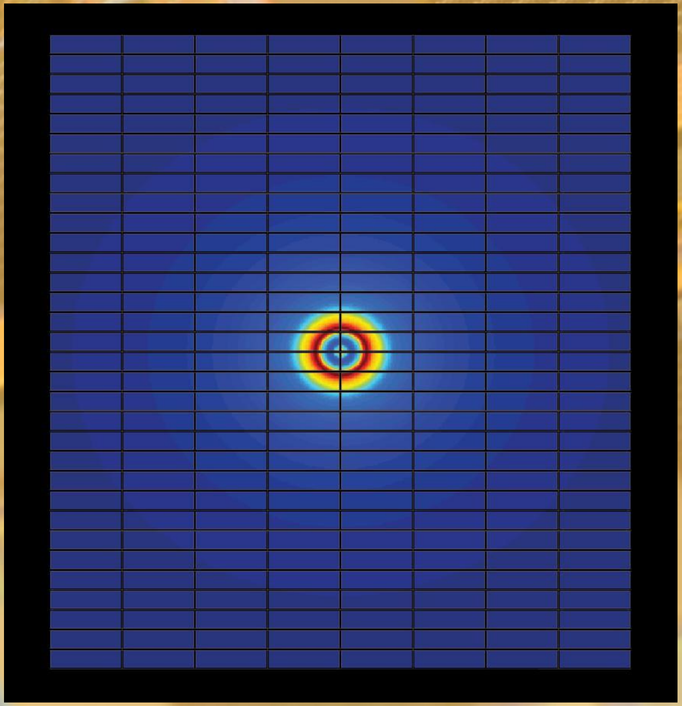
XFEL Chip Development (the UK-LPD Project)

Speaker: Marcus French (STFC)
Project Manager: Matthew Hart (STFC)



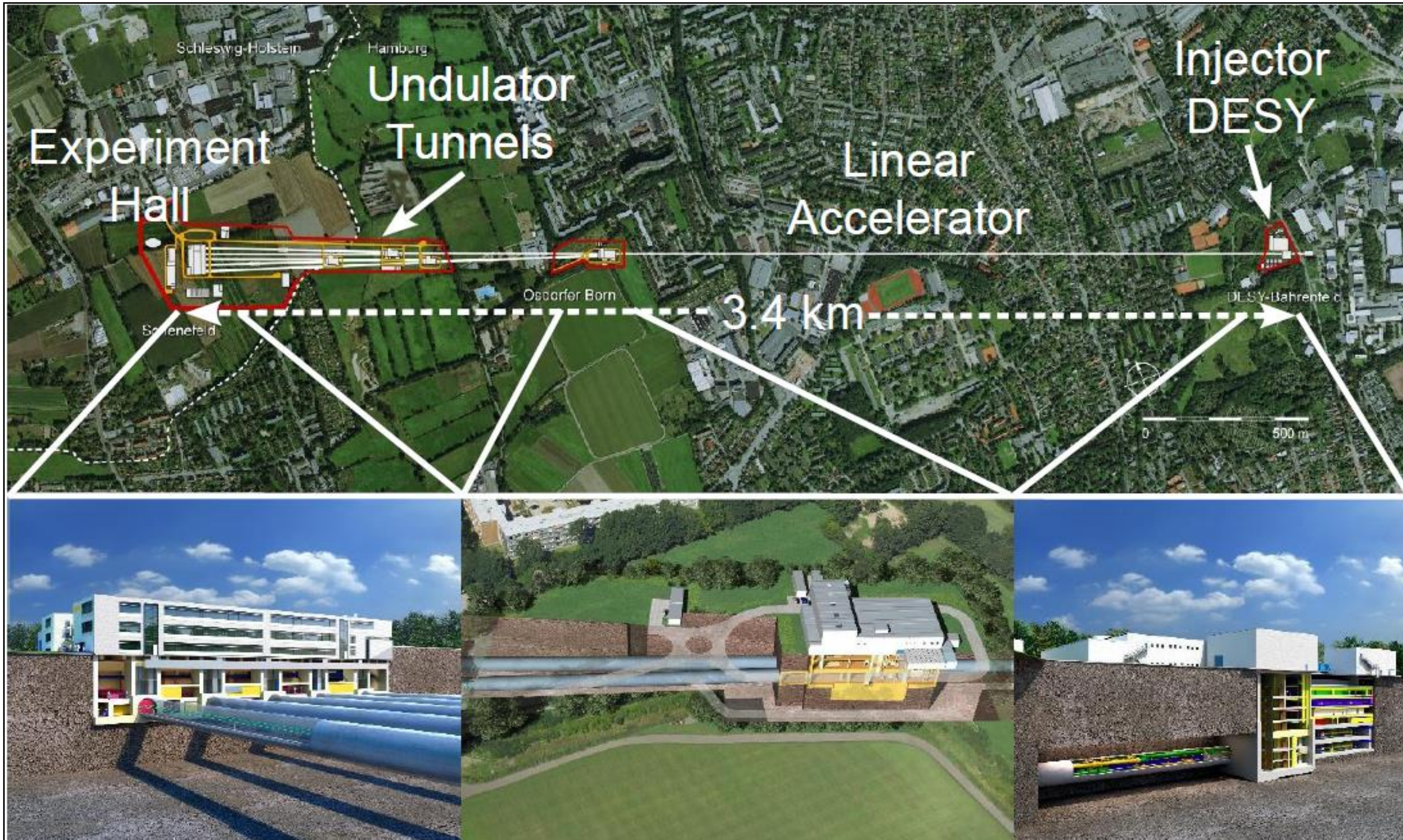
European XFEL

Science & Technology Facilities Council

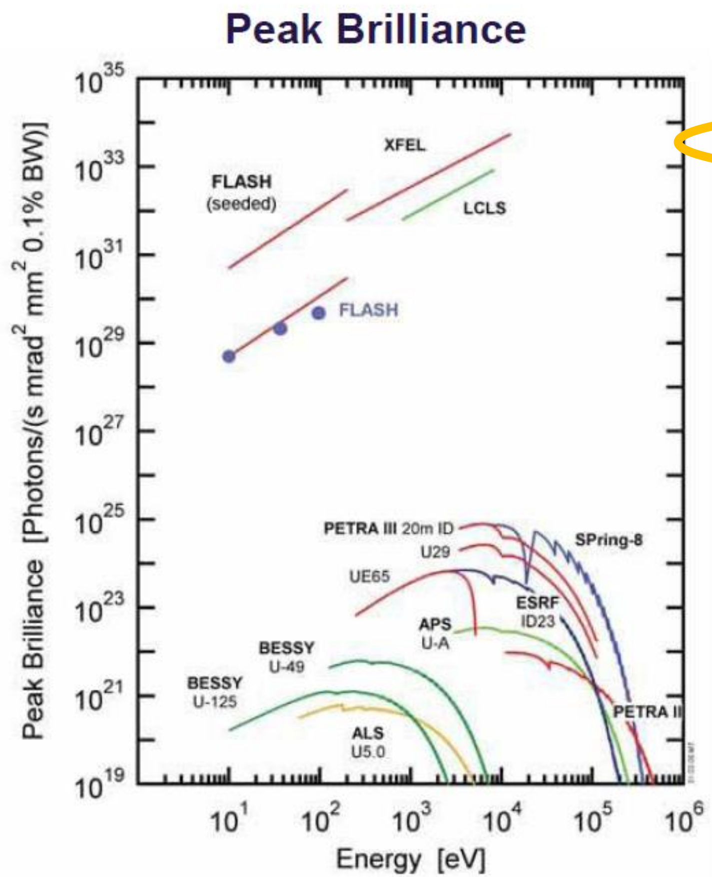
Presentation Outline:

- **Intro to XFEL Requirements**
- **Motivation for the LPD approach**
- **Overview of chip development**
  - Test chip and production versions
  - Summary of architecture
  - Lessons learnt in the programme
- **Where we are now**
- **Looking ahead:**
  - Upgrade options for the future

The European XFEL



Machine Peak Brilliance



Specifications

- Photon energy 0.4 – 20 keV
- Pulse duration < 100 fs
- Pulse energy few mJ
- Superconducting LINAC
  14-17.5 GeV
- 10 Hz (2700 bunches/s)
- 5 beamlines / 10 instruments
  (start up version 3 beamlines with 6 instruments)
- Extensions possible:
  - Additional instruments
  - Additional beamlines

  Start of operation 2015

Pulse duration means effectively simultaneous delivery of signal photons to pixels

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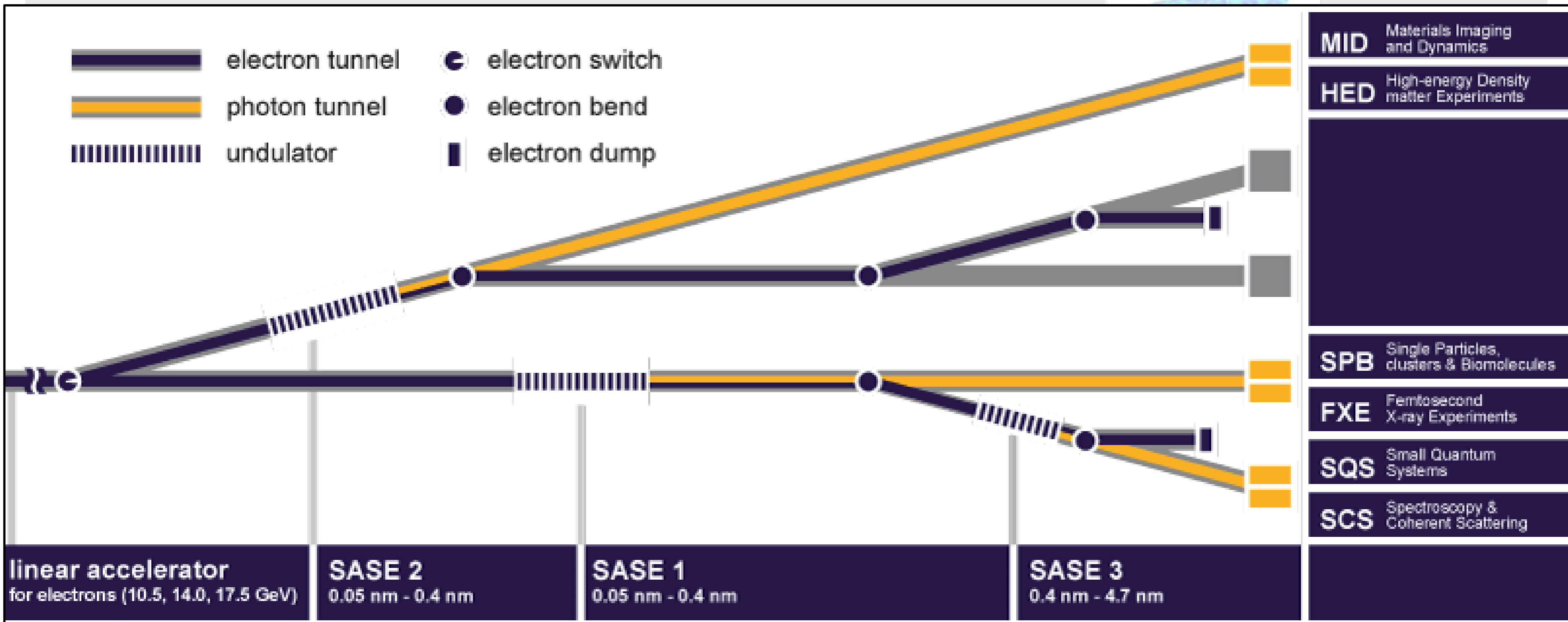
XFEL Science

1

Ultrafast Coherent Diffraction Imaging of Single Particles, Clusters and Biomolecules (SPB)



SASE

Low

intense fields and non-linear phenomena.

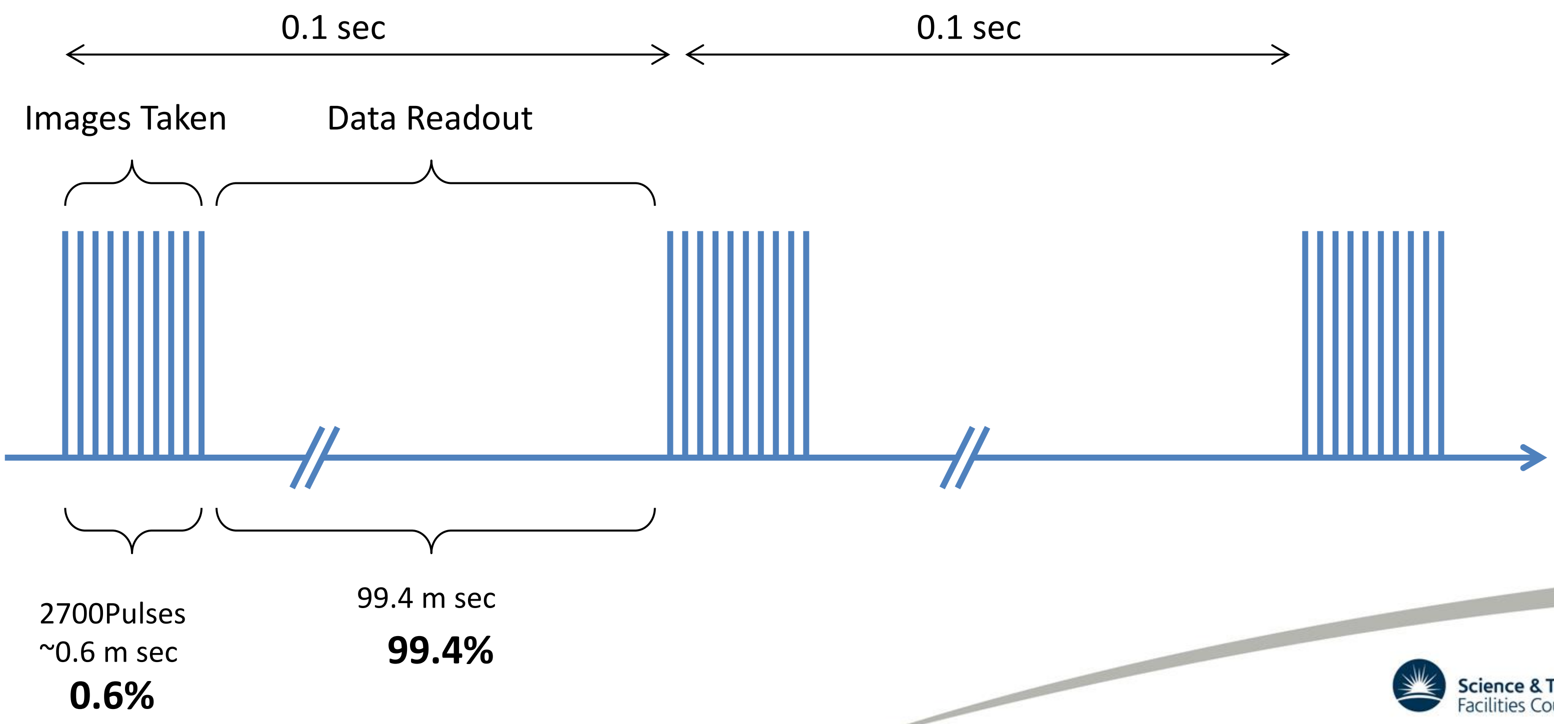
Spectroscopy and Coherent Scattering (SCS)

Structure and dynamics of nano-systems and of non-reproducible biological objects

Key Issue: XFEL Beam Timing

Consequence for ASICs:

- Rapid recording requires in ASIC storage
- Inter bunch time available for converting and reading out data
- Memory must retain values for 0.1 seconds without droop



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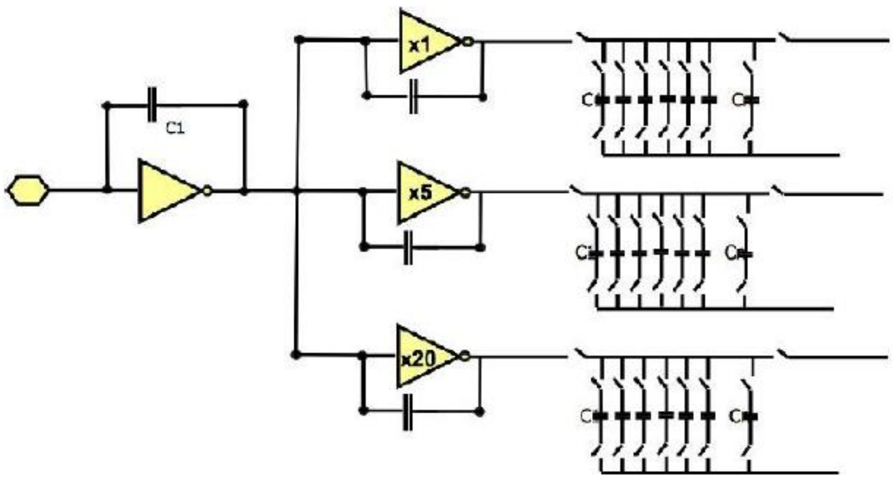
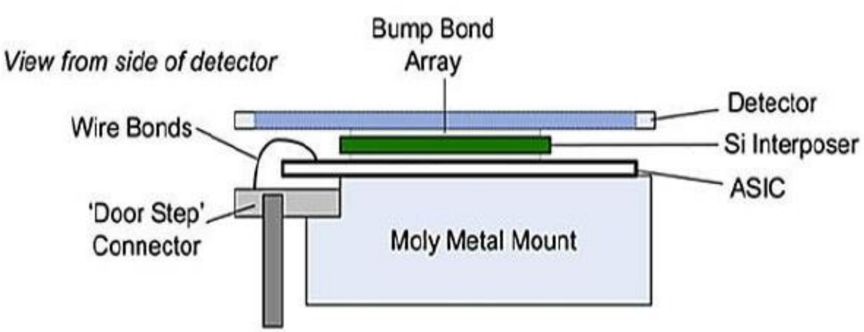
LPD Proposal 2006

LPD Pixel Cell

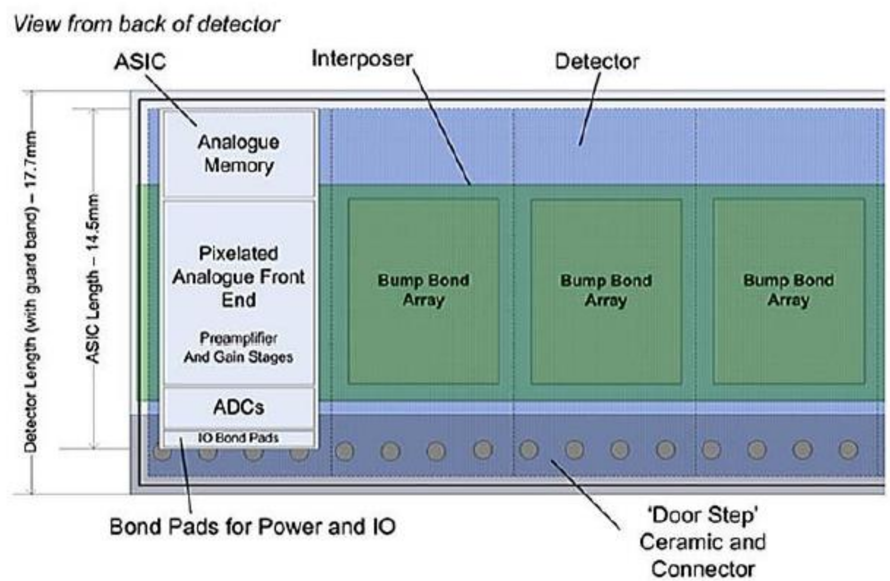


LPD ASIC and Sensor



Front End ASIC

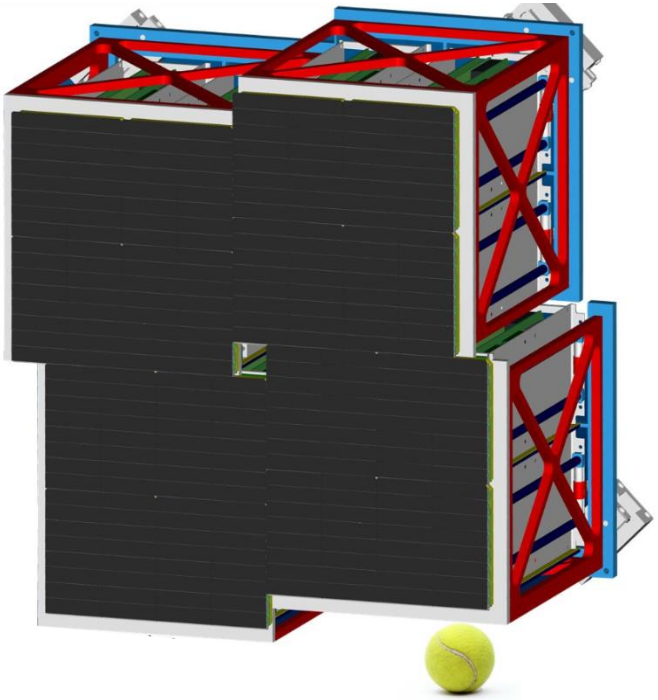
- 3 fold multi-gain concept and analog storage pipeline
- 512 channels per ASIC
- 16x 12 bit on chip ADC
- Design IBM 130 nm technology



LPD System Summary

1 Megapixel System

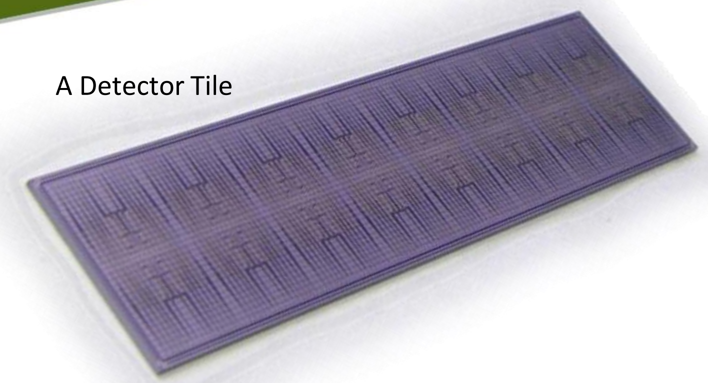
- **1 Megapixel** - 500um pixels
- **4.5MHz frame rate**
- **High dynamic range**, 1 to 1x10^5 photons per pixel per pulse, Achieved using multi-gain architecture.
- Chip control is driven by a **command word interface**. e.g. ‘Veto’ a frame captured.
- **512 frame memory depth** continuously stores all three gains, overwriting whenever a veto is received.
- Output data rate ~**10GByte/s** per megapixel



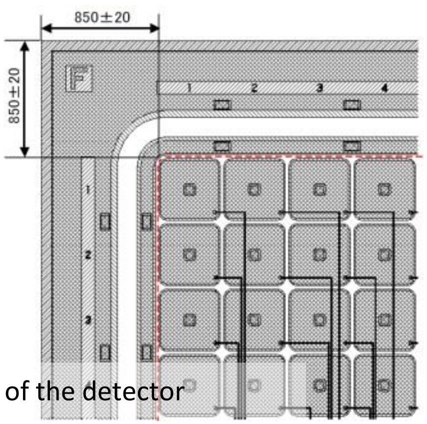
An LPD megapixel detector.
- 16 Super Modules
- 256 Detector Tiles
- 2048 ASICs
- 1,048,576 pixels

LPD Area Coverage

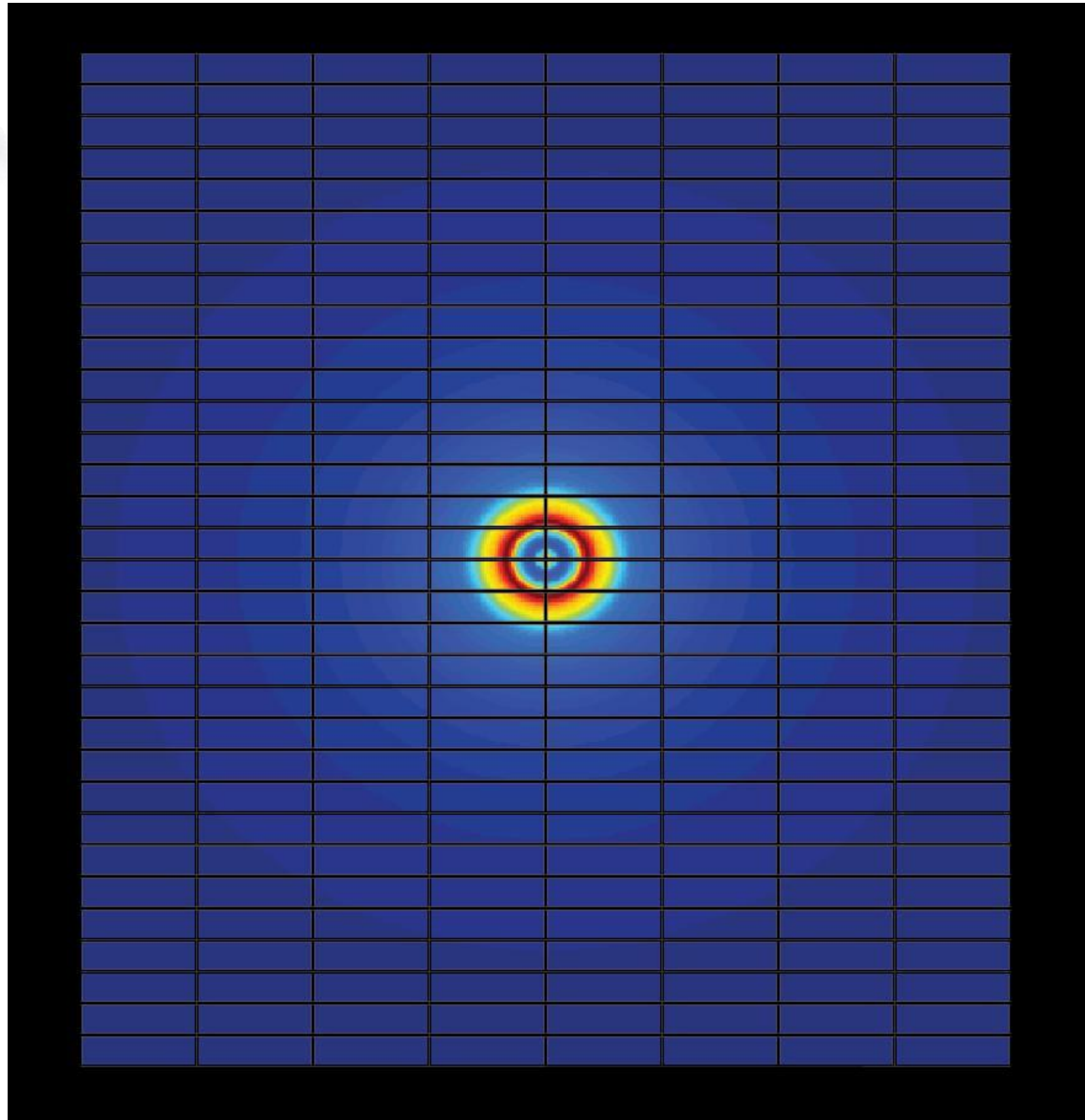
A Detector Tile



- Silicon Detector
- 32 x 128 Pixels (4096 total)
- 500 µm Pitch
- Manufactured by Hamamatsu
- Overall active area 87%

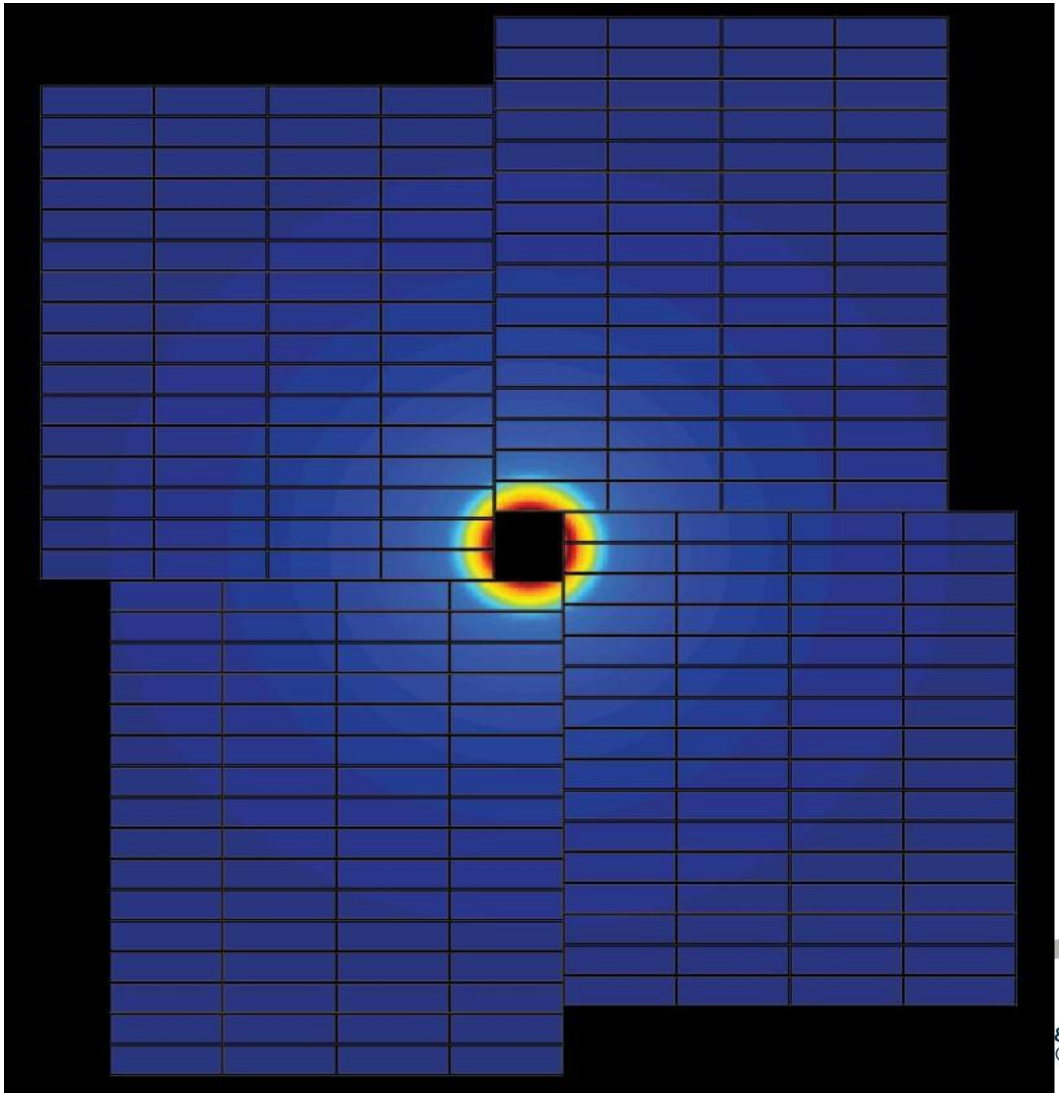


Corner region of the detector



LPD Area Coverage

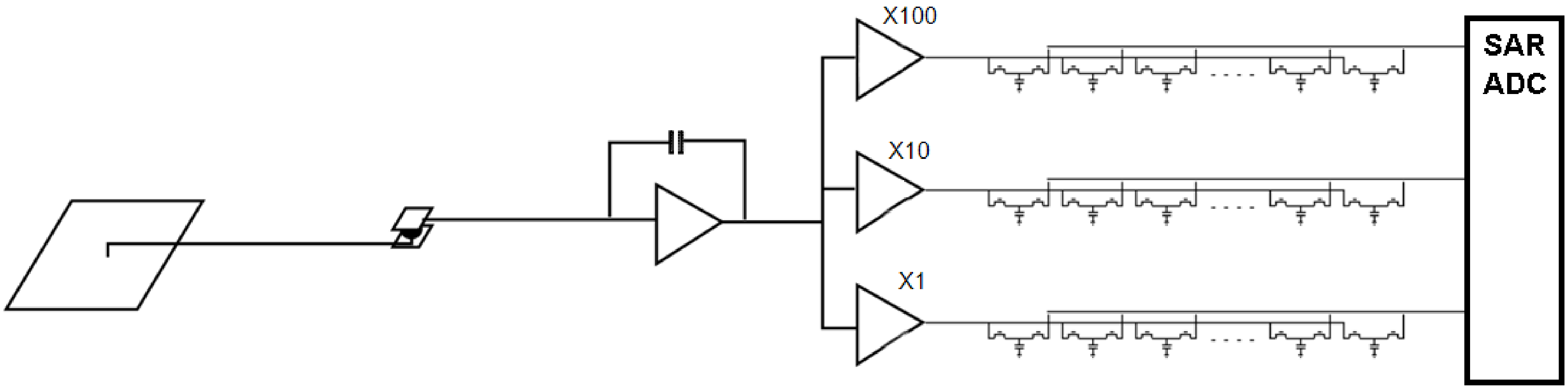
- Sliding Geometry
- Allows repeat exposures to account for dead pixels/tiles
- Computer control available to move the quadrants remotely



LPD Architecture

Advantages:

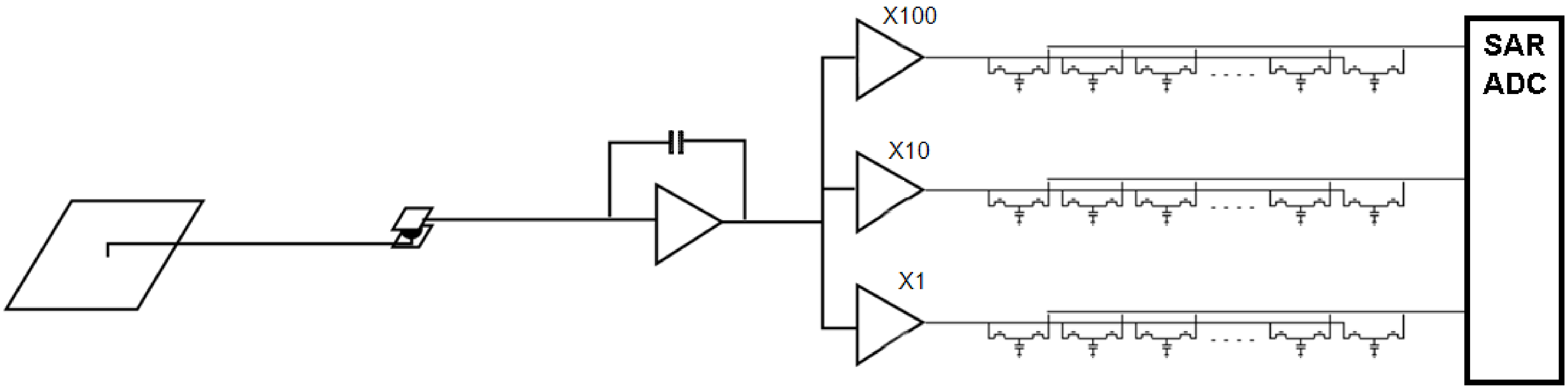
- A fixed feedback capacitor provides a direct and immediate path for the detector current pulse
- There is no capacitor switching at the front end during the pulse
- The amplifier input voltage is stable, even for large pulses (a few mA)
- Memory and ADC can be shielded for radiation hardness
- Offline selection of gain data gives more flexibility for future signal processing



LPD Architecture

Disadvantages:

- The gain of the pre-amp is small: 10uV per 12keV photon (higher noise)
- The extra preamp gain stages and switched capacitors contribute significant additional noise
- 3 memory cells per sample triples ADC conversion overhead
- Higher power for multiple amplifiers and additional readout circuitry



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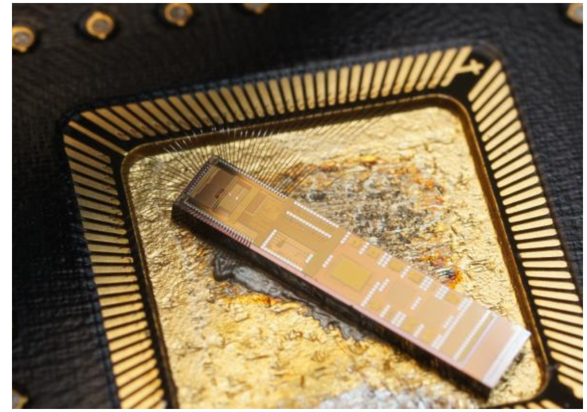
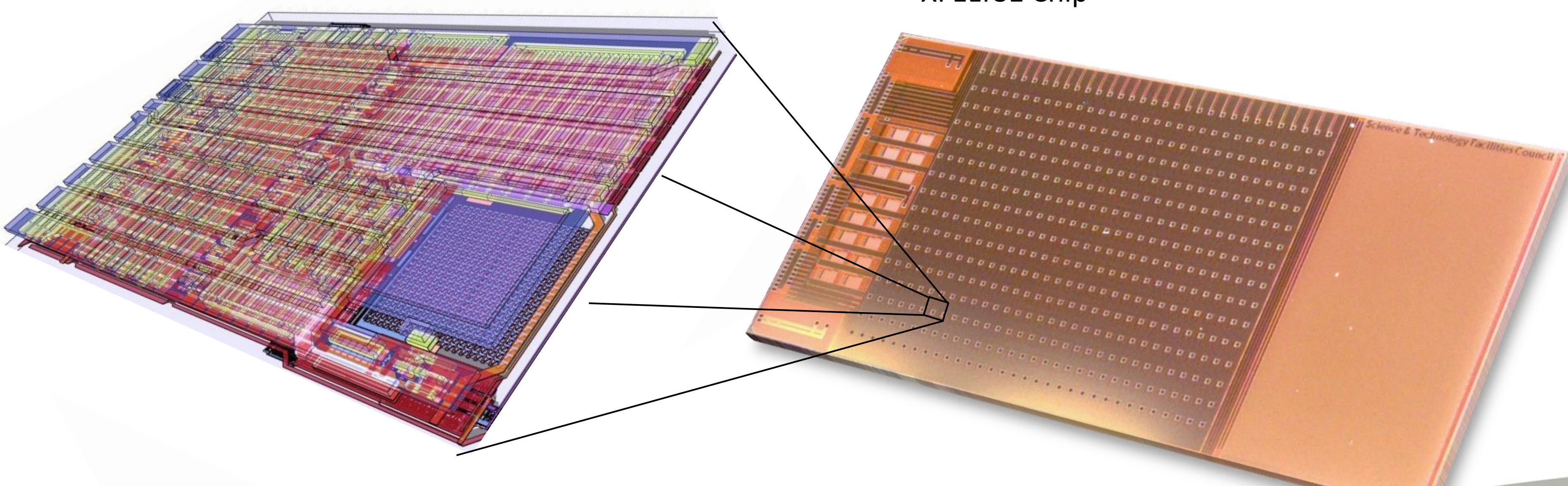
Chip Overview

The ASIC is now in V2 production.

- First test chip XFELTS1
- Then two full ASIC layouts

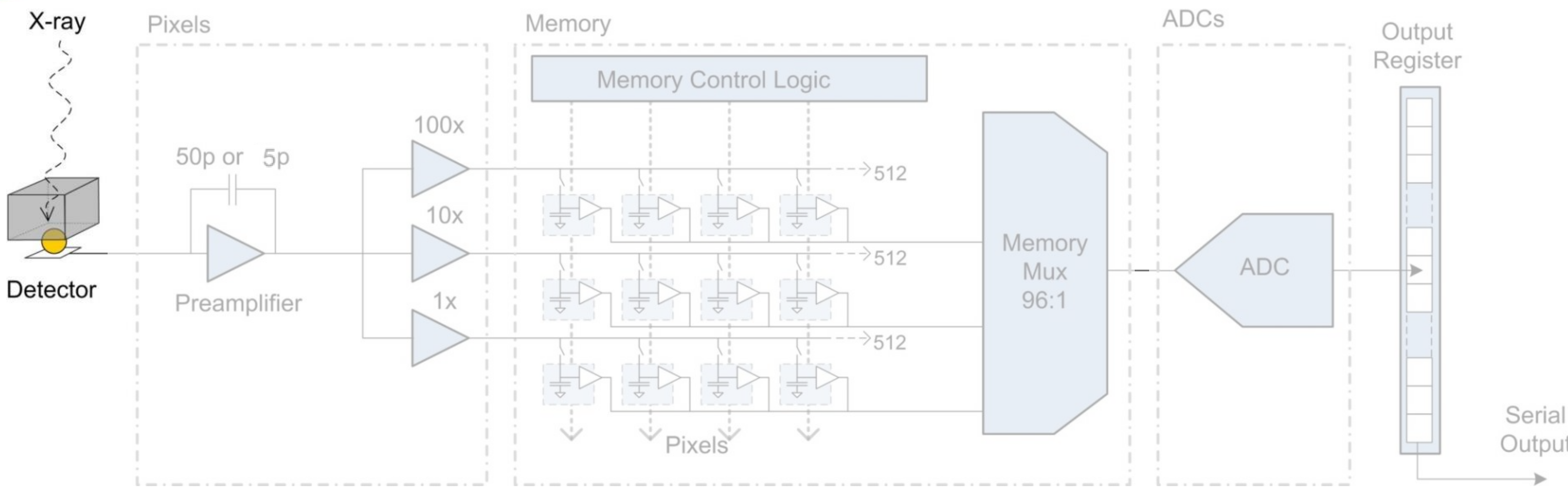


XFELTS1 Chip

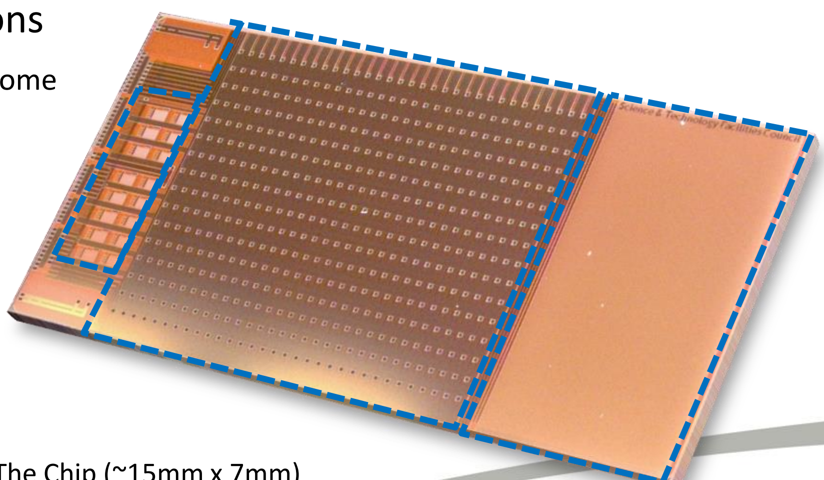


V1 ASIC (~15mm x 7mm)

Readout ASIC

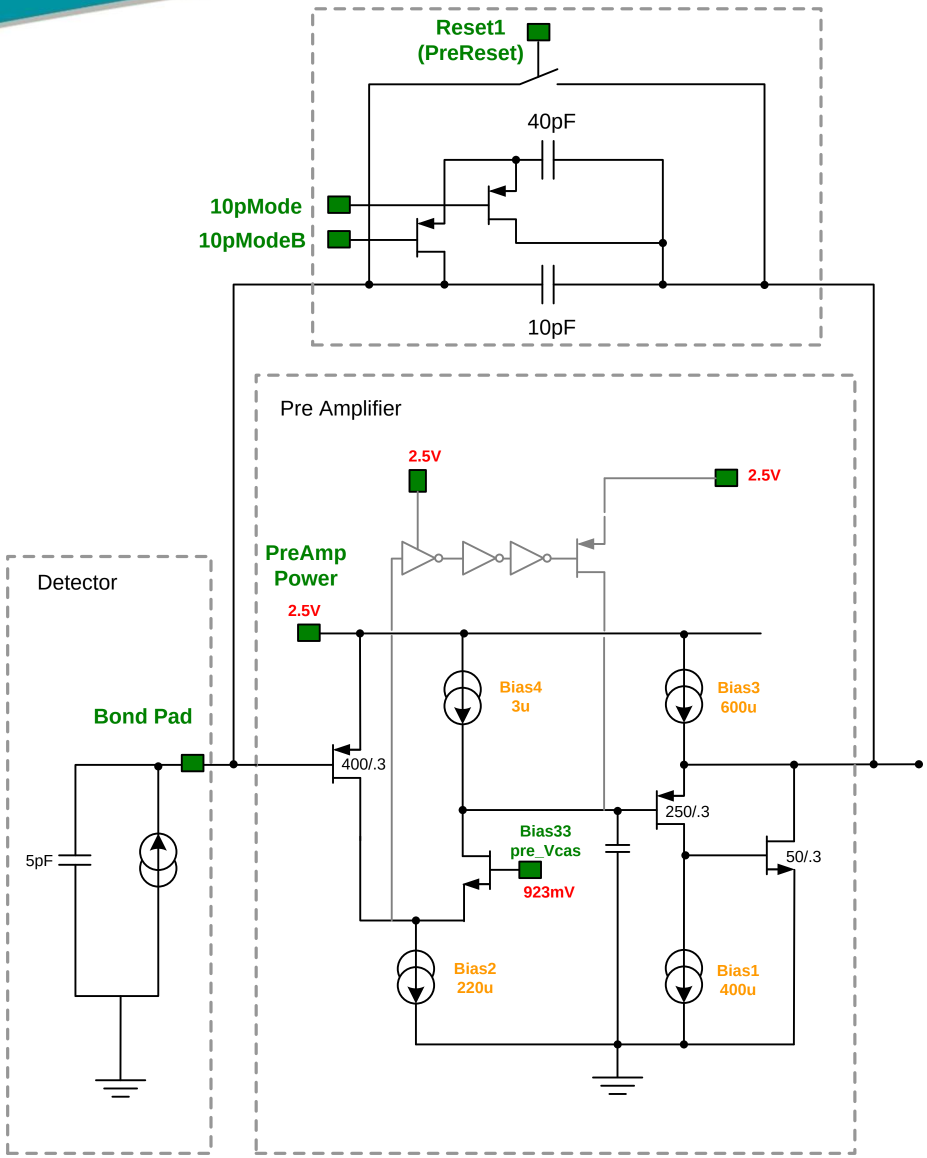


- 512 Channels
- Preamplifier with 50pF feedback – 10^5 12keV photons
  - An additional high mode gives lower noise at the expense of some dynamic range.
- 100x, 10x and 1x parallel gain stages
- 512 frames of memory for each channel and gain
  - Veto System
- 16 SAR ADCs – 12 Bit
- 100MHz digital output
- IBM 130 nm



The Chip (~15mm x 7mm)

Preamplifier

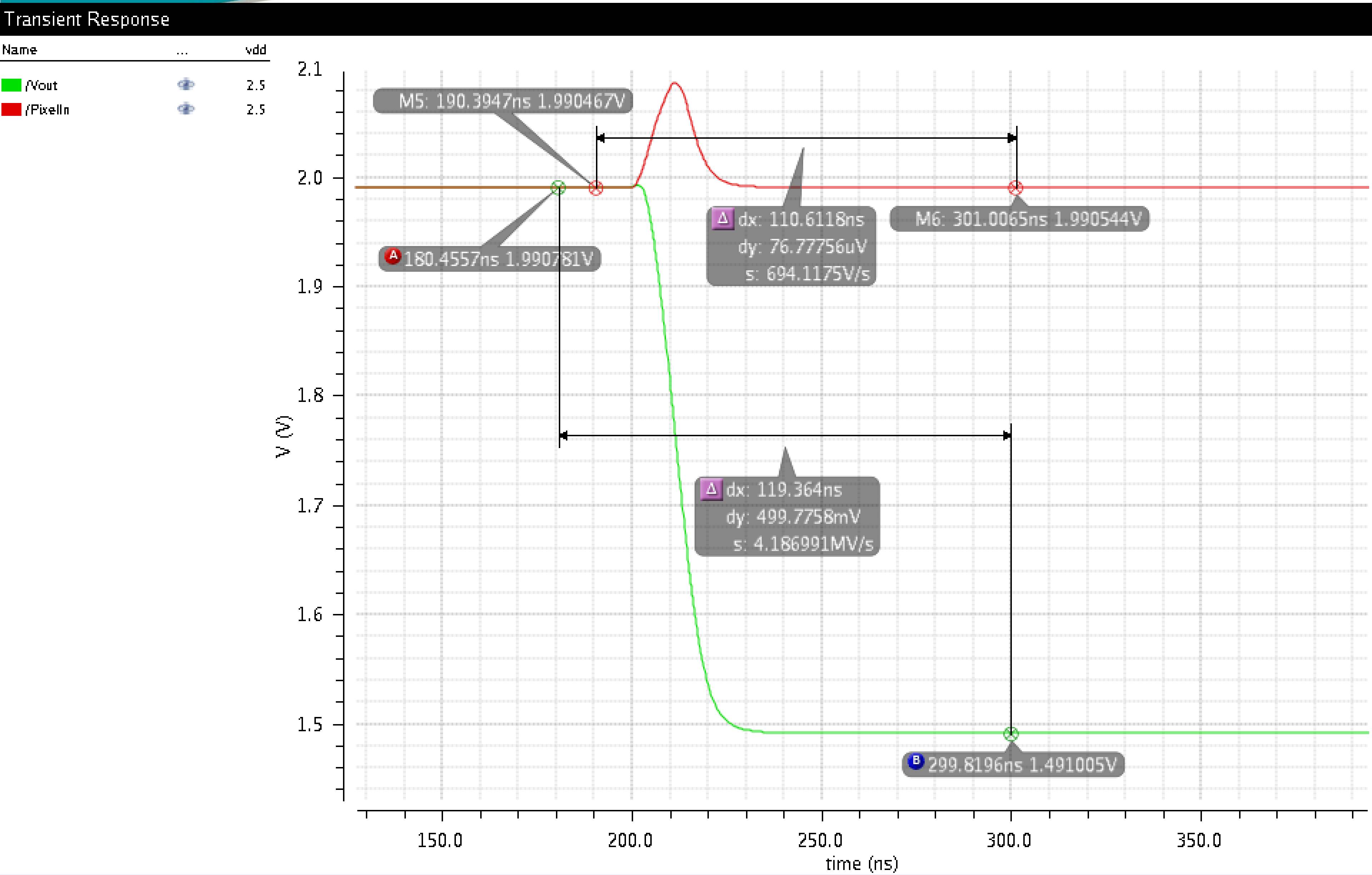


- Folded cascade structure
- Additional rapid recovery circuit added for V2
- High Open Loop Gain

Learning points:

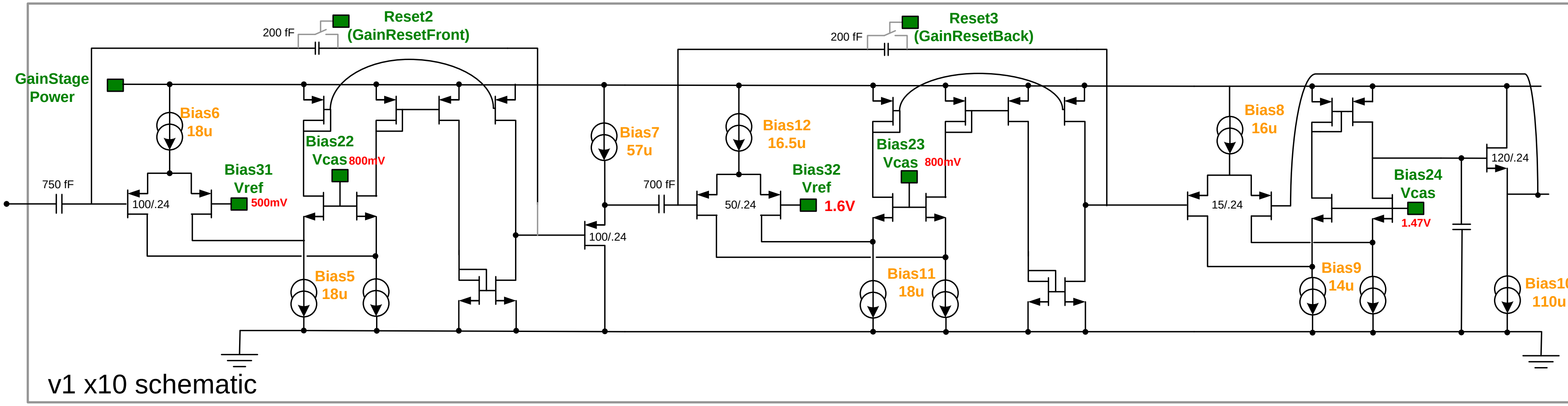
- Issue with recovery circuit with interposer channels that leak to gnd
- Switching noise from resets seem higher than expected

Preamplifier Transient Response



Gain Stages

- 1x , 10x ,100x



- Differential gain stages added more noise than we expected
- This led to a change to single ended designs for V2

Learning points:
- This method uses a large area of silicon and power
- Also the multiple stages complicated system timing

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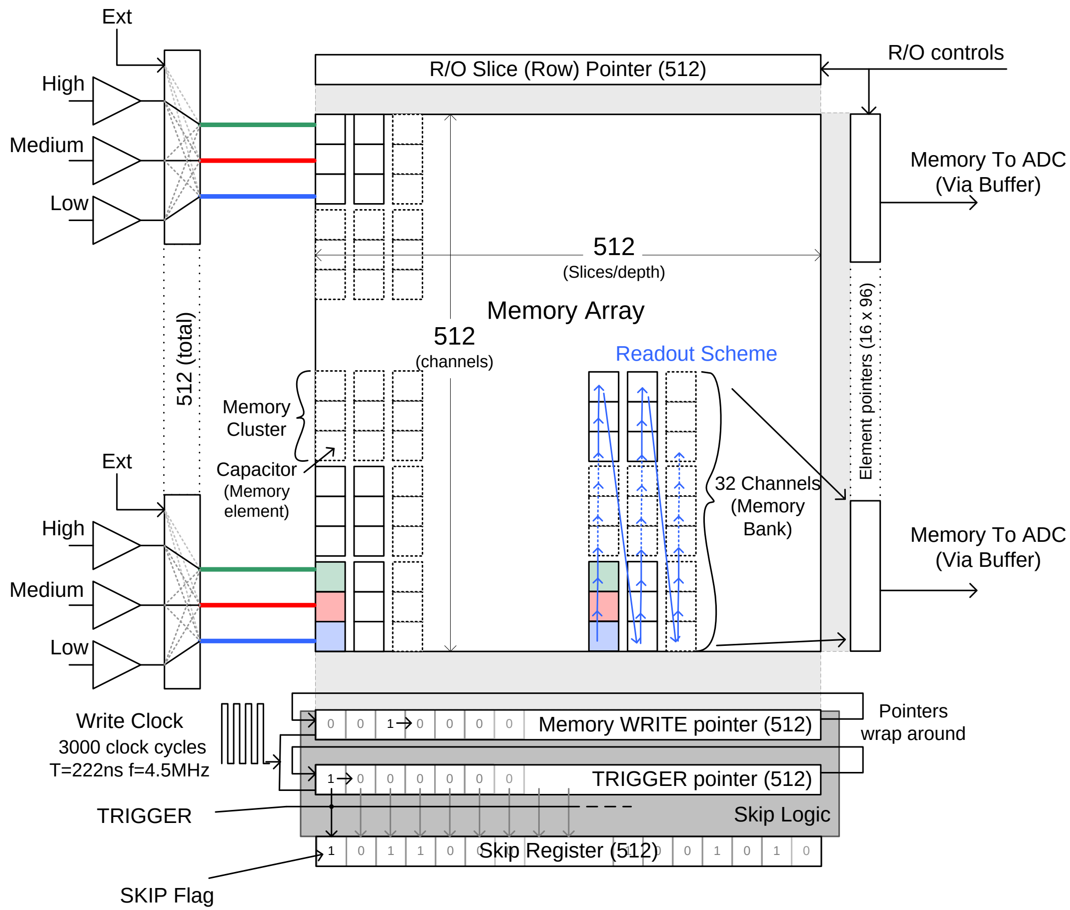
Memory

- Pipeline logic
- Reused that from APV25 design in CMS
- Enables flexible veto latency

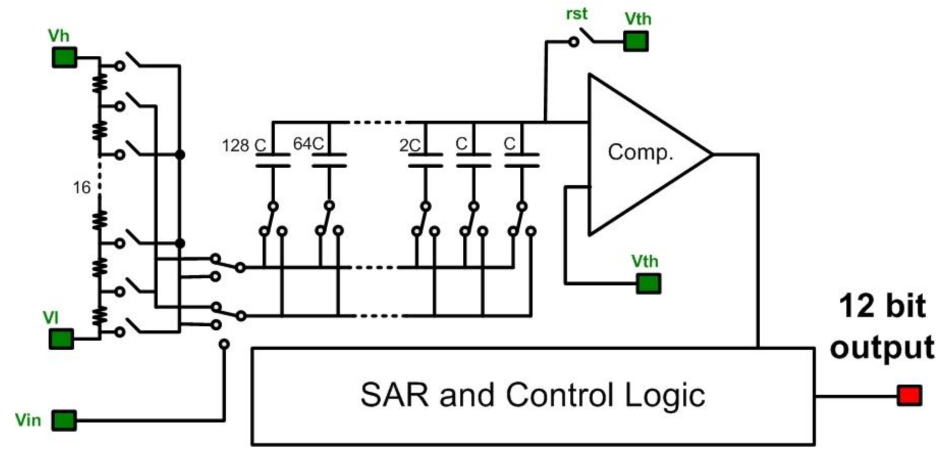


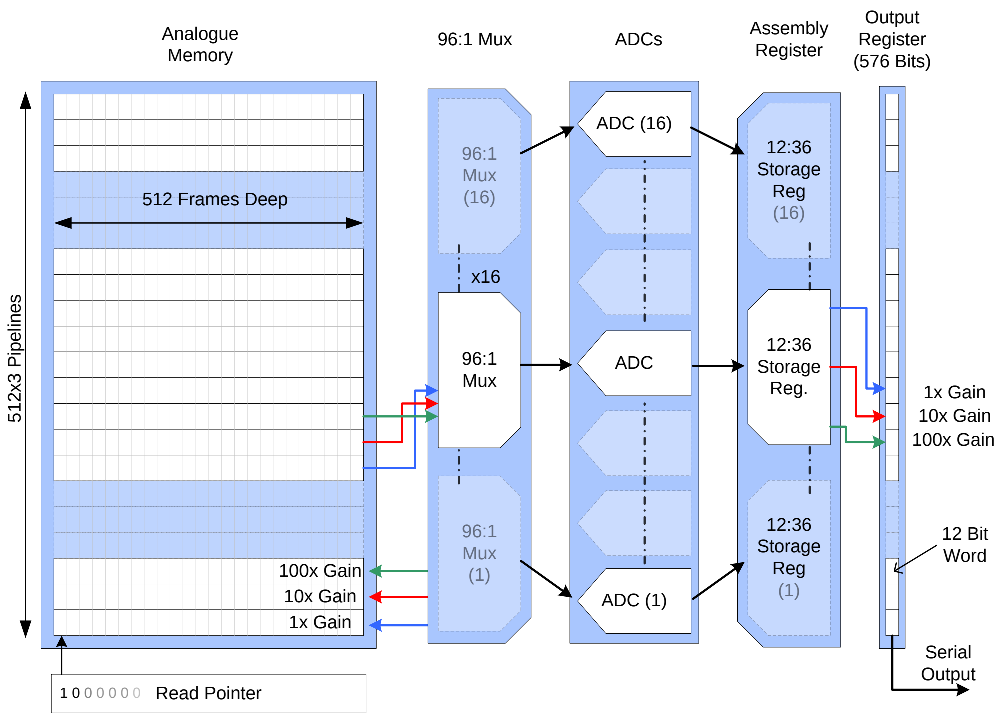
Learning points:

- Had issue with capacitor leakage post radiation
- Multiple voltage domains gave headaches to designers
- Complexity meant this was costly in design time requiring mixed signal verification

ADCs

- Sub-ranging successive approximation 12bit ADC
- Simplifies interfaces



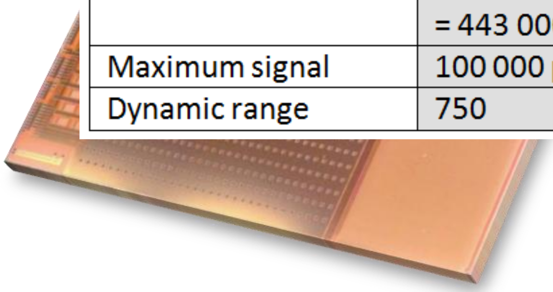


Learning points:

- Had timing problem in V1 that limited testing with ASIC
- Additional power in ASIC added to FE heat load, not insignificant
- Added complexity to ASIC test and production verification

Performance Specifications

	Standard Mode		High Gain Mode	
	V1 asic (50 pF)	V2 asic (50 pF)	A1 Asic (10pF)	V2 asic (5pF)
Gain x100				
Gain achieved	56	100 (note 1)	56	100
Noise rms	7.7 ph rms (12 keV) = 25700 el.	1.9 ph rms (12 keV) = 6 300 el.	1.9 ph rms (12 keV) = 6 300 el.	0.3 ph rms (12 keV) = 1000 el.
Maximum signal	1 000 ph	1 000 ph	200 ph	100 ph
Dynamic range	130	525	105	330
Gain x10				
Gain achieved	7.0	10	7.0	10
Noise rms	30 ph rms (12 keV) = 100 000 el.	20 ph rms (note 2) (12 keV) = 66 700 el.	6.9 ph rms (12 keV) =23 000 el.	4 ph rms (12 keV) = 13 300 el.
Maximum signal	10 000 ph	10 000 ph	2 000 ph	1 000 ph
Dynamic range	330	500	290	250
Gain x1				
Gain achieved	0.51	1	0.51	1
Noise rms	133 ph rms (12 keV) = 443 000 el.	60 ph rms (12 keV) = 200 000 el.	53 ph rms (12 keV) = 175 000 el	6 ph rms (12 keV) = 20 000 el.
Maximum signal	100 000 ph	100 000 ph	20 000 ph	10 000 ph
Dynamic range	750	1670	377	1670



x1 stage was now ADC noise limited
x100 noise is higher than this related to power issues

Control

- Command Interface via fast LVDS input (100MHz)
- Slow Control Registers programmed once at start up (~3.9 K bits)

Learning points:

- This system proved inflexible and does not allow fine optimisation of timing
- It does make you think through the whole system operation early on

1	0x00	NOP	no operation
2	0x01	STAND_BY	low power mode
3	0x02	POWER_UP	normal power
4	0x03	ON_CHIP_RESET_DISABLE	switch to manual rst
5	0x04	ON_CHIP_RESET_ENABLE	switch to auto rst
6	0x05	RESET_PRE_AMP	manual rst 1
7	0x06	RESET_GAIN_FRONT	manual rst 2
8	0x07	RESET_GAIN_BACK	manual rst 3
9	0x09	TEST_MODE_D	pseudo random no.
10	0x0A	TUNE_MODE	1s and 0s
11	0x0B	CLEAR_SKIP_REGISTER	rst skip reg
12	0x0C	RESET_WRITE_POINTER	rst write pointer
13	0x0D	RESET_TRIGGER_POINTER	rst trigger pointer
14	0x0E	START_WRITE_POINTER	start pointer
15	0x0F	START_TRIGGER_POINTER	start pointer
16	0x10	TRIGGER_FLAG_SET	puts flag in skip reg
17	0x11	READ_OUT_DATA	start memory read
18	0x12	REMOVE_RESET_PRE_AMP	manual rst 1 off
19	0x13	REMOVE_RESET_GAIN_STAGE1	manual rst 2 off
20	0x14	REMOVE_RESET_GAIN_STAGE2	manual rst 3 off
21	0x15	CLOCK_DIV_SEL	change clock div
22	0x16	SELF_TEST_EN	calibrate En
23	0x17	STOP_READ_OUT	end readout cycle
24	0x18	RESET_STATE_MACHINE	return to IDLE state
25	0x5A5A5	SYNC_RESET	sync commands

What design changes were considered for V2 ASIC?

Thin oxide option:

When building V2 we considered switching to thin devices:

Advantages of thin-oxide transistors for the pixel area:

- significant enhancement in radiation hardness;
- improvement in noise performance and/or lower power
- reduction of gate area

Disadvantages considered were:

- complete redesign and layout needed for all of the amplifiers in the pixel, delaying the LPD2 submission time by many months
- a reduction in dynamic range, possibly by a factor of 2, for Cf=50pF (changing to Cf=100pF would add new complications to the design)
- the limited amplifier output voltage range would increase input-referred memory and ADC noise contributions
- increased risk from gate oxide breakdown, particularly with large charge transients from the detector

Thin oxide option

In the end the change to thin-oxide transistors was considered to be a high risk option.

Decision - Stayed with thick-oxide designs with its known limitations, however:

- The improved top-level layout ensured that matched pairs of transistors are subject to the same radiation dose (assuming uniform exposure). Mismatch in dose was the main radiation effect seen in LPD1 testing.
- The thick-oxide designs are well understood and characterised, both in simulations and test results. We deliberately avoided major changes in circuits designs and architectures for LPD2, in order to minimise risk factors.
- The detector and interposer will provide significant shielding at 12keV, but there could be radiation effects for long exposures particularly at higher energies or with non-uniform images.

Did change Gain stage architecture

The differential amplifier was chosen for V1 because:

- good rejection of power supply noise
- stable operating point over a range temperature and supply voltage

However:

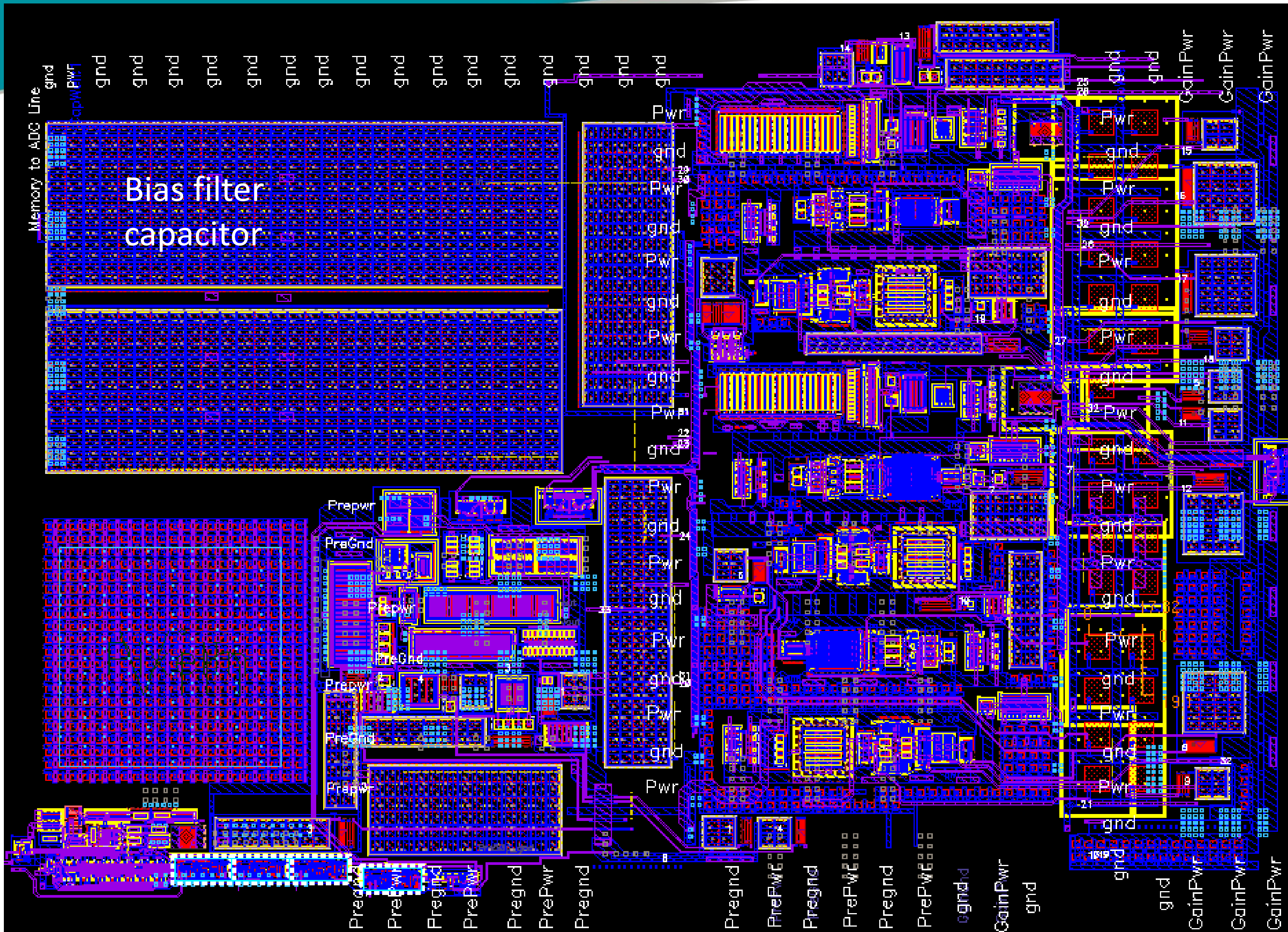
- noise contributions from double the number of transistors (input and biasing)
- double the power (for a given input transistor gm)

At review the amplifiers were all changed to single-ended format

- Gives the best transistor noise performance, for a given power supply current
- Test results from v1 showed that single-ended stages (100x front-end) did not suffered from power supply noise injection.

This change also gave more flexibility for bias settings.

Pixel layout 1



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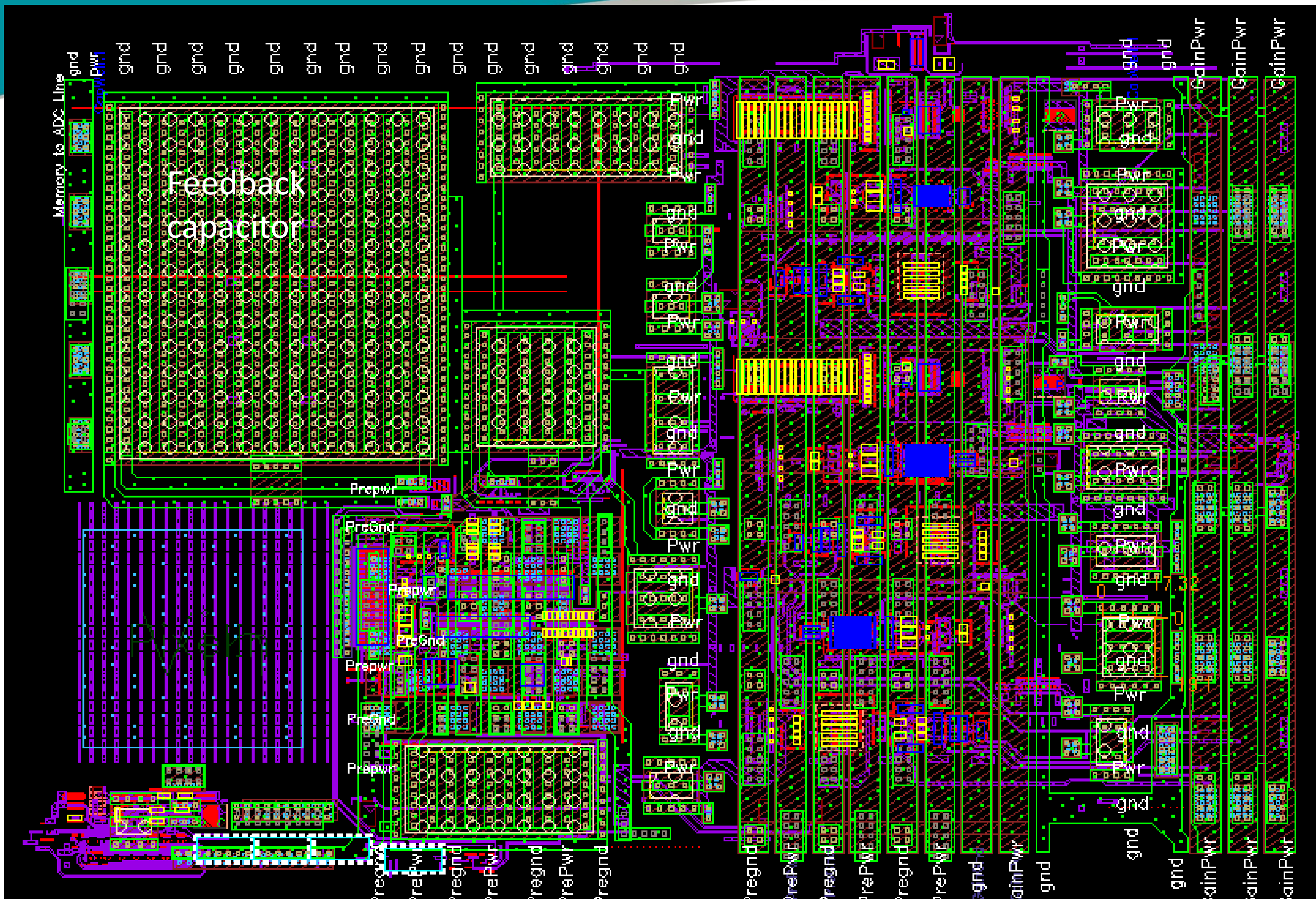
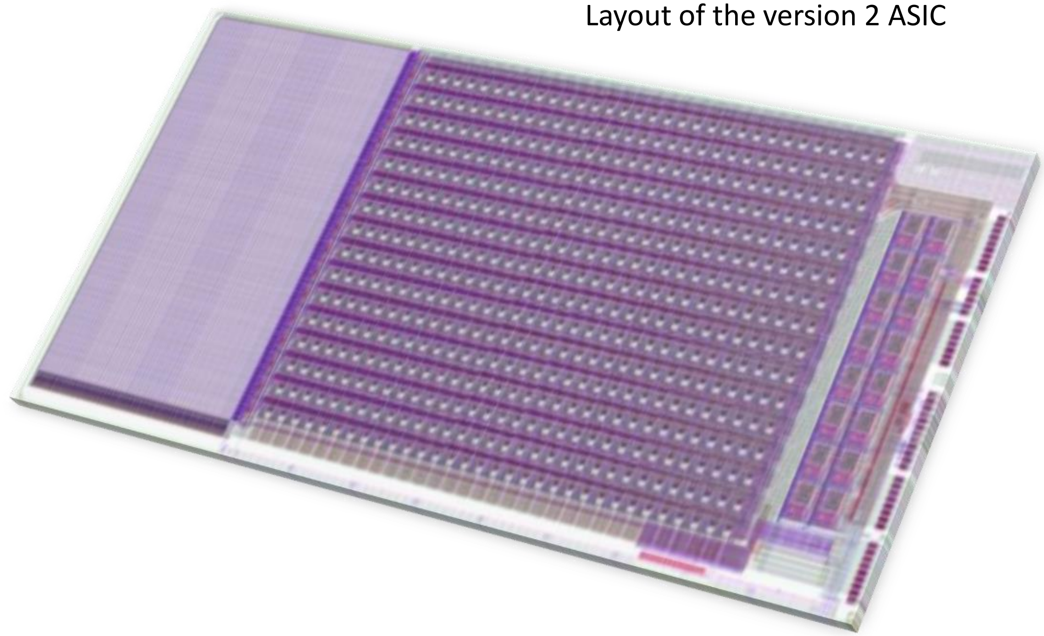
Pixel layout 2



ASIC V2 Summary

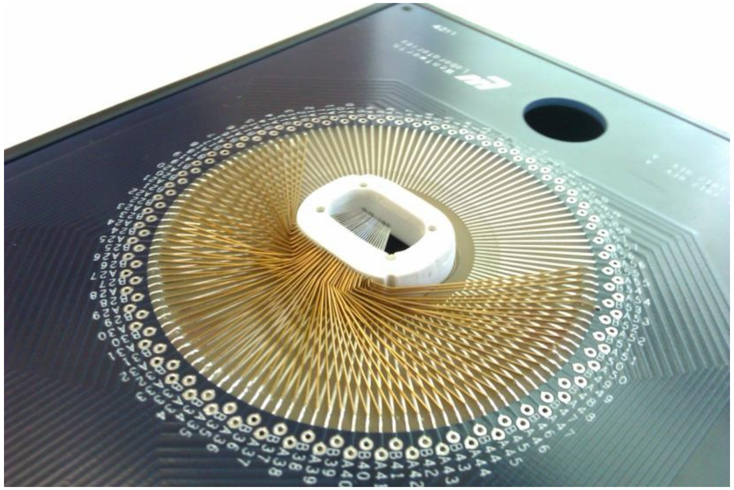
Layout of the version 2 ASIC



- Version 2 ASIC
  - **Improvements in power distribution**
  - **Noise is reduced** by a factor of 4 in 100X gain stage.
  - **High gain mode is now a 10x** increase of front end gain (50pF to 5pF change in feedback)
  - **Layout changes enabled memory and ADC radiation shielding**.

Gain Stage	Version 1 ASIC		Version 2 ASIC (Simulated Values)	
	Normal Mode	High Gain Mode	Normal Mode	High Gain Mode
	Noise (12keV ph, rms)	Noise (12keV ph, rms)	Noise (12keV ph, rms)	Noise (12keV ph, rms)
100x	7.7	1.9	1.9	0.3
10x	29.7	6.9	20	4
1x	133	53	60	6

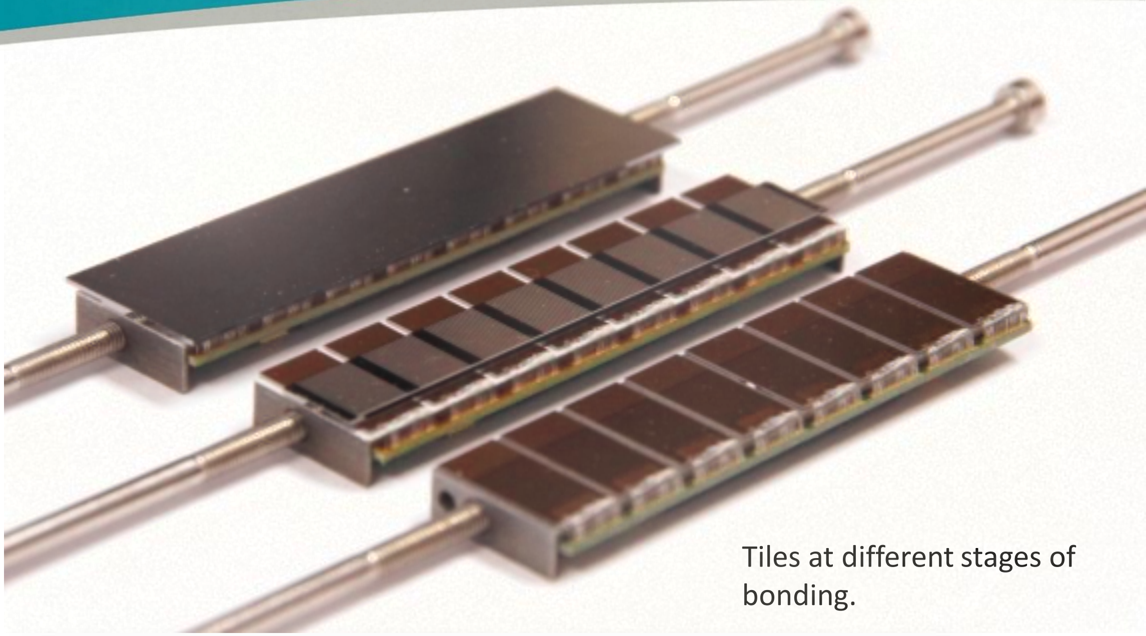
ASIC V2 Testing



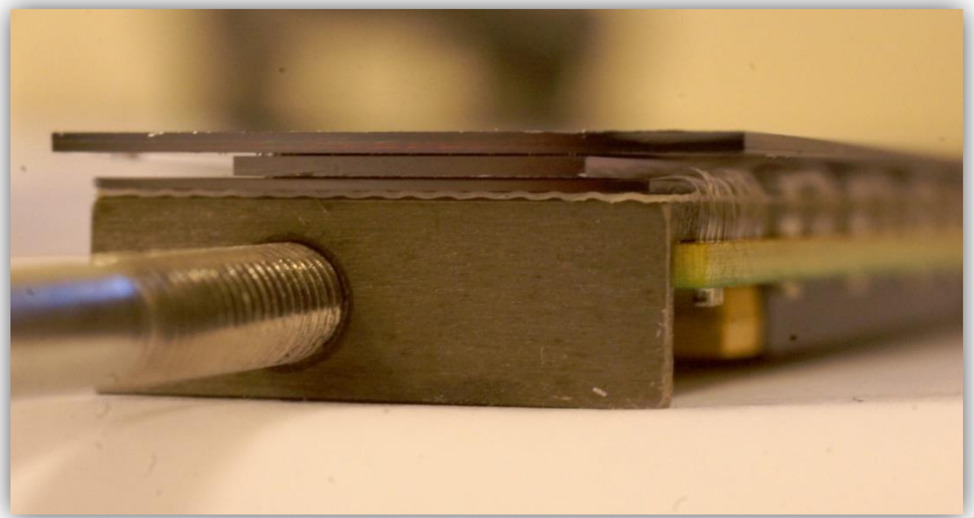
- Wafer Probing
  - ASICs must be probed to ensure quality detector tiles
    - Dead ASICs
    - Dead ADCs
    - Bad pixels or memory elements.
  - Probe card manufactured and tested on a loose version 1 ASIC. (86 way)

Interconnect/System Build

- Detector Tile Stack
  - Detector
  - Interposer
  - 8 x ASIC
- Gold stud to Silver loaded epoxy bonding
- Concealed ASIC I/O wire bonding
- 4 Side buttable
- Radiation hardness improved with Tungsten inserts.



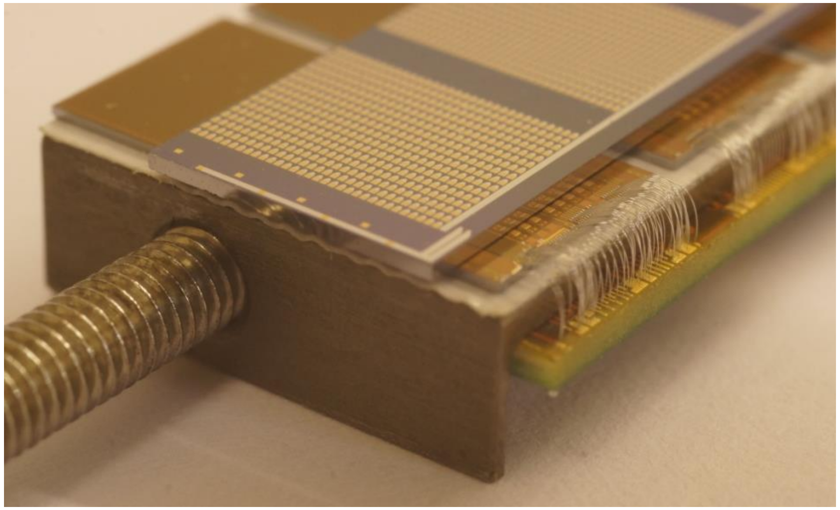
Tiles at different stages of bonding.

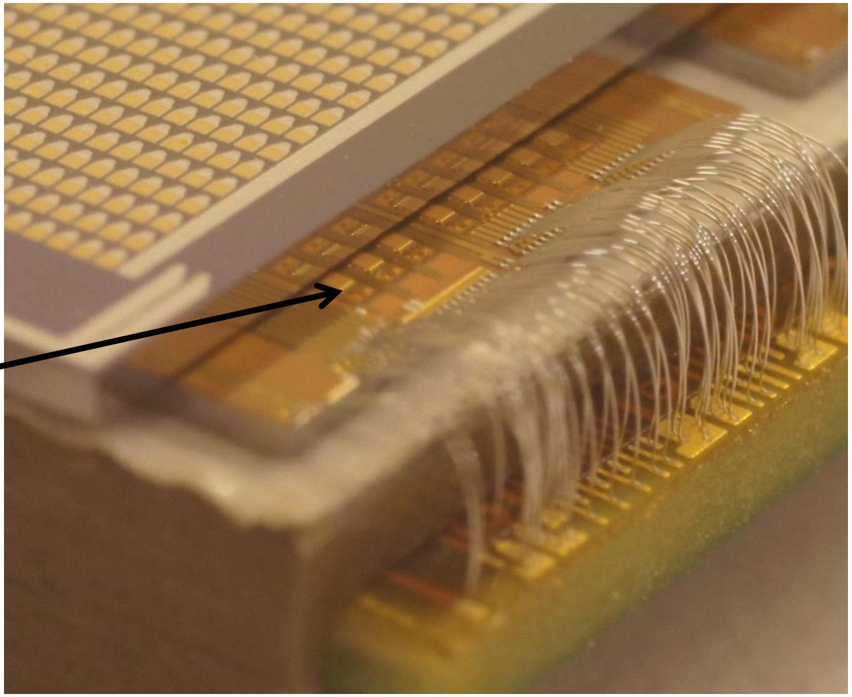


Side view of the detector tile

Interconnect/System Build

- Radiation hardness issues caused by difference in dose across shielded regions of the ASIC
- Solution was to move common circuits into regions of matched shielding.

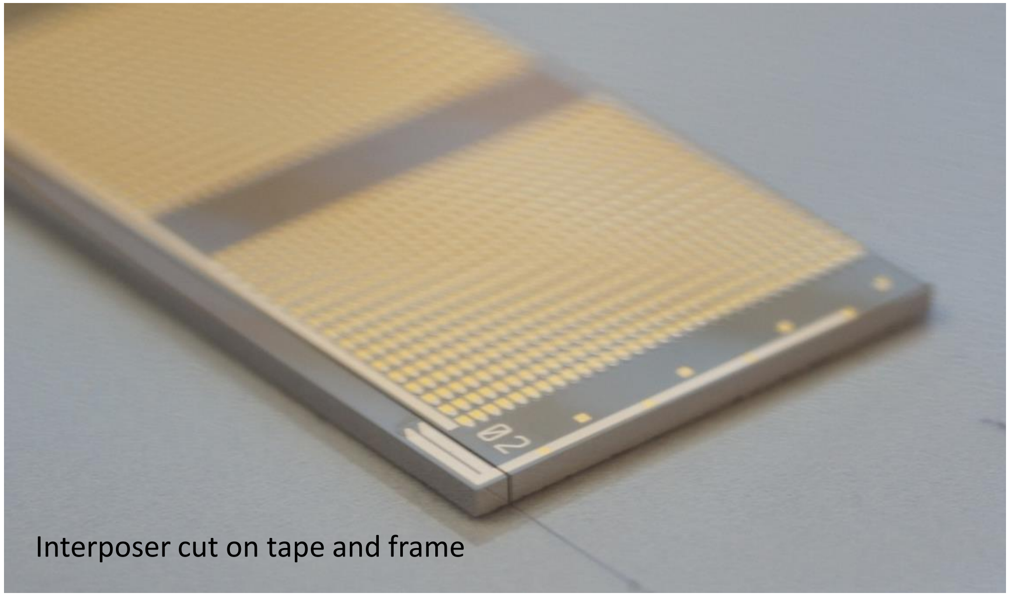




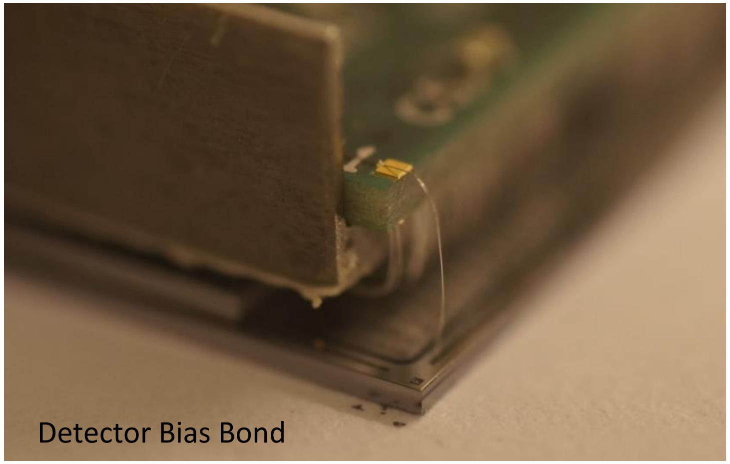
There are 2 rows of ADCs, here we can see half of the first row. The interposer straddles these circuits.

Interconnect/System Build

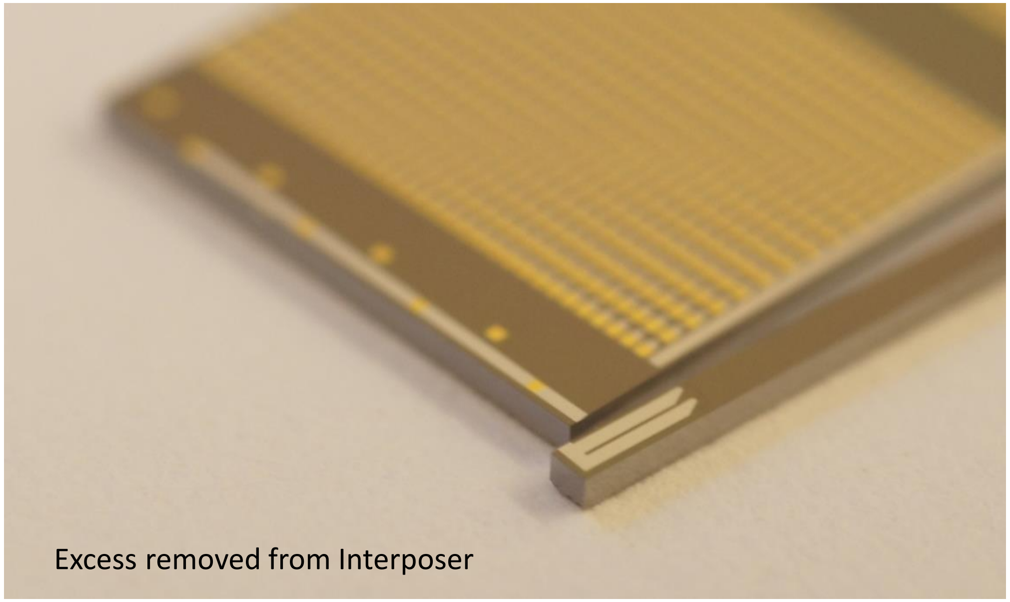
- Trimmed the interposers to enable shielded layout for ADCs



Interposer cut on tape and frame

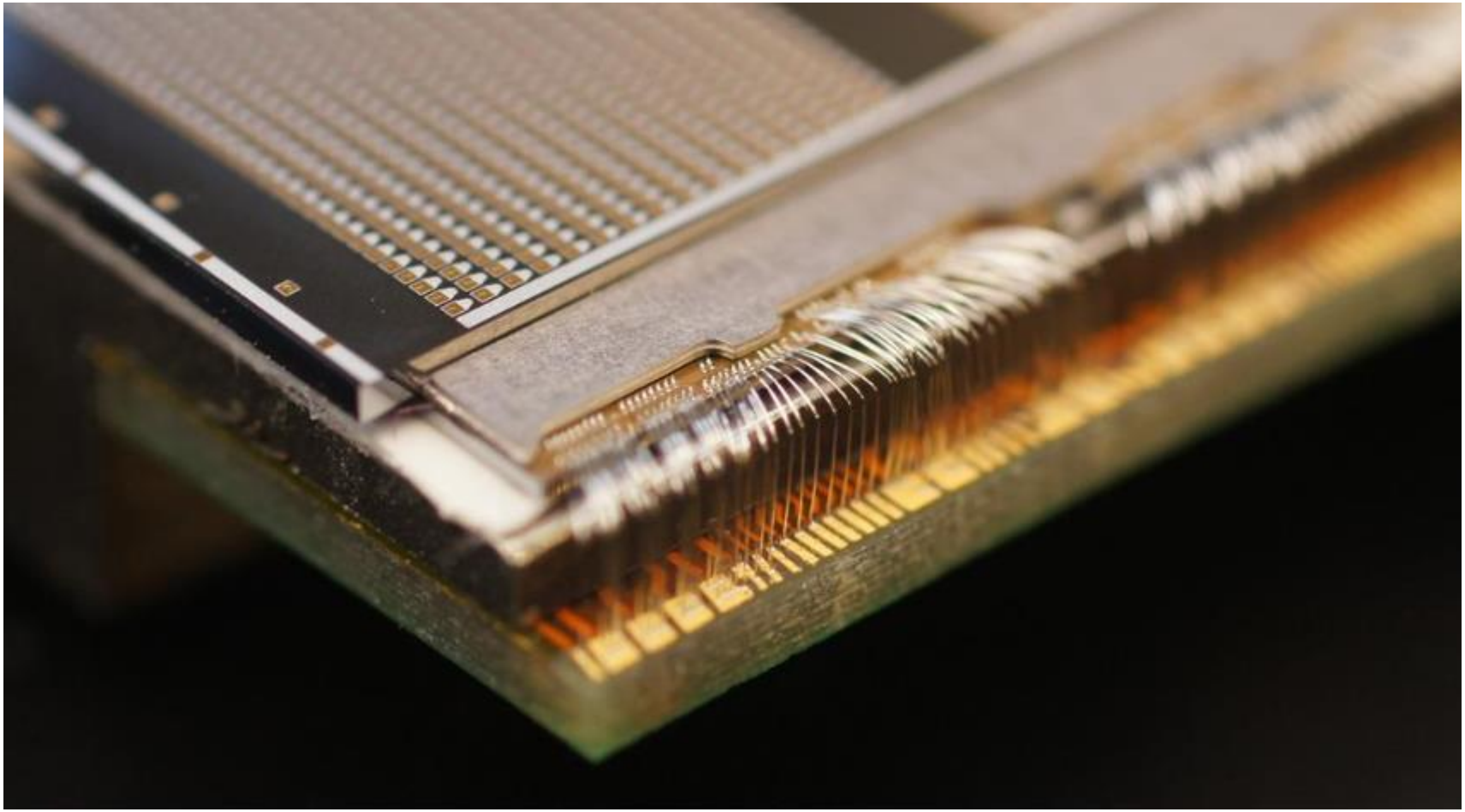


Detector Bias Bond



Excess removed from Interposer

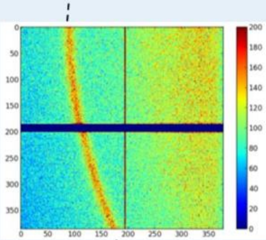
Tungsten shield in place

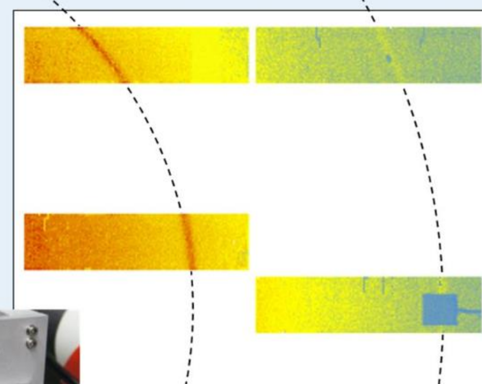


Numerous tests including May 2013 at SLAC

- Testing with real FEL
- Real test with simultaneous photons
  - Also tests full DAQ chain
  - Software integration with beamline

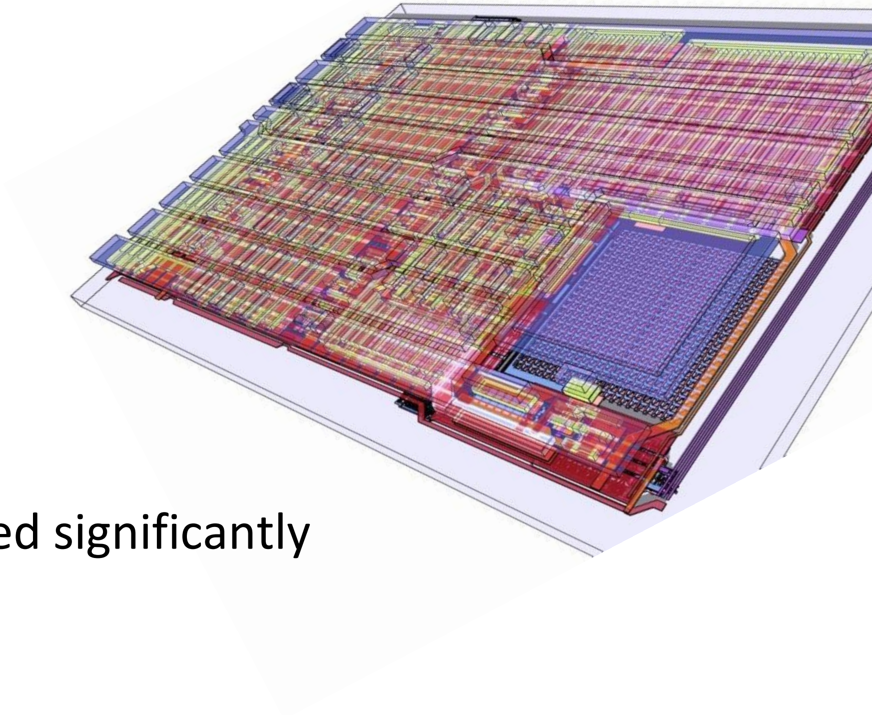
Imaging TiO2 diffraction rings with CSPAD (Left) and LPD (right) simultaneously for calibration
Here the LPD system is part populated with 4/16 tiles





Chip Overview

The various updates and changes to the design all worked as expected:



1) The timing bug for ADCs corrected the readout issue with V1

2) Power distribution in the ASIC improved significantly

3) Noise performance improved

We are now in the process of completing the rest of the system build and manufacture.

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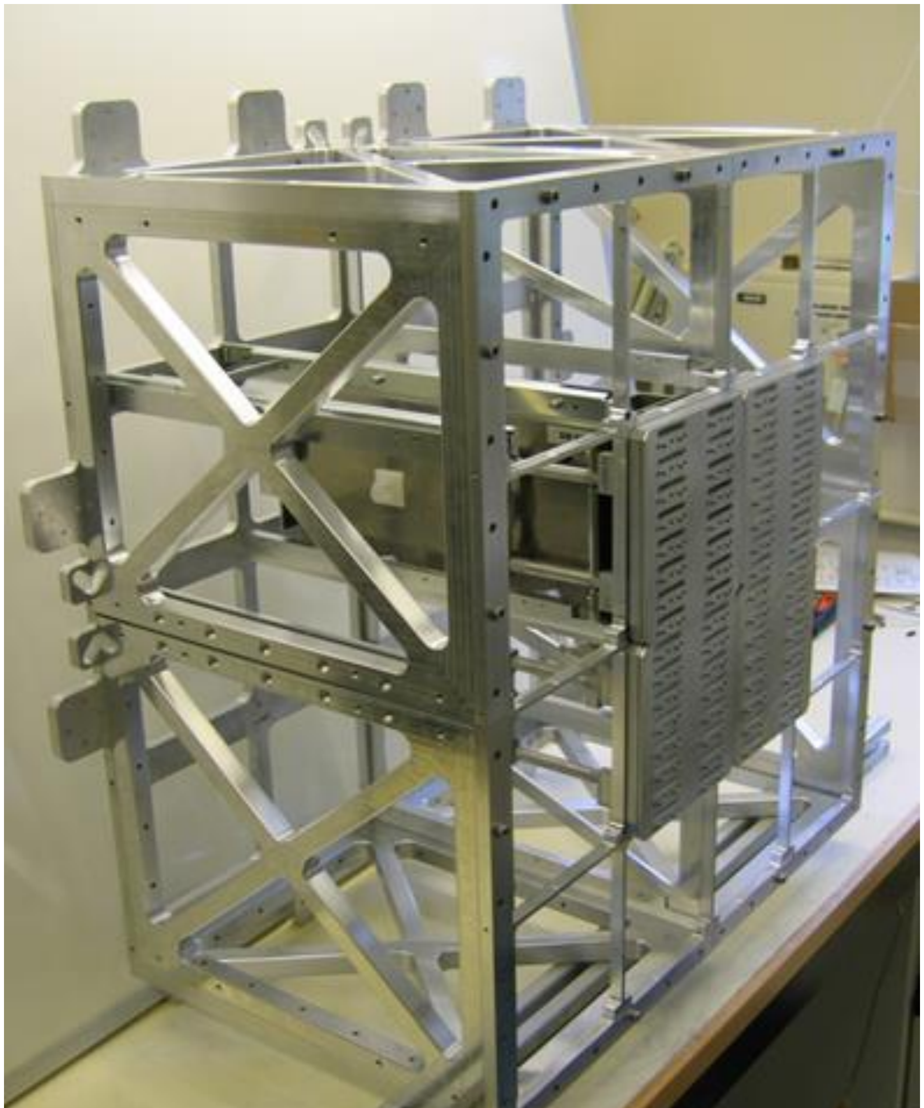
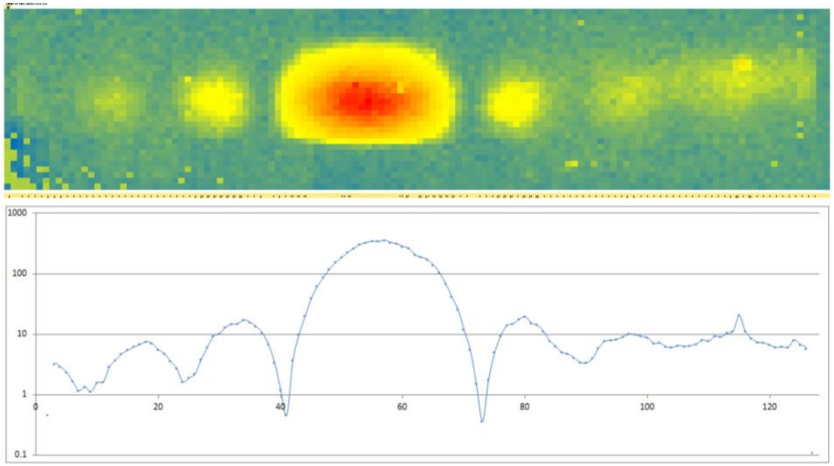
  - Lessons learnt in the programme
- **Where we are now**
- **Looking ahead:**
  - Upgrade options for the future

Manufacturing systems

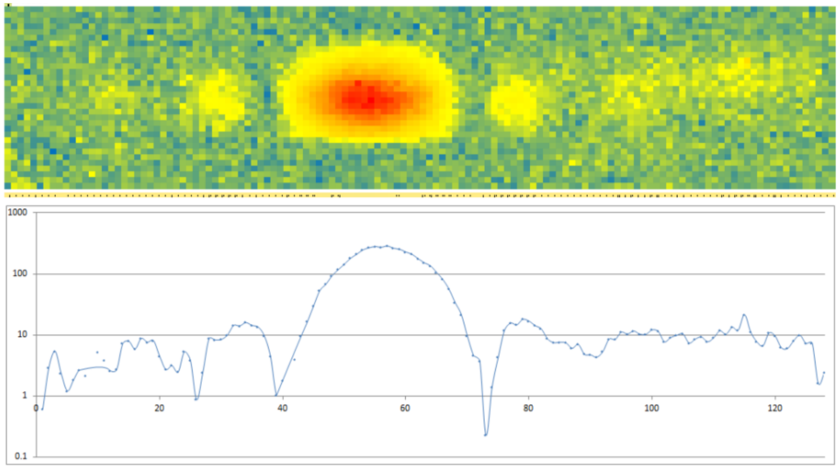


CLF Testing at RAL

Single Slit Diffraction - 5pF Mode



Single Slit Diffraction - 50pF Mode



Test now with a laser at home…

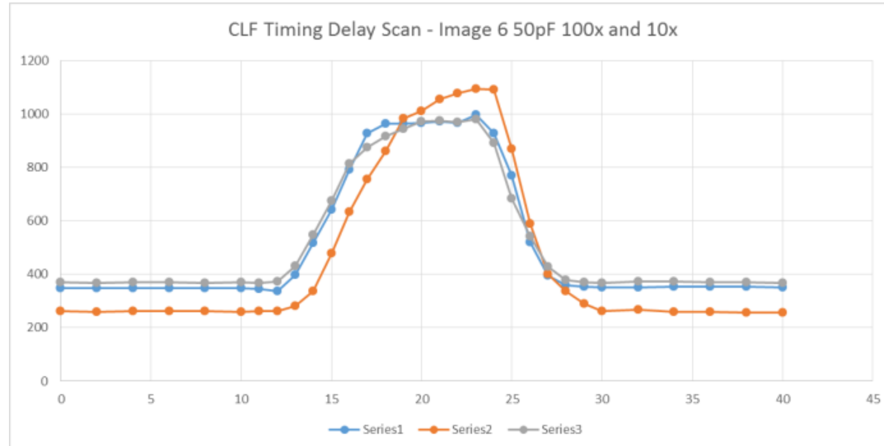
Testing with pulsed IR laser. This enables rapid progress towards qualification of high speed and high signal response

- Class 4 IR laser, run at low power and 100Hz rep rate
- Attenuation through Aluminium coating multiple orders of magnitude.
- Synchronised to 10nsec Similar to LCLS operation

CLF Timing Investigations

CLF Testing

- Enables tuning in timing resets and sample point



- Optimising sensor bias voltage for best charge collection time.

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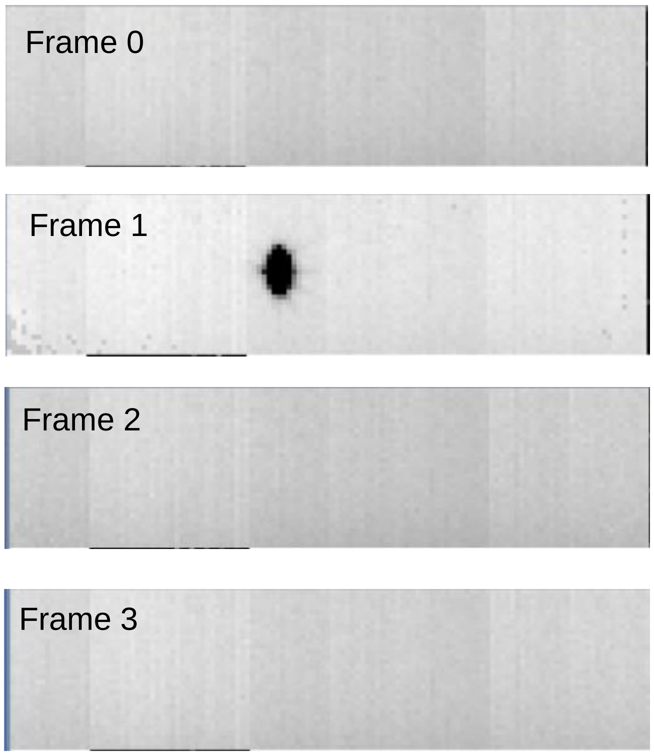
Recovery from saturation

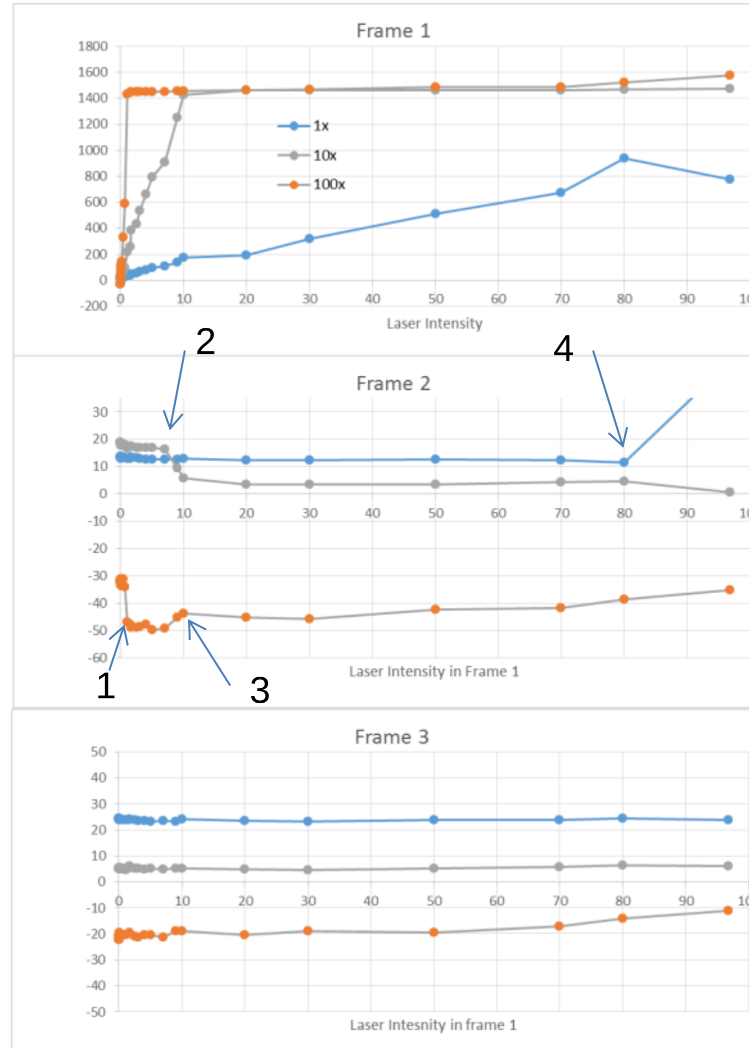
CLF Testing

Allows you to easily explore full dynamic range over large numbers of pixels

- Full dynamic range sweep
- Recovery from saturation improved over LCLS data, similar to noise levels.
- +/- 10 ADUs

Laser Intensity 98mV = 18uJ
50pF Data





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Summary of Lessons Learnt:

Key Things (personal view):

- Everything takes longer than expected
- With XFEL Schedule we would have benefitted from more test structures early on
- We did learn a lot from the large ASIC early in the project
- Mechanics, cooling and powering are large design items
- We spent a lot of time on numerous mechanics options
- We are still learning new things about our chip!
- …

Presentation Outline:

- **Intro to XFEL Requirements**
- **Motivation for the LPD approach**
- **Overview of chip development**
  - Test chip and production versions
  - Summary of architecture
  - Lessons learnt in the programme
- **Where we are now**
- **Looking ahead:**
  - Upgrade options for the future

How to Upgrade?

- Science Demands:
  - **Higher resolution**
  - **Don't want to sacrifice memory depth**
  - **Lower system noise and power**
  - **Increased radiation hardness**
- Approaches:
  - **Scale pixels smaller?**
  - **Go for 3D integration?**
- Other points:
  - **Long development times means we need to start now, ahead of XFEL operation**
  - **Significant expense and risk**

A new XFEL High Resolution Camera Concept

A high-Z Hybrid Camera System containing 2D CCD in-pixel Memory Storage for 5MHz Image Capture with Large Pixel Count at 60 micron pitch to address the challenge of scaling to much smaller pixels whilst retaining ~400 frame memory depth.

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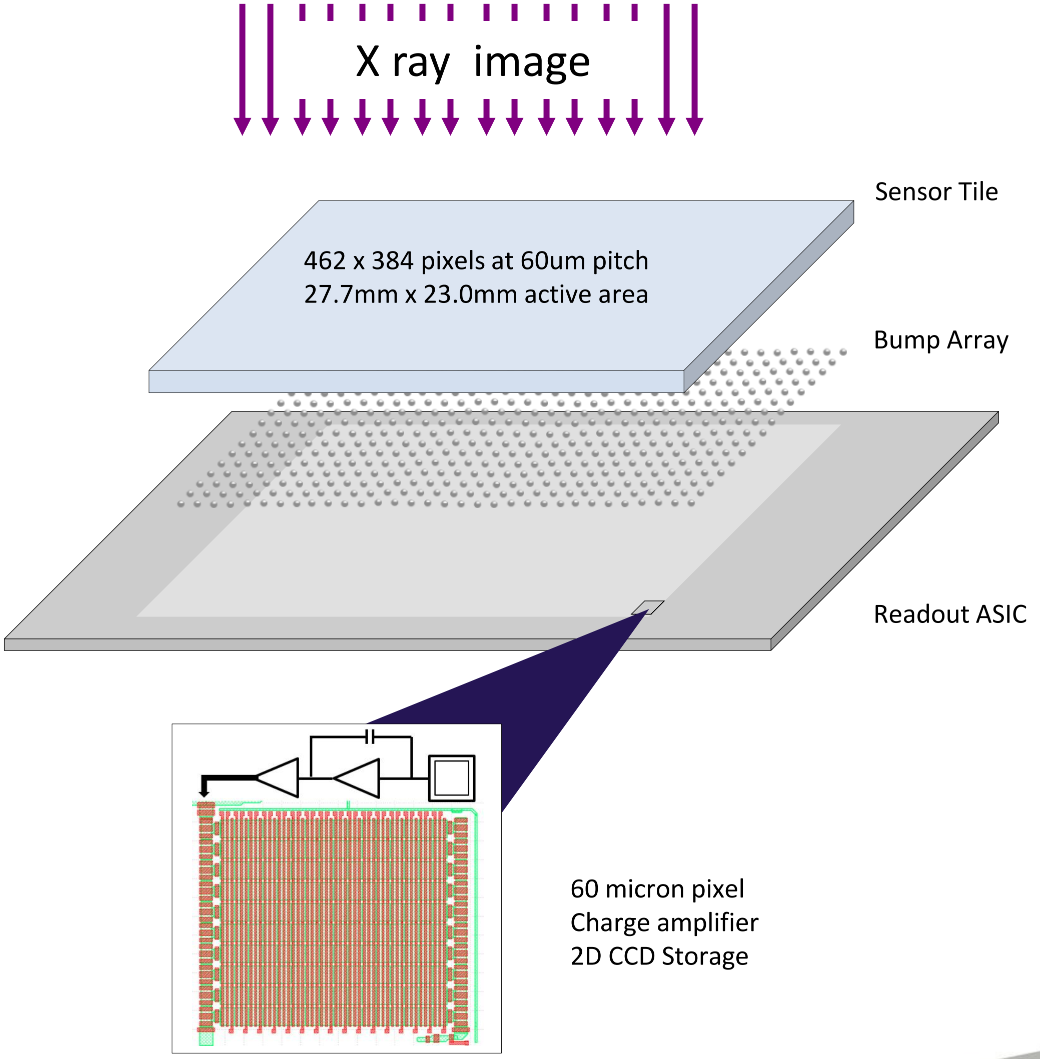
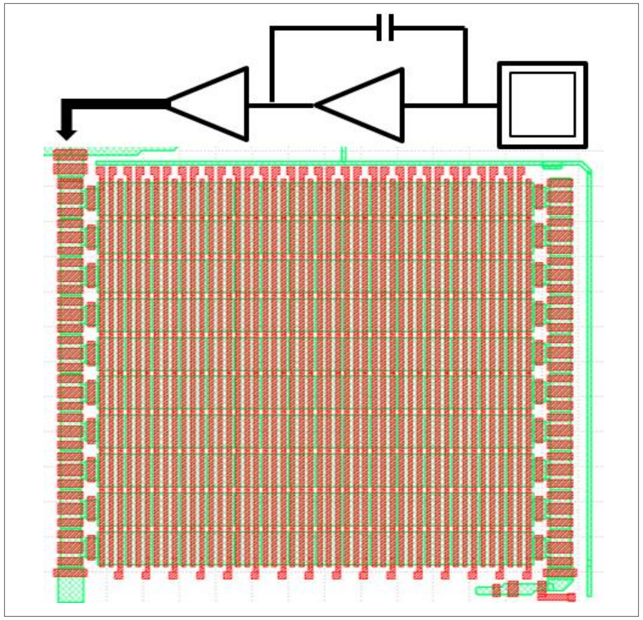
Rutherford Appleton Laboratory

Proposed Geometry:



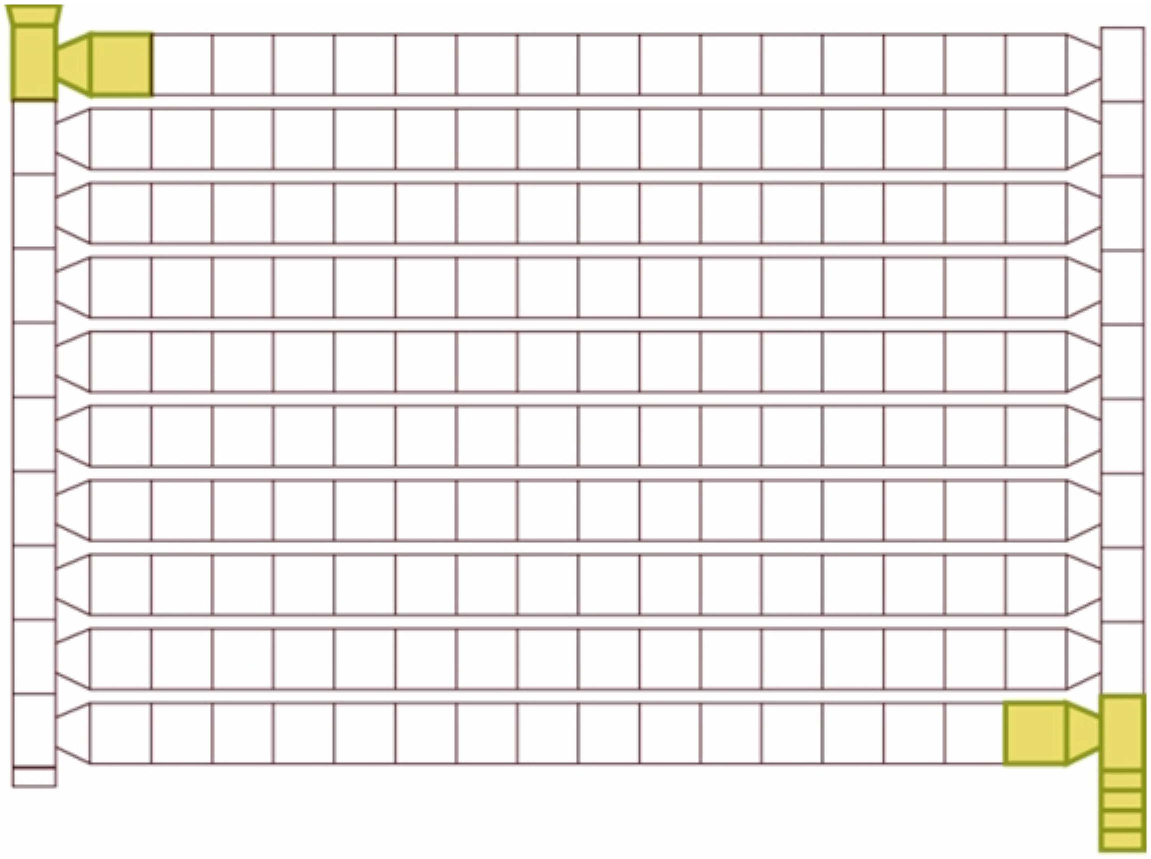
Proposed Pixel Architecture

- Bump-bond pad for Indium or solder assembly
- Dynamic range
  - 100 fF charge integrator
  - 220 photons at 12keV
- CCD Matrix
  - Could contain more memory than is readout (if readout skips through unwanted cells)
  - Various geometries possible depending on application requirements
  - Power saved between bunches as limited CCD clocking in that period

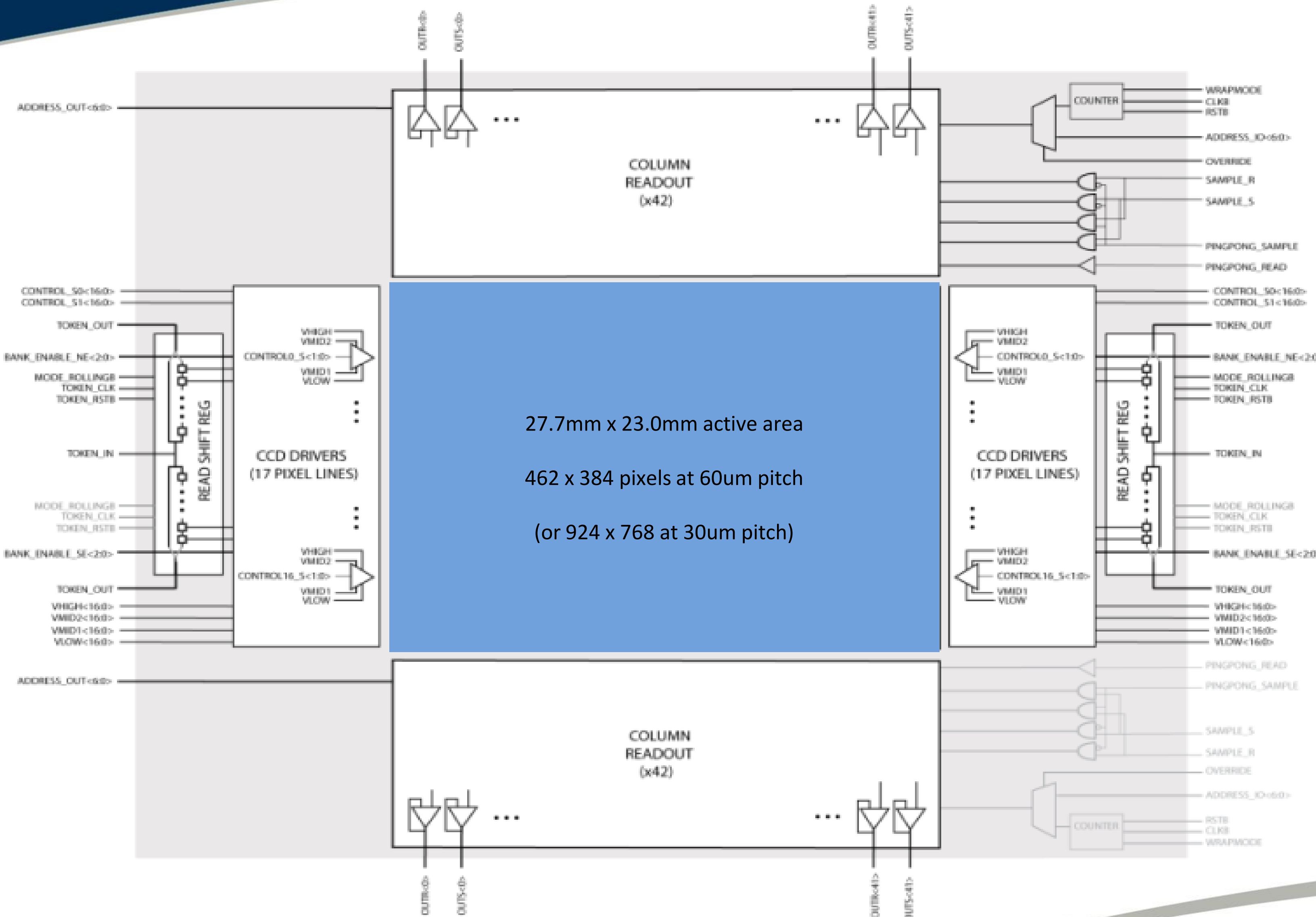


CCD Memory Shift Operation

- Use classic ‘Fill and Spill’ method for loading CCD from charge amp output
- Use input register for implementing veto latency
- 2D matrix then optimises transfer efficiency for long memory
- Complete CCD readout in the 100ms XFEL pulse gap



Readout ASIC Floorplan



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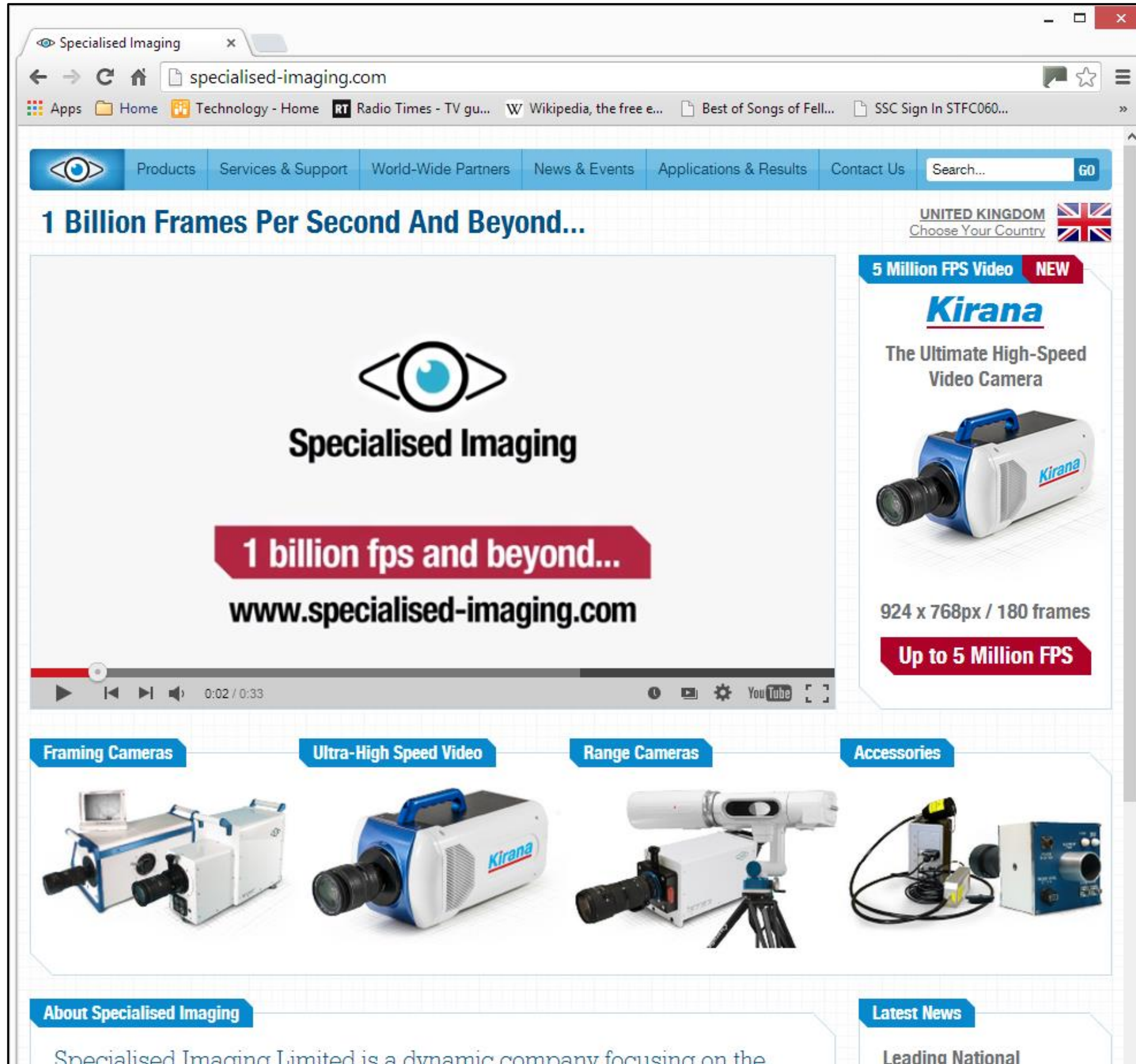
RAL Partnership with Specialised Imaging:

- STFC supplies all Kirana sensors for SI cameras
- CCD System in an advanced development on 180nm CMOS technology
- STFC working with TowerJazz^{TM} to further refine the CCD process for in pixel storage



TOWERJAZZ

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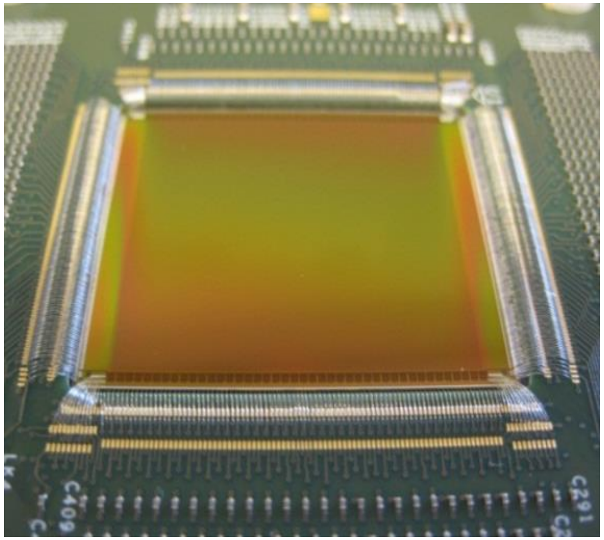
Specialised Imaging 'Kirana' camera product

- Today second generation 0.7Mpixel RAL sensor exists:
  - 30 µm pixel
  - Combined high and ultra-high speed operation
  - Burst mode at 5Mfps with 180 memory cells approx. 3.5 Tpixel/sec
  - Continuous mode at over 1kfps
  - 10 bit system dynamic range
  - Ethernet based DAQ system with full analogue chain available to buy
- What about radiation Hardness?

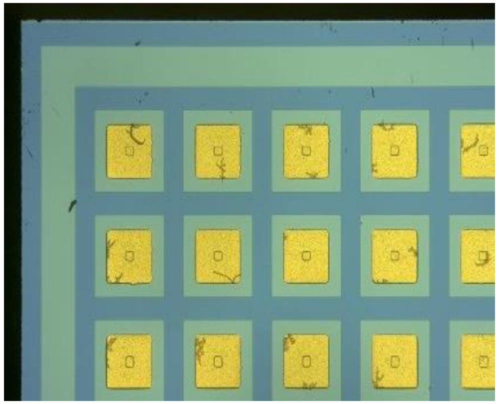


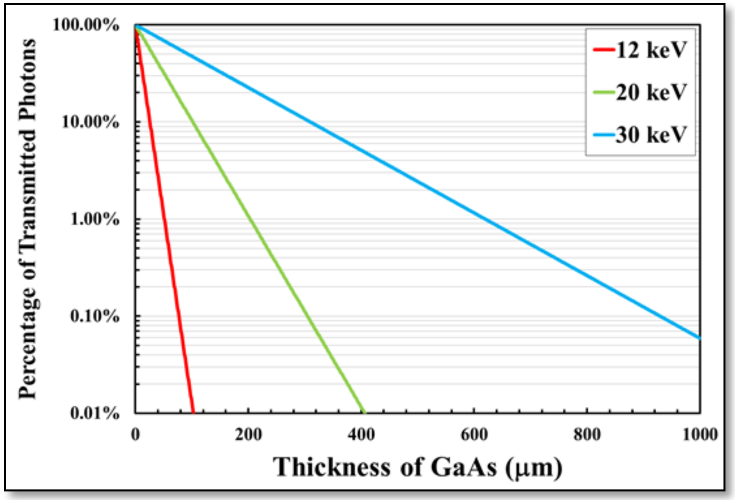
RAL Sensor on Kirana Headboard

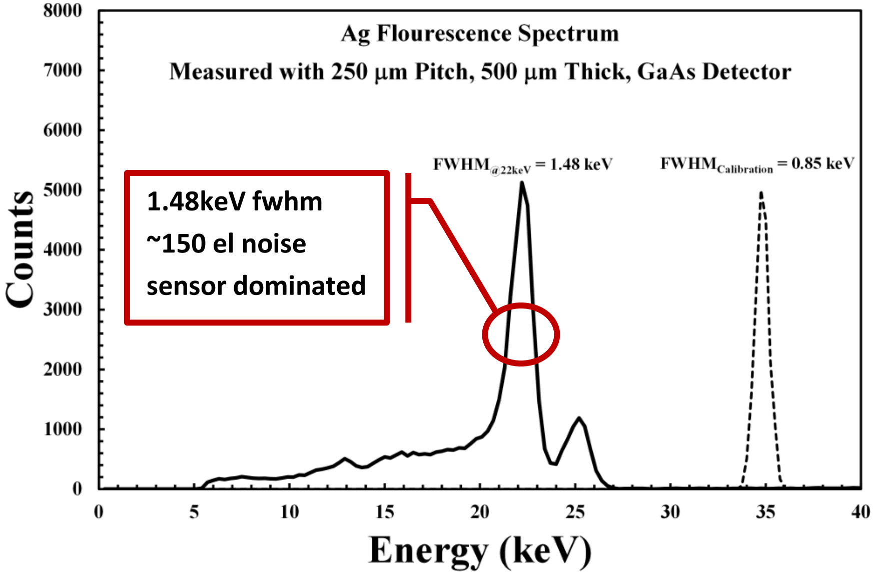
Specialised Imaging Kirana camera

Radiation Damage in CCD?

- CCD Transfer efficiency a key system performance driver
- GaAs material for sensor tile
  - High stopping power for 12keV reduces ASIC dose
  - Interesting recent results from Cr compensated material with RAL Hexitec





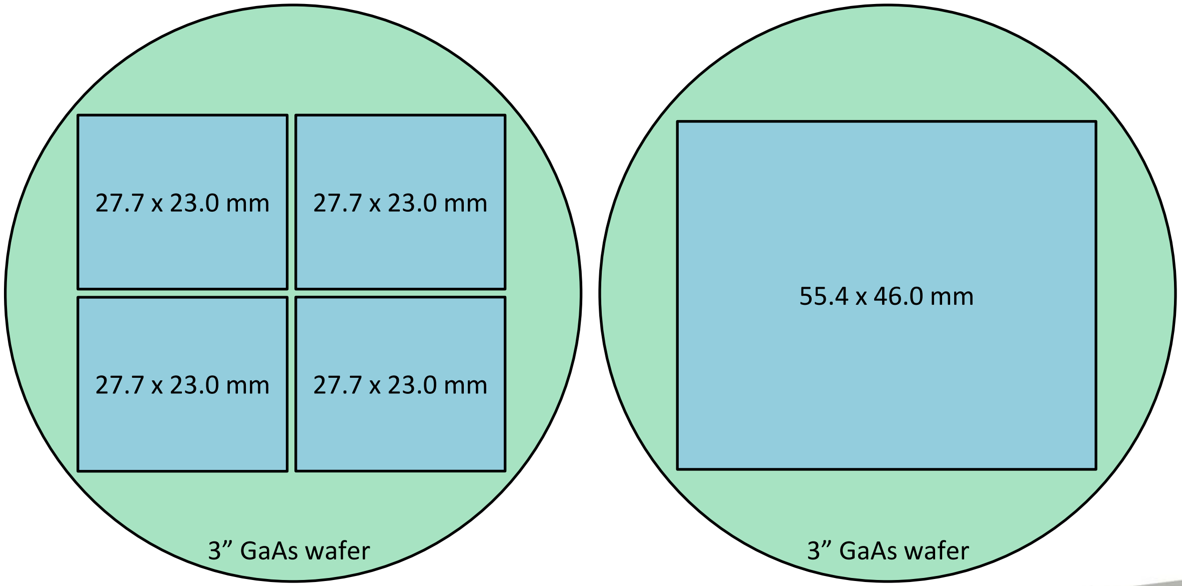


250 micron pitch Hexitec tests with Tomsk material

Possible geometries with stitched sensors?

- ASIC can stitch to 800mm wafer
- GaAs Sensors currently only available on 80mm wafers
- Possible to tile sensor surface with multiple sensors
- Limitation becomes a DAQ one with limits on data volumes to evacuate from sensor between trains

Pixel Pitch	Frame Depth	Pixel Count	X (mm)	Y (mm)
30	100	924 x 768	27.7	23.0
60	400	462 x 384	27.7	23.0
60	100	924 x 768	55.4	46.0



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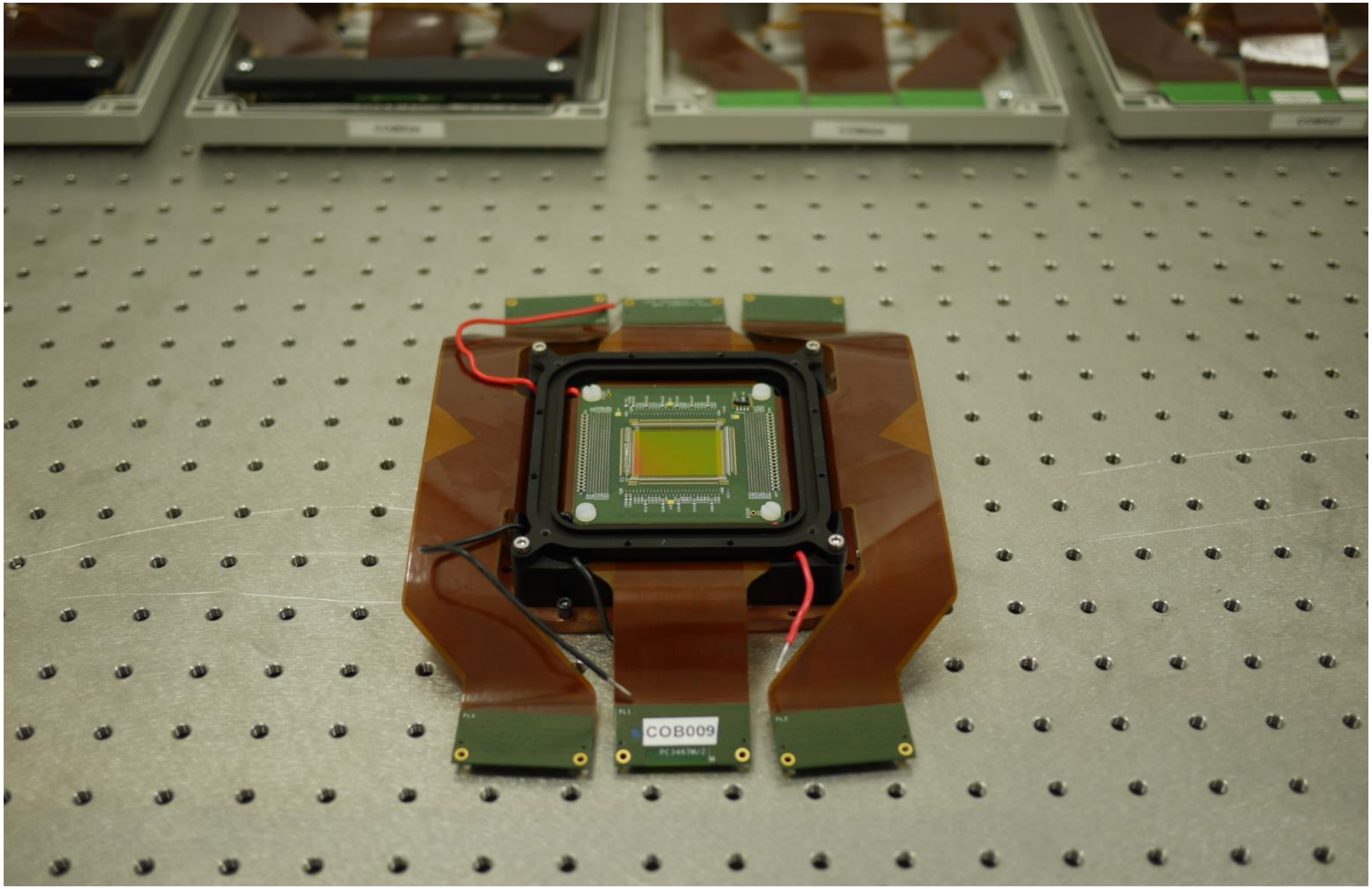
STFC RAL Kirana Sensor



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Summary

- Two versions of the LPD ASIC have been developed
- We are now in the production of the full Mpixel device
- Quadrant system shipped to XFEL for testing DAQ
- Work still to do with power supplies and software etc.
- Currently preparing for fine pitch proposals for system upgrades in the future

Thank you for your attention

Additional thanks to:

- The Hamburg XFEL Project Team
- LCLS, DLS and CLF for test access
- ASIC Designer team at RAL

Photon Calculations (12keV GaAs)

photons	eV	eV / electron	electrons	charge (fF)	C feedback (fF)	Vswing (V)
1	12000.00	4.20	2,857	0.46	100	0.005
20	12000.00	4.20	57,143	9.16	100	0.092
40	12000.00	4.20	114,286	18.31	100	0.183
60	12000.00	4.20	171,429	27.47	100	0.275
80	12000.00	4.20	228,571	36.62	100	0.366
100	12000.00	4.20	285,714	45.78	100	0.458
120	12000.00	4.20	342,857	54.93	100	0.549
140	12000.00	4.20	400,000	64.09	100	0.641
160	12000.00	4.20	457,143	73.24	100	0.732
180	12000.00	4.20	514,286	82.40	100	0.824
200	12000.00	4.20	571,429	91.55	100	0.916
220	12000.00	4.20	628,571	100.71	100	1.007