Quanta Image Sensor (QIS) - an oversampled visible light sensor

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Motivation for this work

- Pixel shrink yields smaller full-well capacity which impacts dynamic range and maximum SNR.
- Photons, or quanta, are digital in nature according to particle view of light and can be represented by binary data.
- Better images can be obtained by oversampling in time and space.

Quanta Image Sensor

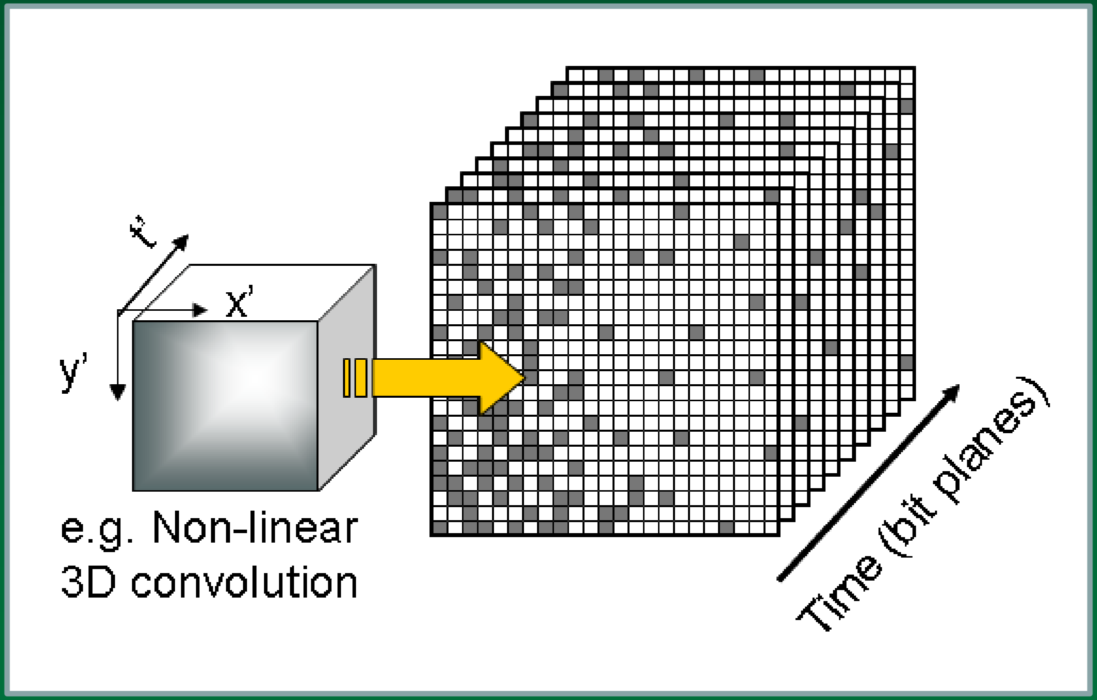
- Original goal for QIS was to make a very tiny, specialized pixel (“jot”) which could sense a single photoelectron.
- Jots would be readout by scanning at a high frame rate to avoid likelihood of multiple hits in the same jot and loss of accurate counting.
- Image pixels could be created by combining jot data over a local spatial and temporal region using image processing.
- The first proposed algorithm was the “digital film sensor” using a “grain” and “digital development” construct.

Quanta Image Sensor

□

▨

Jot = specialized sub-diffraction limit (SDL) pixel, sensitive to a single photoelectron with binary output, "0" for no photoelectron, "1" for at least one photoelectron.



Many jots are needed to create a single image pixel.

e.g. 16x16x16 = 4,096

A QIS might have 1G jots, read out at 1000 fields/sec or 1.0 Tbits/sec

Problems we have been working on

1. Photons to photoelectrons
    - Just starting – how does light get absorbed by small semiconductor jot structures
2. Photoelectrons to jot signal
    - Invent and evaluate candidate jot devices
    - TCAD modelling of those devices
3. Readout of jot signal to digital circuits
    - Low power, single-bit ADC-per-column
4. Getting massive amounts of data off-chip
    - Compression and compressive sensing?
5. Transforming jot data cube into image
    - Algorithms
6. Understanding imaging characteristics

Understanding QIS Imaging Characteristics

E.R. Fossum, Modeling the performance of single-bit and multi-bit quanta image sensors, IEEE J. Electron Devices Society, vol.1(9) pp. 166-174 September 2013.

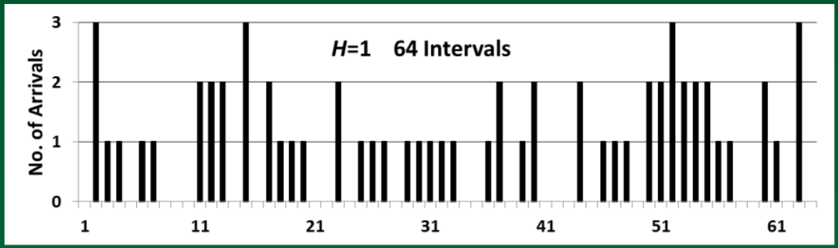
Photon and photoelectron arrival rate described by Poisson process

Define *quanta exposure H* = $\phi\,\tau$ *H* = 1 means expect 1 arrival on average.

Probability of k arrivals

$$P[k] = \frac{e^{-H}\,H^{k}}{k!}$$

Monte Carlo



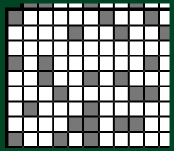
For jot, only two states of interest

□ $P[0] = e^{-H}$

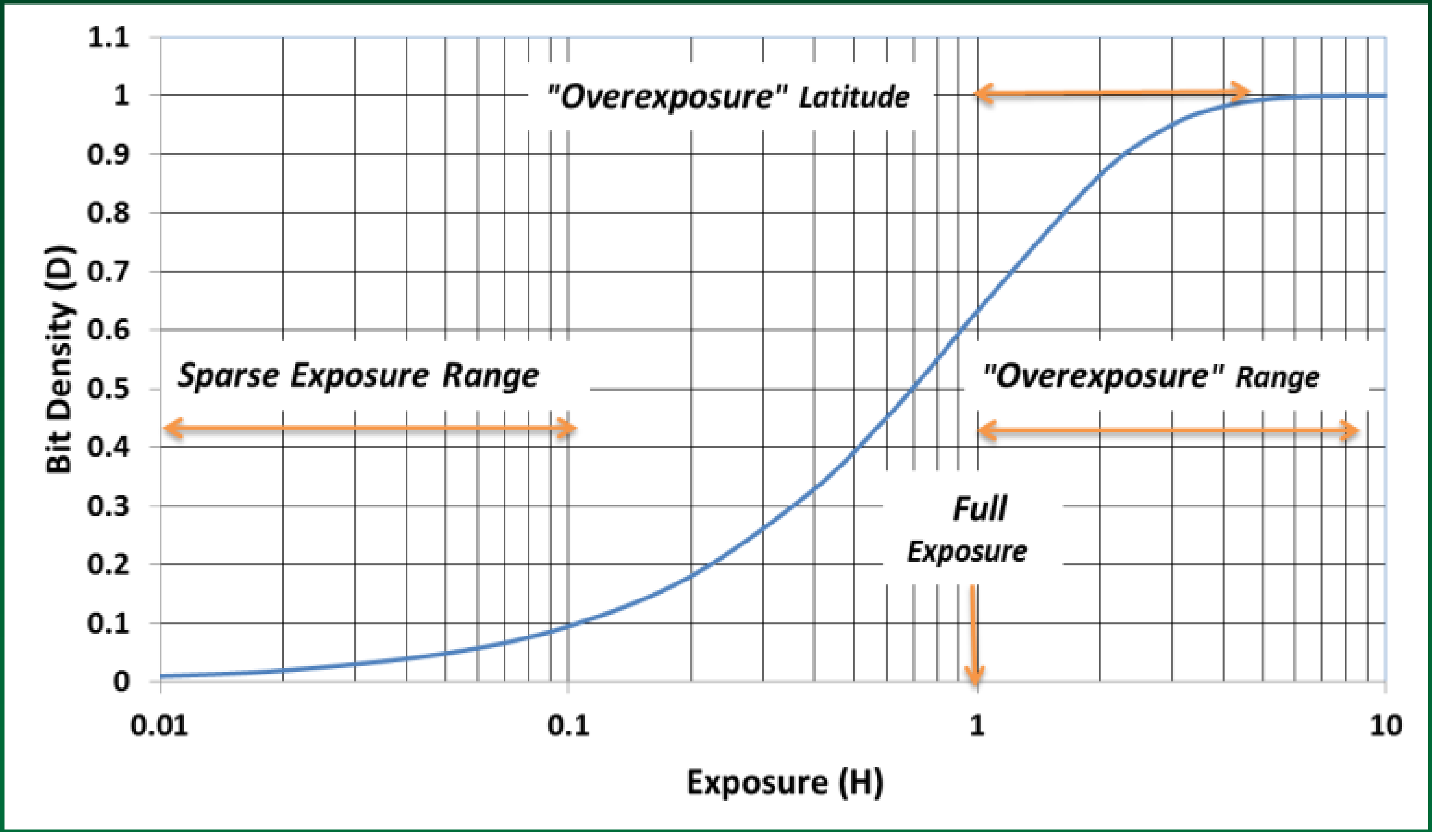
▨ $P[k > 0] = 1 - P[0] = 1 - e^{-H}$

For ensemble of *M* jots, the expected number of 1's : $M_1 = M \cdot P[k > 0]$

Bit Density



$$Bit\ Density\ D \triangleq \frac{M_1}{M} = 1 - e^{-H}$$



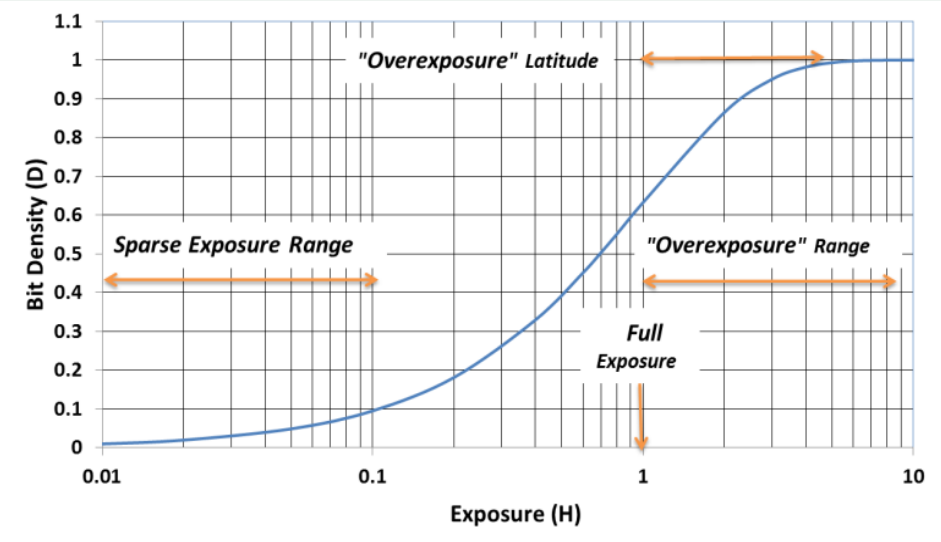
$$D \cong H \quad \text{(linear)}$$

Can determine H from measured D

$$\mathrm{H} = \ln\left[\frac{1}{1-D}\right]$$

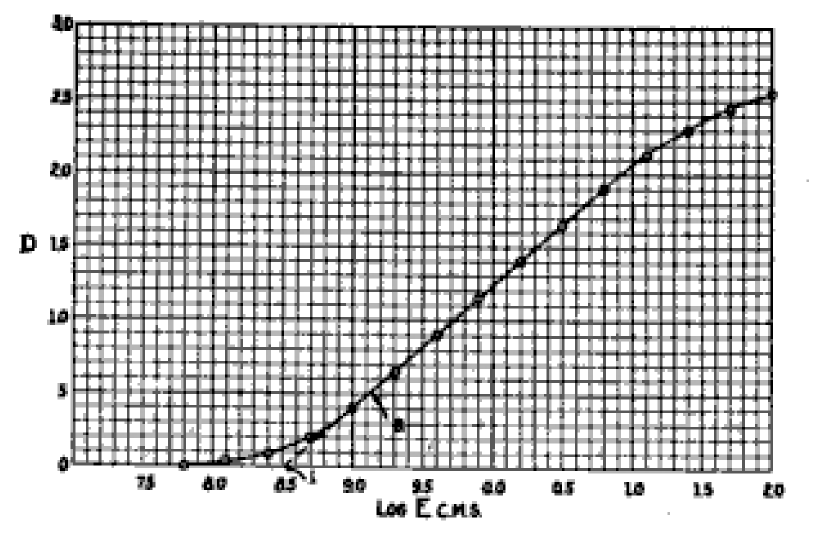
Film-like Exposure Characteristic

QIS D – log H



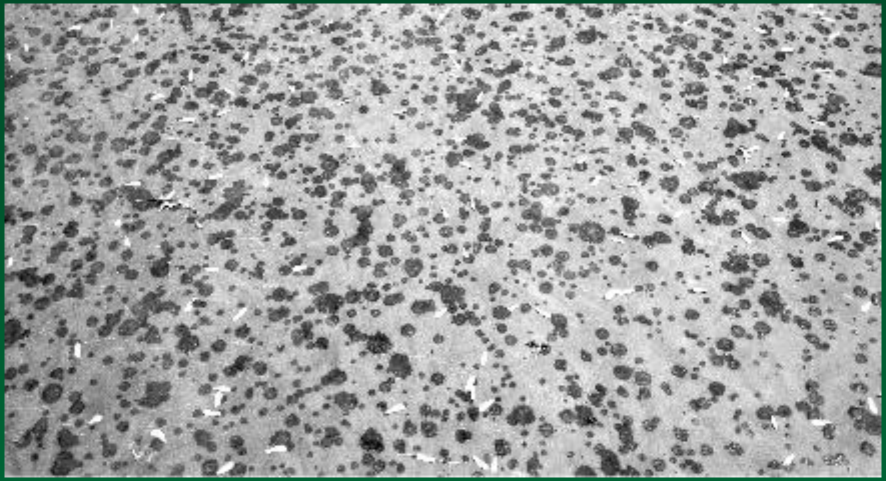
Bit Density vs. Exposure

Film D – log H



Film Density vs. Exposure
1890 Hurter and Driffield

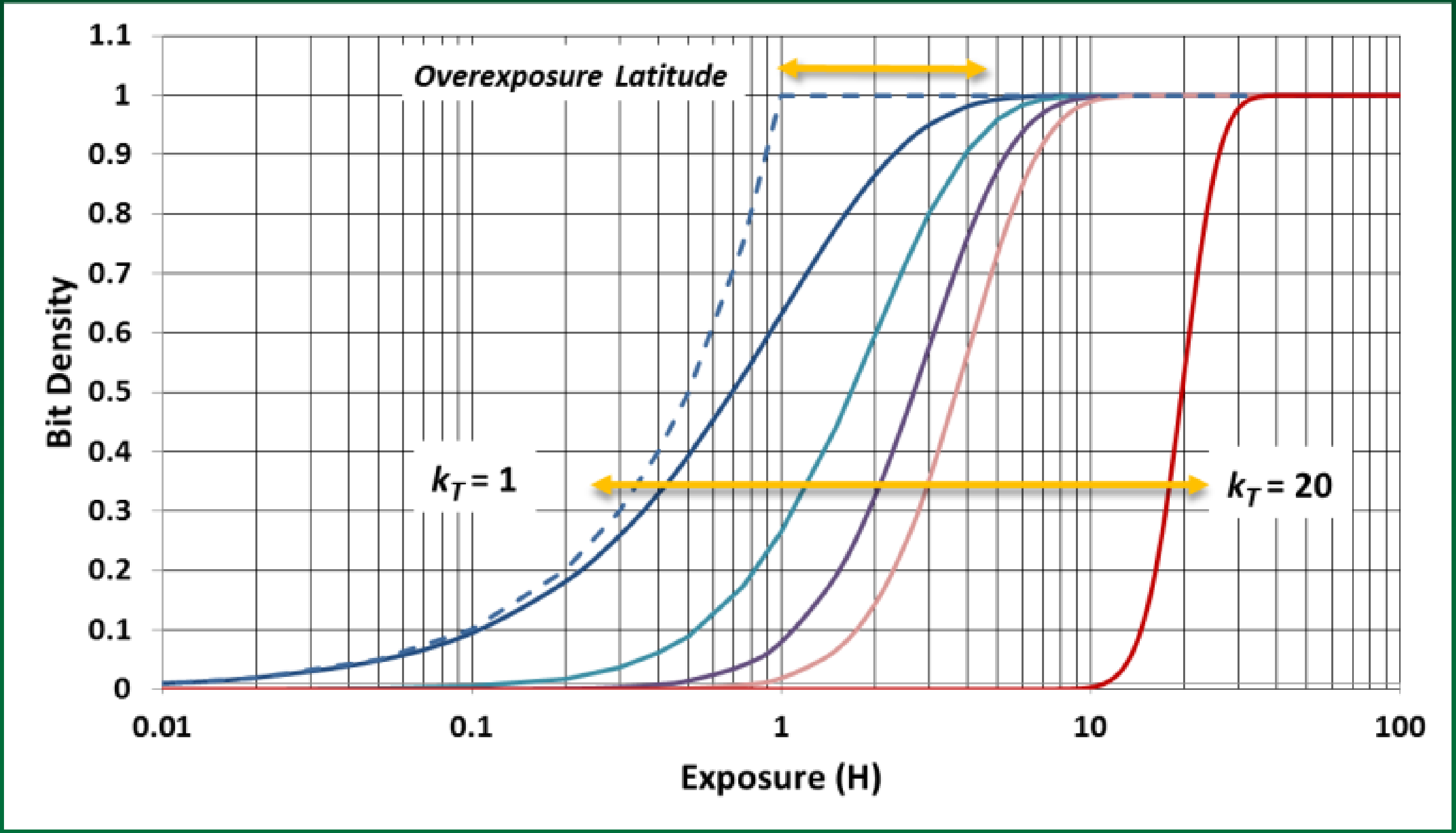
Raindrops on Ground



H~ 0.3 ?

Multi-Arrival Threshold (Binary Sensor but not QIS)

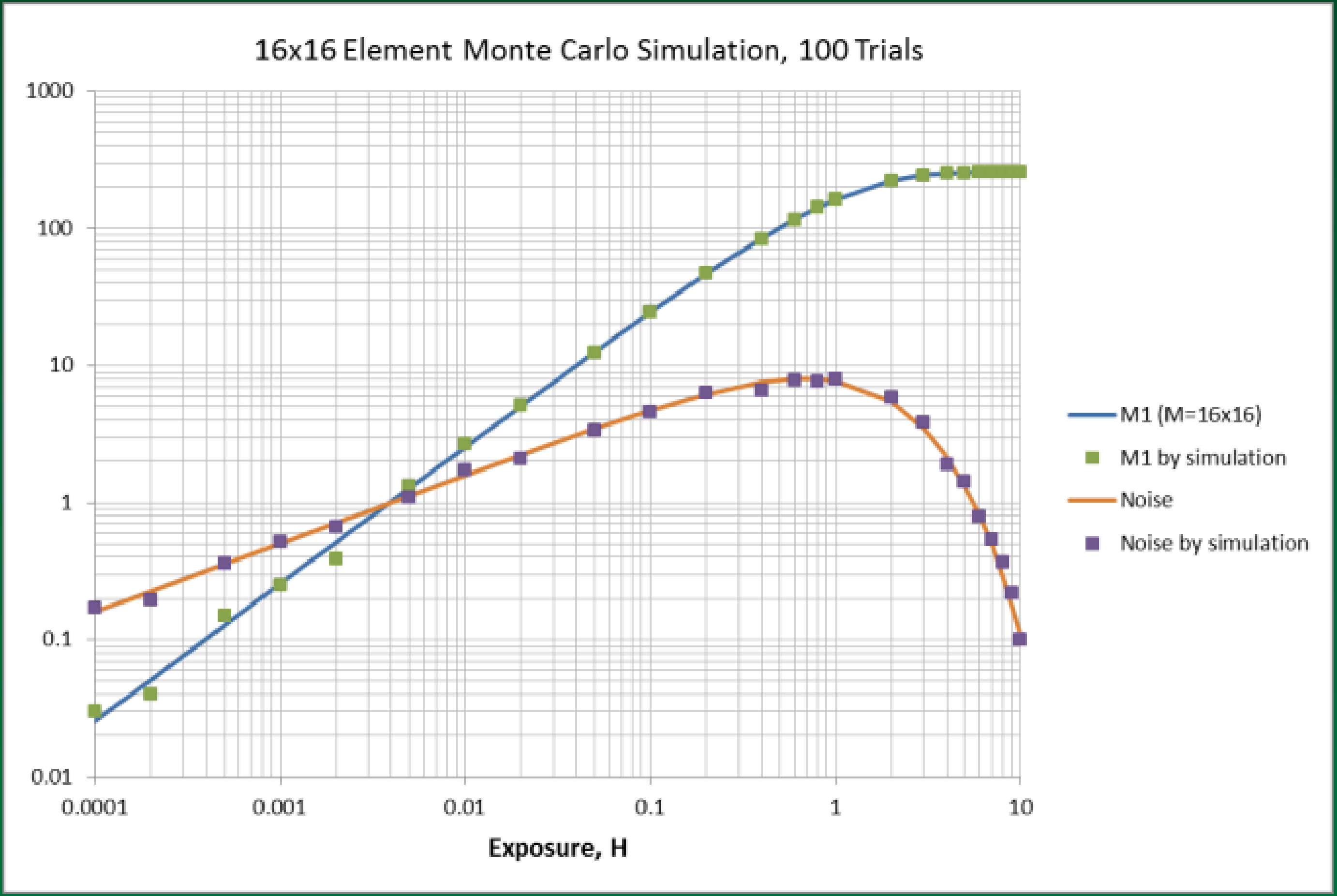
Binary output of sensor =“1” when # of arrivals $k \geq k_T$
Results in reduced higher slope and less overexposure latitude



"Shot" Noise

Variance of a binomial distribution

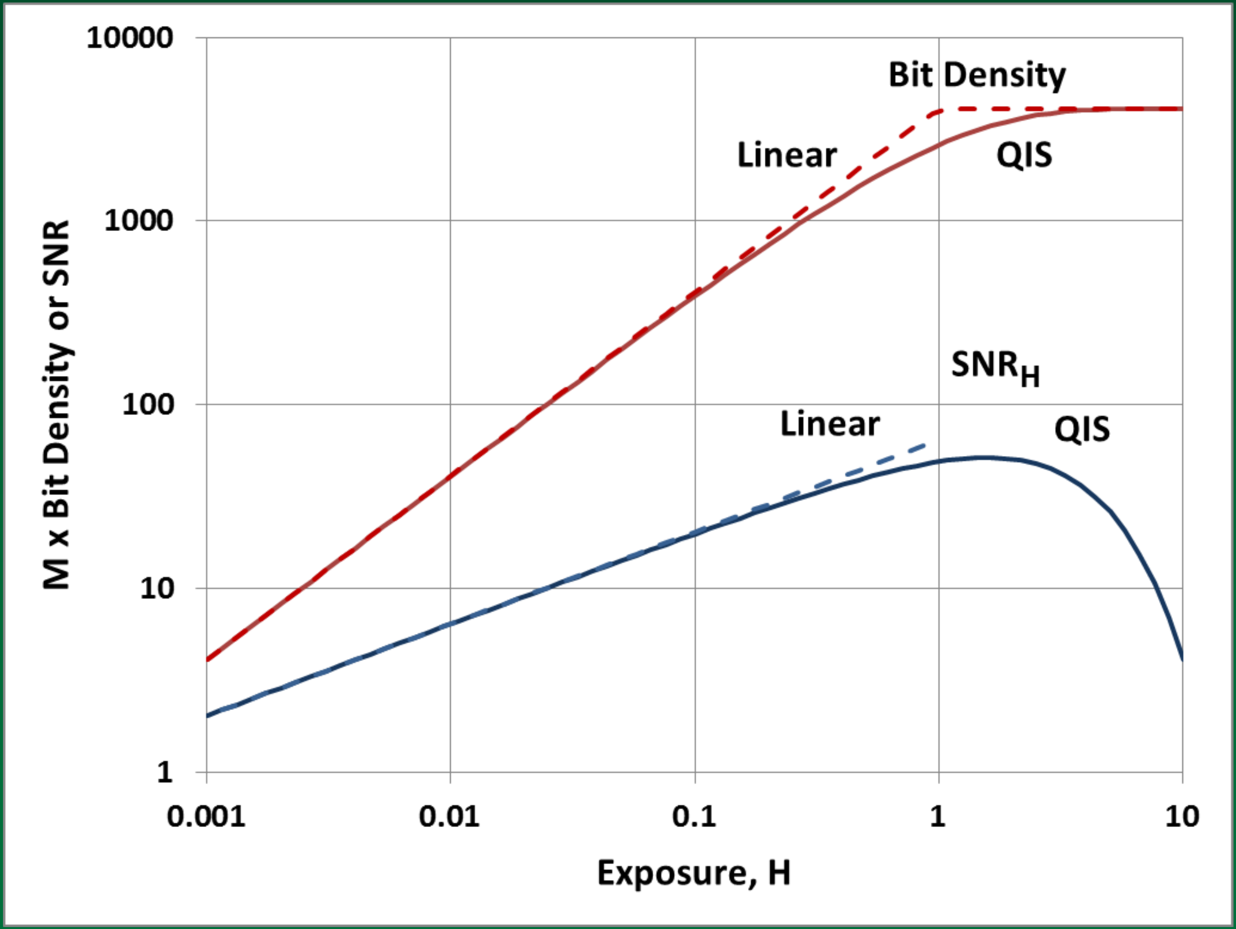
$$\sigma_1{}^2 = M \cdot P[0] \cdot P[k > 0]$$



SNR → ∞ ?

Exposure-Referred Noise

$$\sigma_H = \sigma_1 \frac{dH}{dM_1} \qquad SNR_H = \frac{H}{\sigma_H} = \sqrt{M}\frac{H}{\sqrt{e^H - 1}}$$

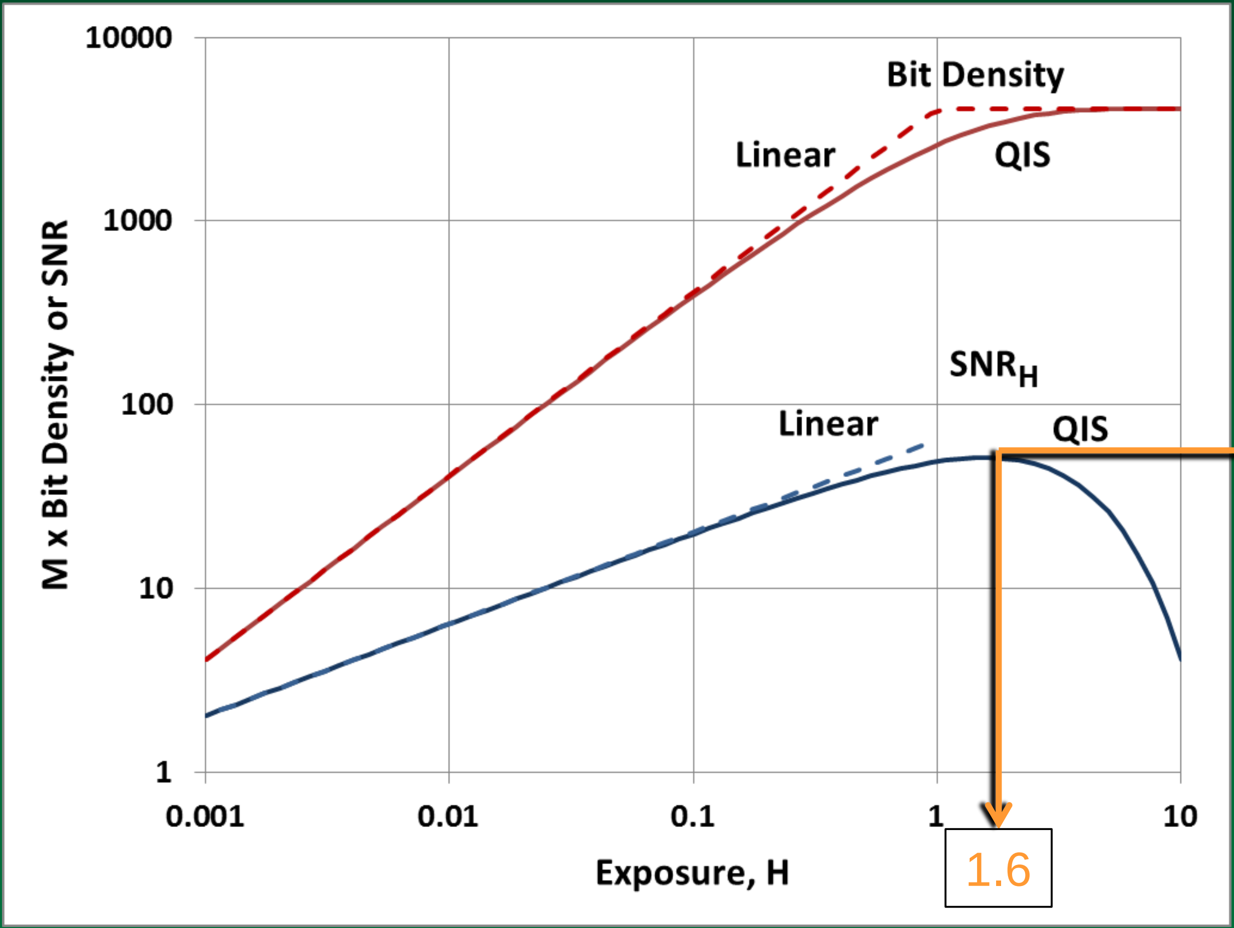


M=4096

$SNR_H \rightarrow 0$

Exposure-Referred Noise

$$\sigma_H = \sigma_1 \frac{dH}{dM_1} \qquad SNR_H = \frac{H}{\sigma_H} = \sqrt{M}\frac{H}{\sqrt{e^H - 1}}$$



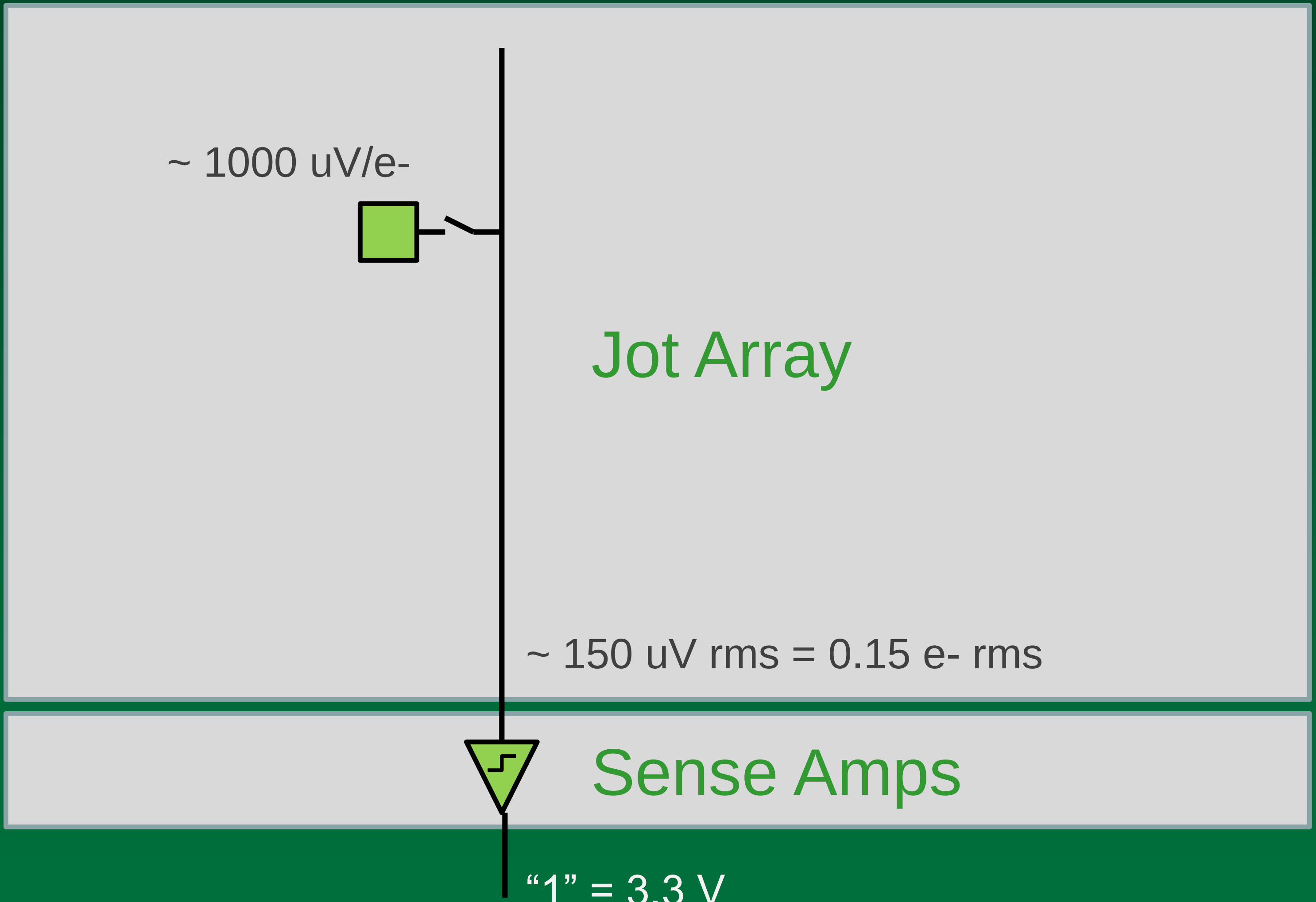
M=4096

51.5
34.2 dB

1.6

THAYER SCHOOL OF ENGINEERING AT DARTMOUTH

Readout Assumption for Read Noise



~ 1000 uV/e-

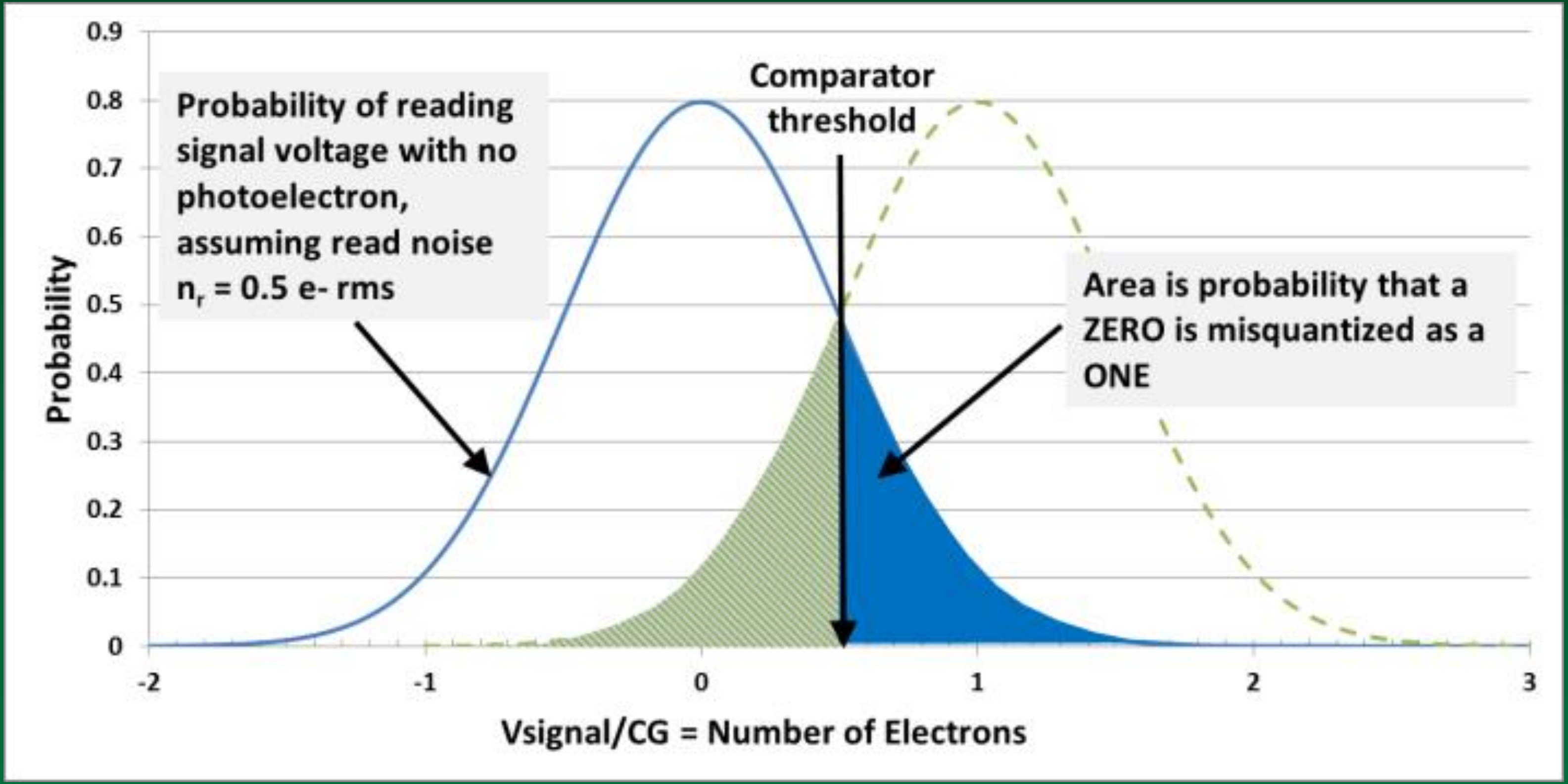
Jot Array

~ 150 uV rms = 0.15 e- rms

Sense Amps

“1” = 3.3 V

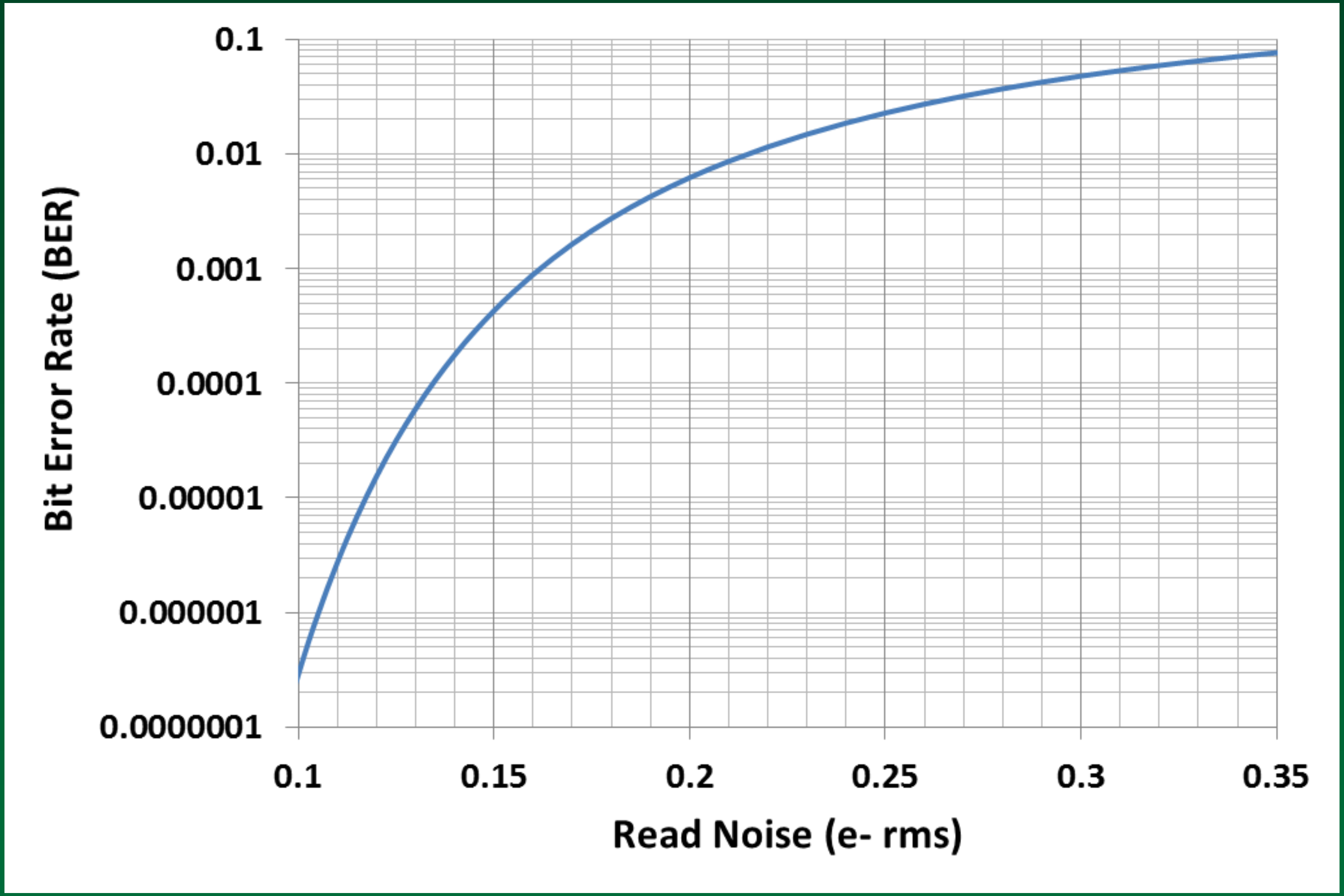
Read Noise and Bit Error Rate (BER)



Probability of reading signal voltage with no photoelectron, assuming read noise n_r = 0.5 e- rms

Area is probability that a ZERO is misquantized as a ONE

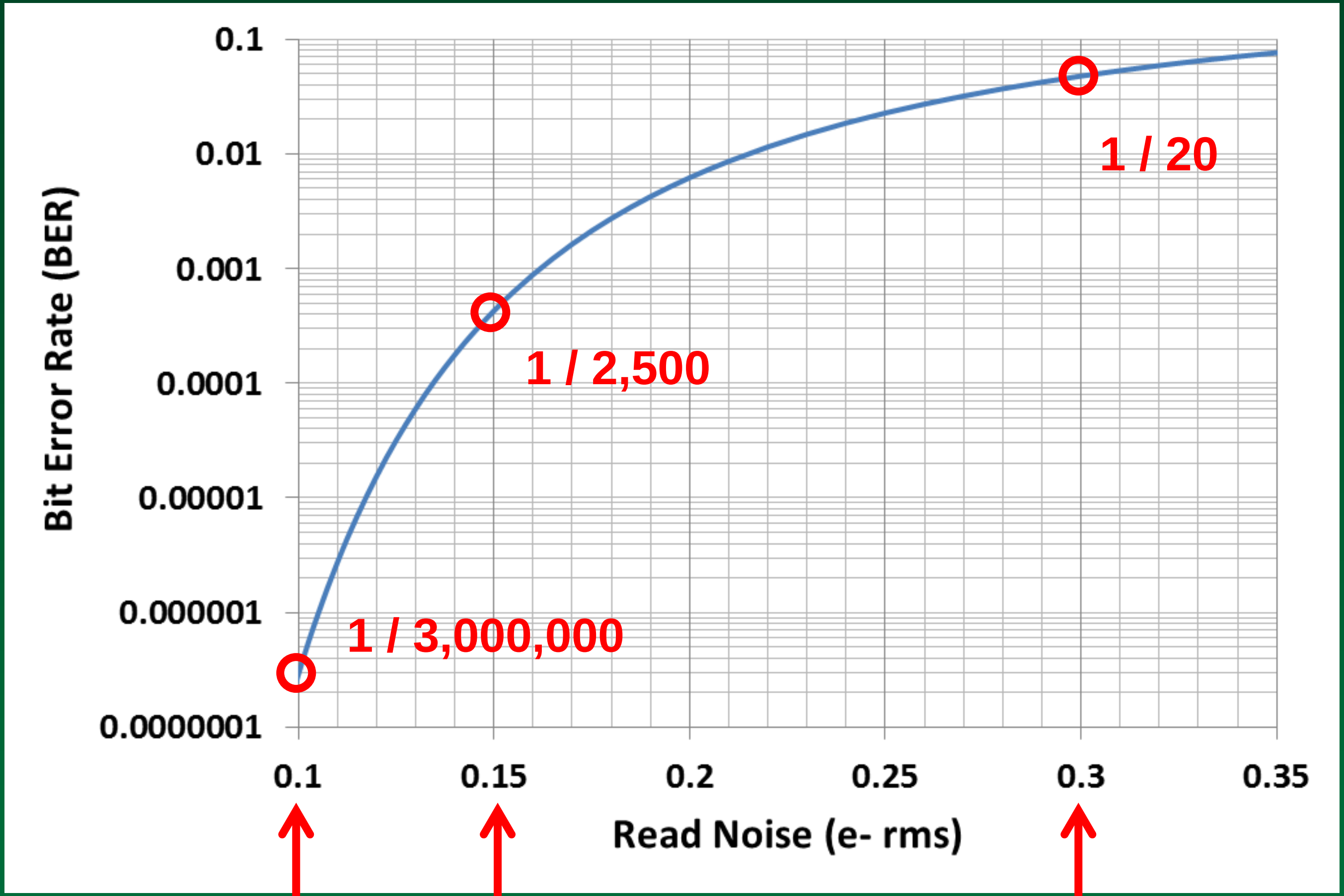
BER vs. Read Noise



$$BER = \frac{1}{2} erfc\left(\frac{1}{\sqrt{8 n_r}}\right)$$

What is an acceptable bit error rate?

BER vs. Read Noise



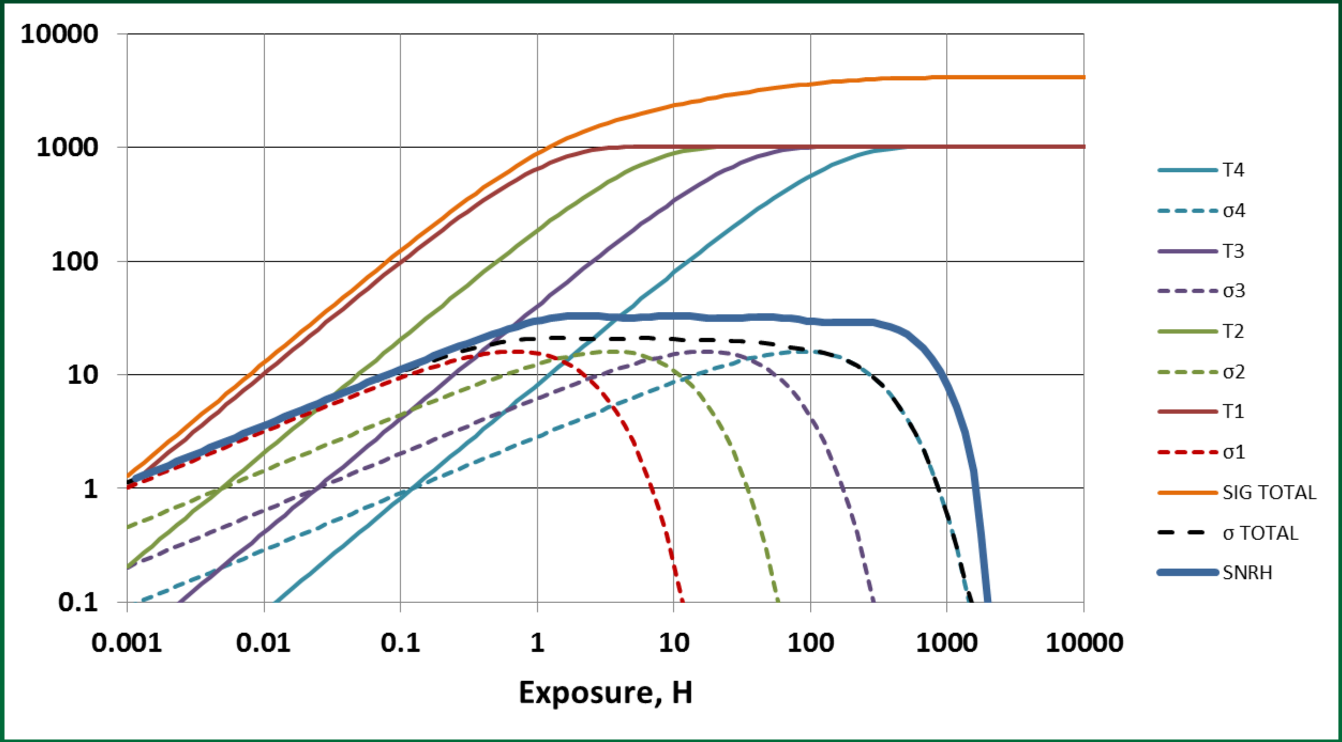
Fossum
2011
WAG

Fossum
2013

Teranishi
2012

Increased Dynamic Range

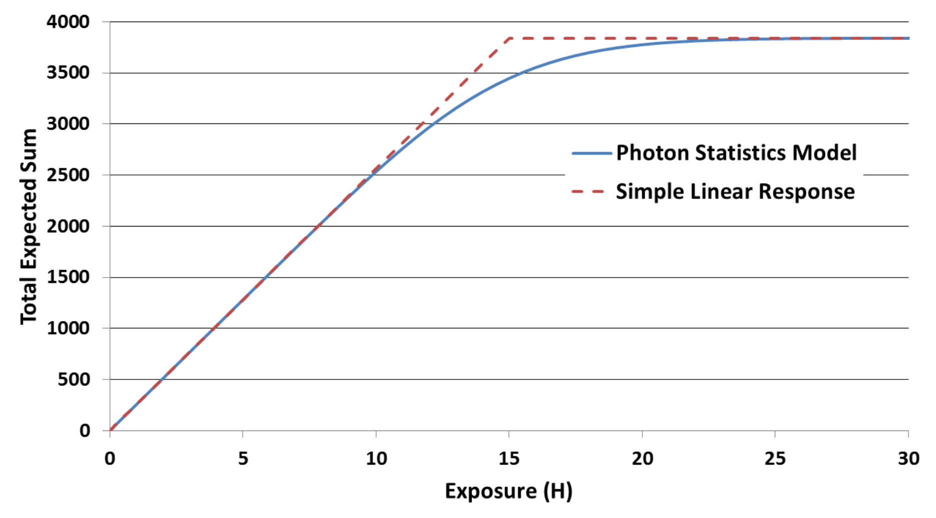
Sum of 16 fields
4@ T=1.0
4@ T=0.2
4@ T=0.04
4@ T=0.008



120 dB

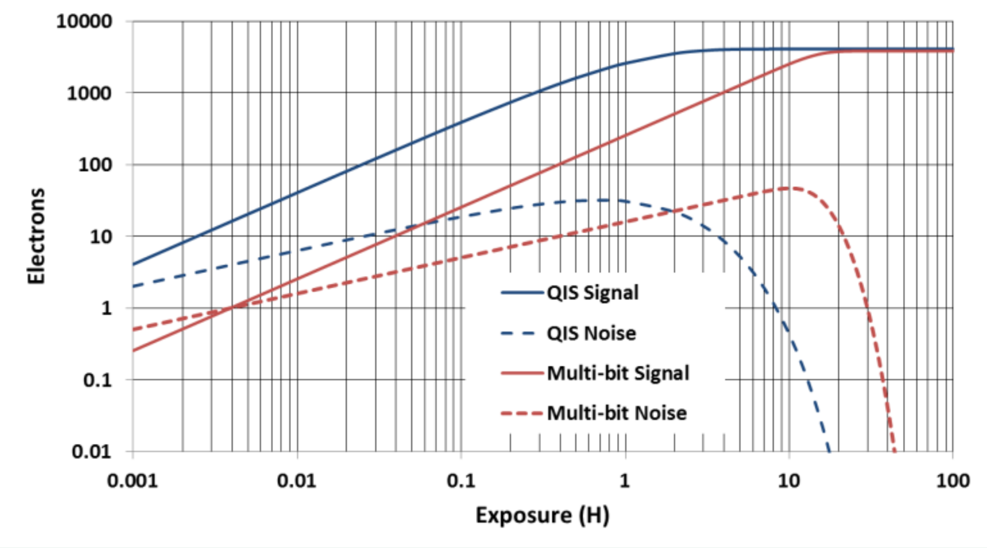
Multi-bit Pixels

Counting low number of photoelectrons, e.g. 4b yields FW = 15 e-



Sum 4x4x16 = 256 pixels
Max = 15x256 = 3840

1b v. 4b



QIS: M=4096
4b: M=273

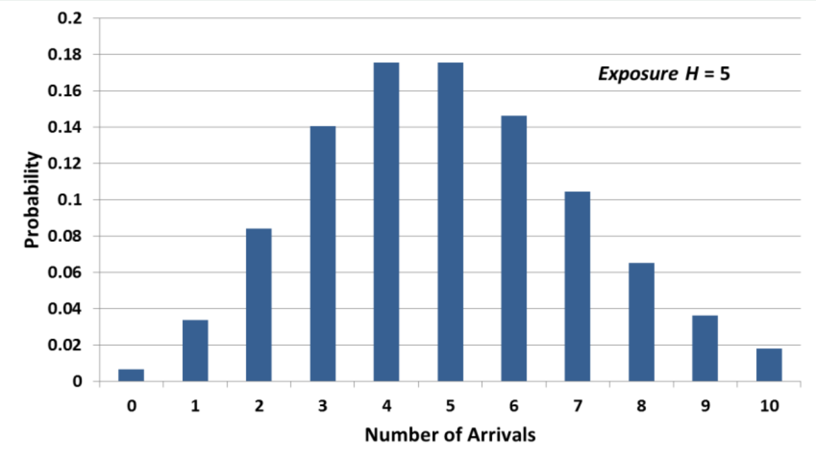
Shot Noise and Read Noise

“Shot” Noise

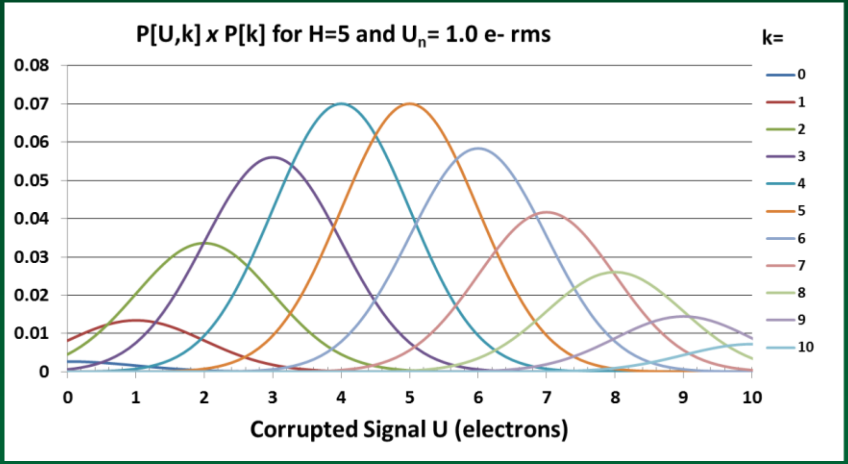
$$\sigma^2 = <k^2> - <k>^2$$

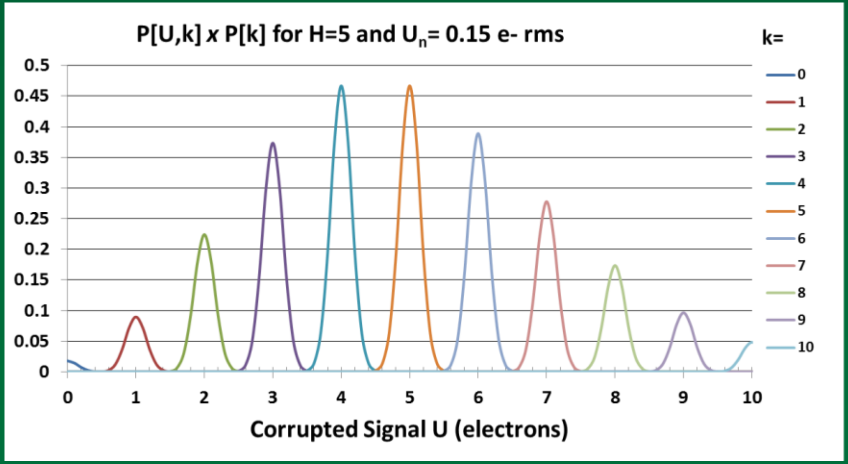
plus

Read Noise (Gaussian model)

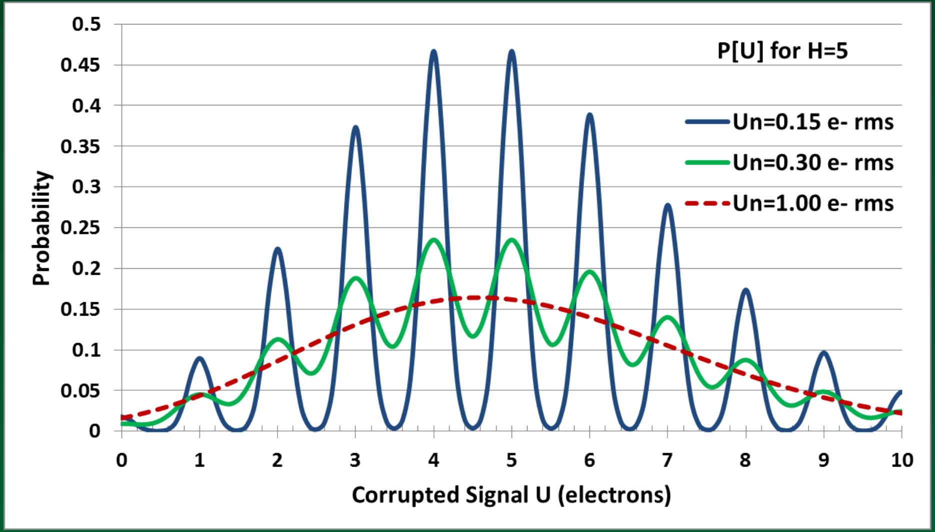


$$P[k] = \frac{e^{-H} H^k}{k!}$$

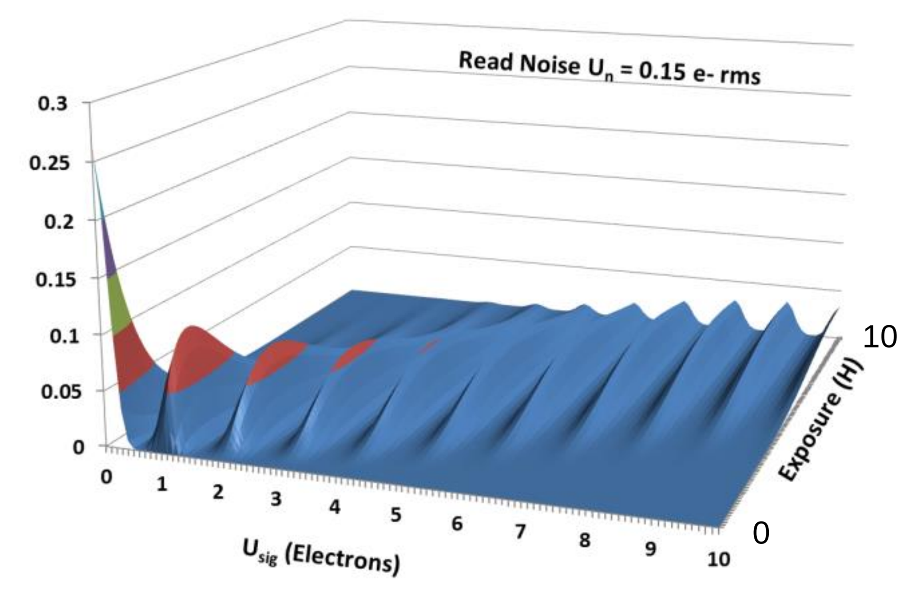




Effect of Read Noise on Photoelectron Counting for Multi-bit Pixel



Note “peak” for H=5 is not at 5 e-



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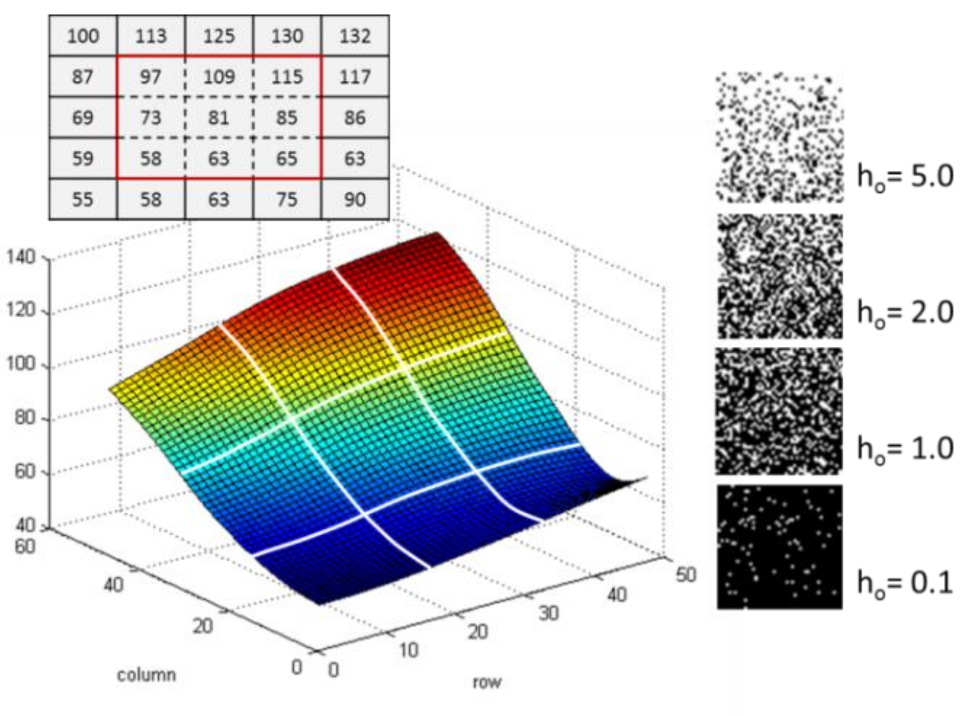
Transforming the Jot Data Cube into Images

Yue Song and E.R. Fossum

End to End System Simulation

Input Image
256x256 8b = 0.5 Mb

→ 4096x4096 1b x 16 fields = 256 Mb



100	113	125	130	132
87	97	109	115	117
69	73	81	85	86
59	58	63	65	63
55	58	63	75	90

$$H = \frac{S_H h_o}{255}$$

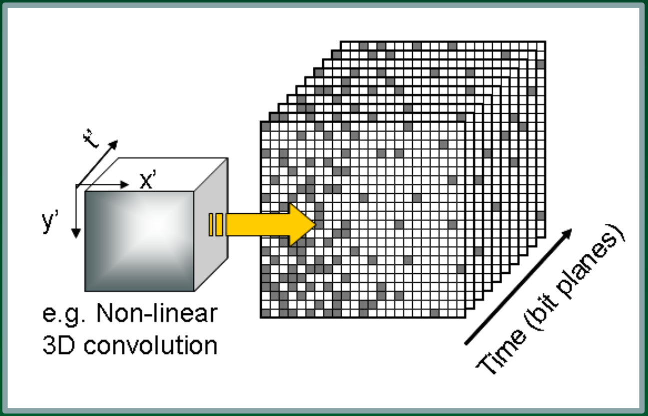
Output Image
1024x1024 8b

in this example

1 pixel = Σ 4x4x16 jots

$$SNR \le \sqrt{256}$$

Convolution

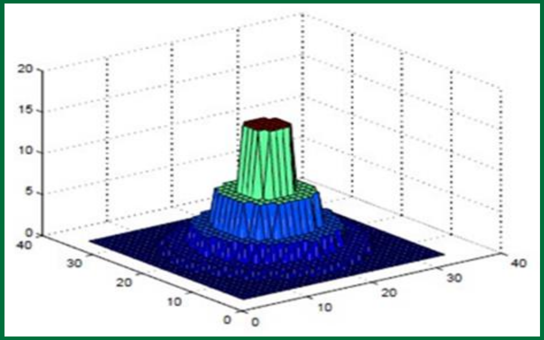


2D Examples:

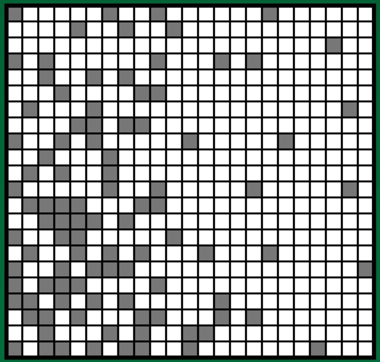
Binary
valued
filter

1	1	1	1
1	1	1	1
1	1	1	1
1	1	1	1

Binary-
weighted
filter

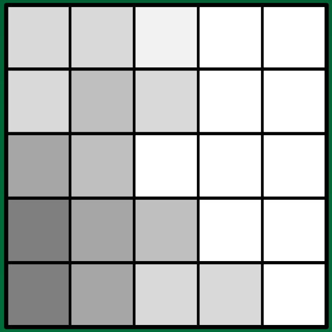


*

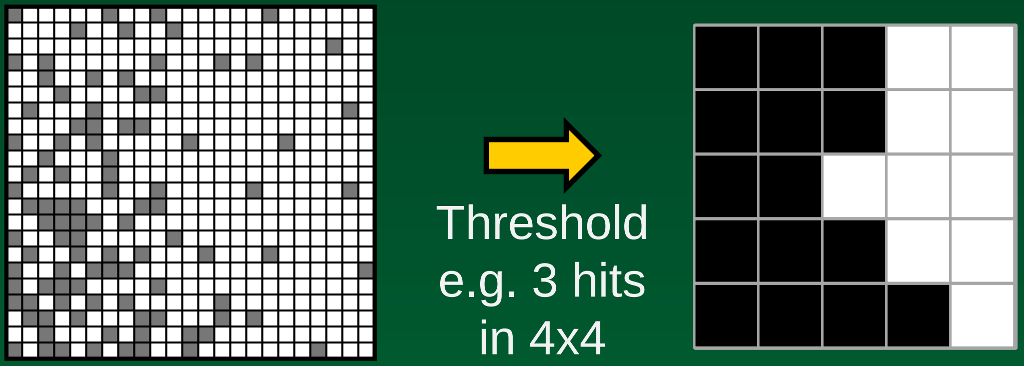


jot data

Down
sample



Digital Film Sensor Algorithm



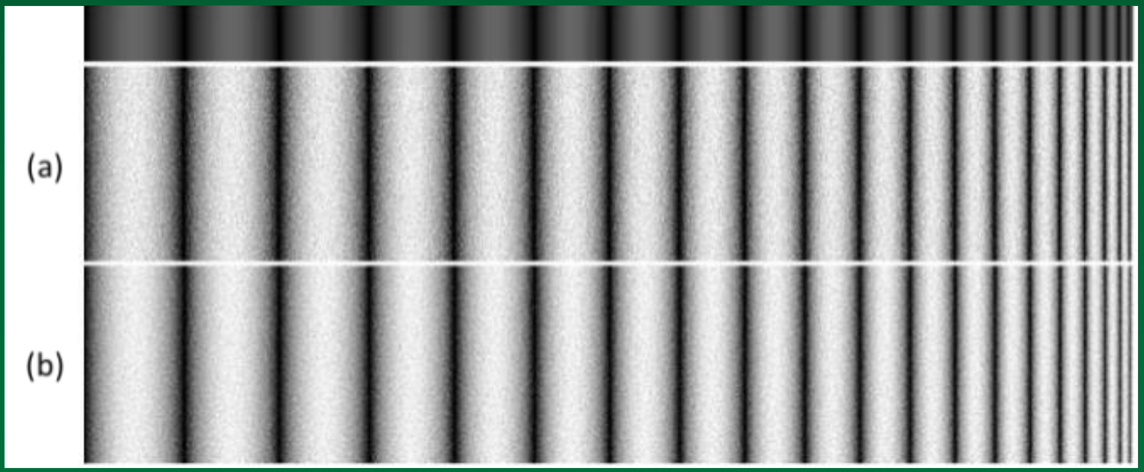
Threshold
e.g. 3 hits
in 4x4

“gain”

Synthetic input image

After DFS development

Plus filter with dynamic kernel size



Readout of Jot Signal to Digital Circuits

Saleh Masoodian, Arun Rao, Song Chen, Kofi Odame and E.R. Fossum

Readout Signal Chain Strawman Design

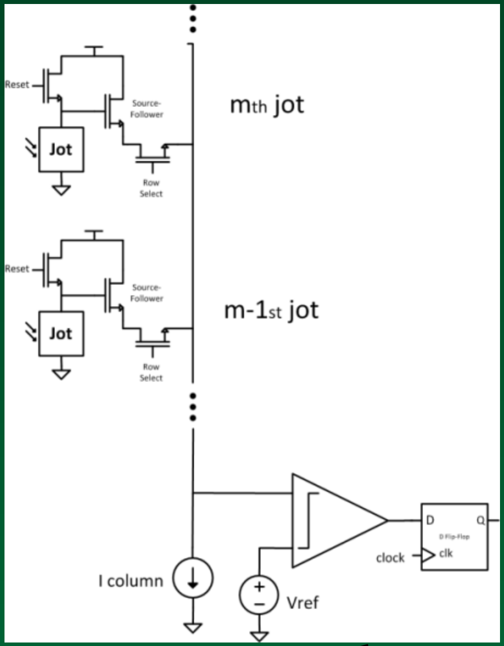
General requirements:

- Need to scan 0.1-10 Gjots at 100-1000 fields per sec
- 8k – 80k jots per column → 0.8 – 80M jots/sec

Assumptions:

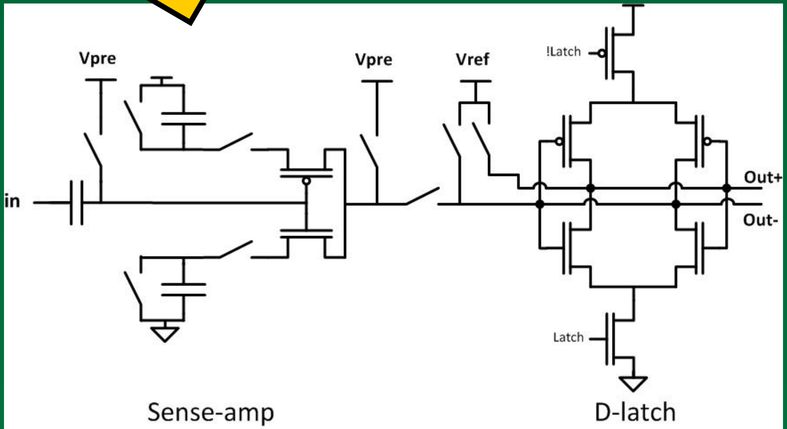
- 0.1 Gjot at 100 fps → 1Mjot/sec
- 1 mV/e- conversion gain
- 150 uV rms noise on column bus (0.15 e- rms)
- 0.18 um process
- Vdd = 1.8V

Readout Signal Chain



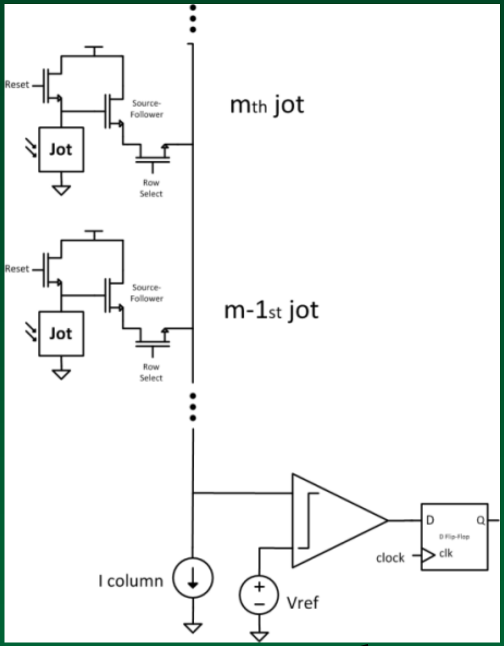
Generic column bus

Process	V_{DD}	Jot array	Column Speed	Column power	Comp power	Total	Array Power
CURRENT DESIGN							
0.18um	1.8V	0.001 Gjots (1k X 1k)	1MJ/s (1000fps)	0.71uW	1.28uW	1.99uW	1.99mW
0.18um	1.8V	0.1 Gjots (10k X 10k)	1MJ/s (100fps)	6.44uW	1.28uW	7.72uW	77.2mW
SCALED DESIGN							
0.18um	1.8V	0.1 Gjots (10k X 10k)	10MJ/s (1000fps)	64.4uW	12.8uW	77.2uW	772mW
45nm	1.1V	1 Gjots (24k X 42K)	24MJ/s (1000fps)	57uW	2.9uW	59.9uW	2.5W
22nm	0.8V	1 Gjots (24k X 42K)	24MJ/s (1000fps)	20uW	0.74uW	20.74uW	0.87W
45nm	1.1V	10 Gjots (75k X 133k)	75MJ/s (1000fps)	553uW	9uW	562uW	75W
22nm	0.8V	10 Gjots (75k X 133k)	75MJ/s (1000fps)	197uW	2.3uW	199.3uW	26.5W



Adapted from Kotani et al. 1998

Readout Signal Chain



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22nm	0.8V	1 Gjots (24k X 42K)	24MJ/s (1000fps)	20uW	0.74uW	20.74uW	0.87W
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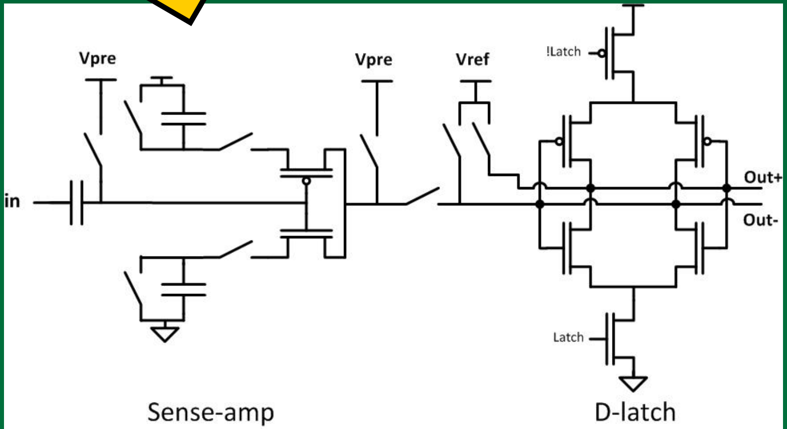
22nm	0.8V	10 Gjots (75k X 133k)	75MJ/s (1000fps)	197uW	2.3uW	199.3uW	26.5W

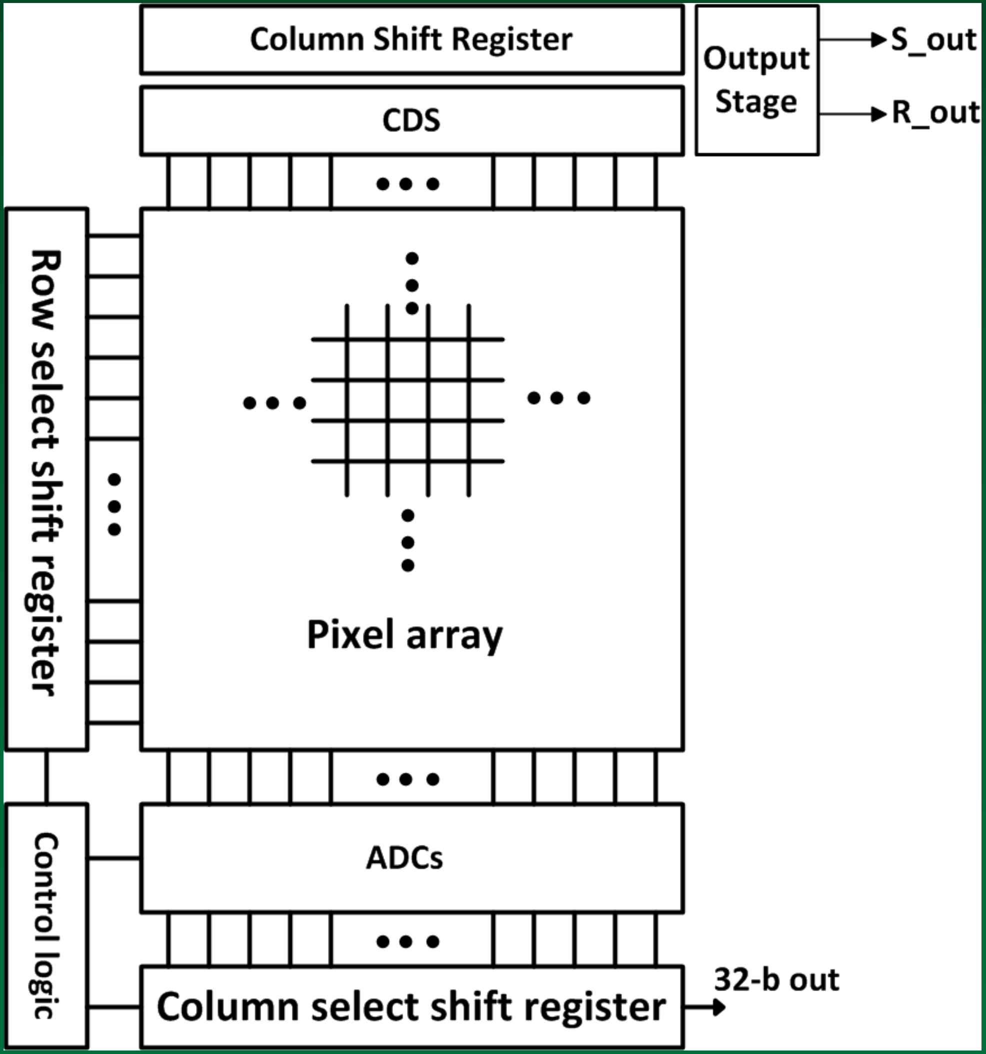


Adapted from Kotani et al. 1998

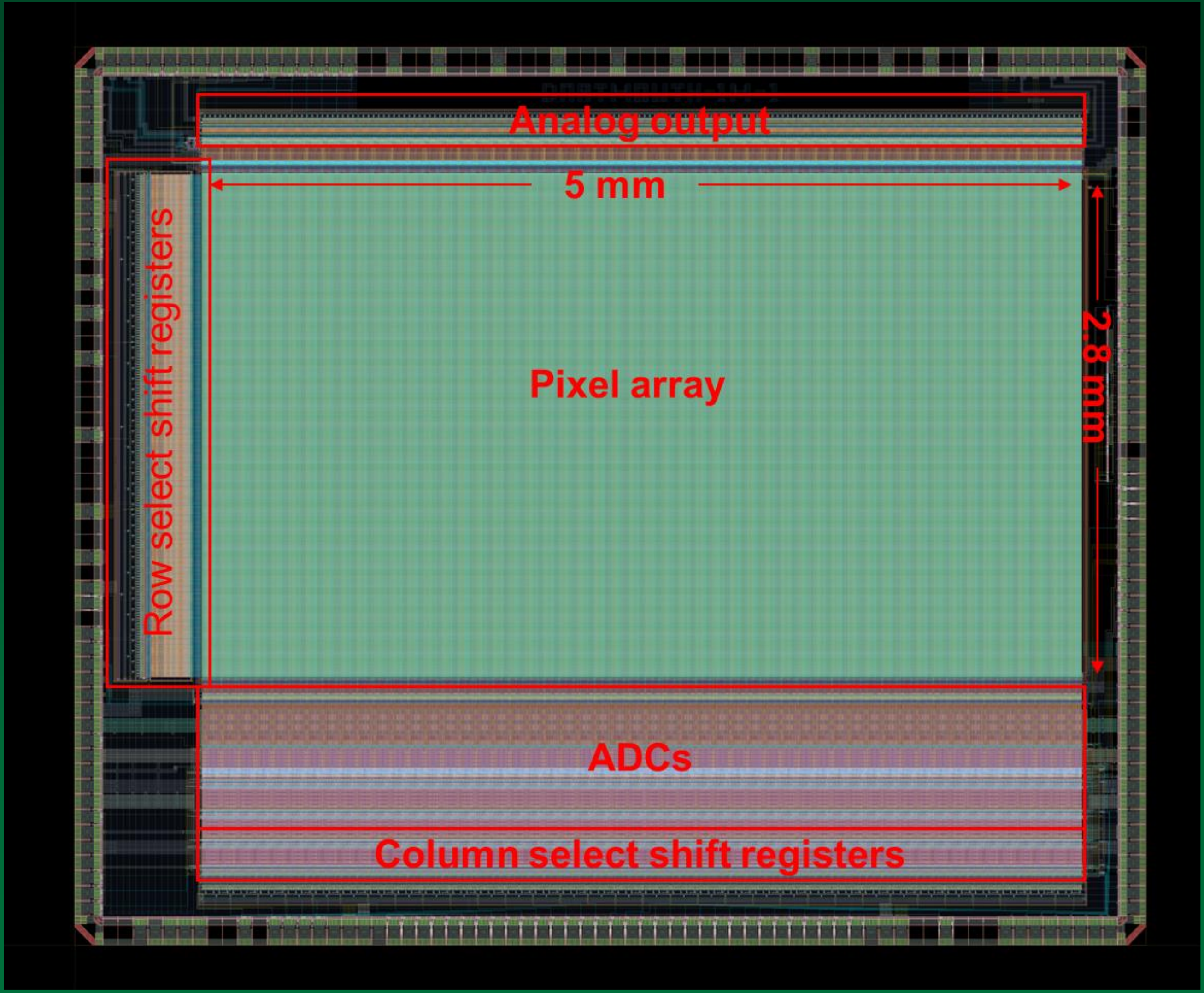
1000fps 1 Mjot binary pixel image sensor

Process	XFAB-XC018, 0.18um, 6M1P	
VDD	1.8V (Analog), 3.3V (Array)	
Pixel type	3T-APS	
Pixel pitch	3.6um	
Photo-detector	Photodiode	
Conversion gain	200uV/e-	
Array	1376(H) X 768(V) (WXGA 16:9 ratio)	
Frame rate	1000fps	
Column noise	< 150uV	
ADC sampling rate	768KSa/s	
ADC input referred offset	<500uV	
Output data rate	32 (output pins) X 33 Mb/s	
Power (Binary imager)	Array	2.3mW
	ADCs	2.5mW
	Digital	5mW
	Total	9.8mW
I/O pad power	50mW	

1000fps 1 Mjot binary pixel image sensor



1000fps 1 Mjot binary pixel image sensor



Chips are just back and packaged but untested

65nm pathfinder for 1 Giga jot at 1000fps

- 1Gjot imager has a 24,000 X 42,000 pixel array
- Limited space for Dartmouth on multi-project chip on multiproject wafer so only 32 columns
- There are 24,000 pixels in each column.
- Power consumption per column is multiplied by 42,000 to get the power consumption of a 1Gjot imager.

65nm pathfinder for 1 Giga jot at 1000fps

<table>
<tr><td>Process</td><td colspan="3">65nm, 1P5M</td></tr>
<tr><td>VDD</td><td colspan="3">1.2V (Analog), 2.5V (Array)</td></tr>
<tr><td>Pixel type</td><td colspan="3">4-shared PPD, 1.75T/pixel</td></tr>
<tr><td>Pixel pitch</td><td colspan="3">1.4um</td></tr>
<tr><td>Array</td><td colspan="3">32(H) X 24000(V)</td></tr>
<tr><td>Frame rate</td><td colspan="3">1000fps</td></tr>
<tr><td>Column noise</td><td colspan="3">< 150uV</td></tr>
<tr><td>ADC sampling rate</td><td colspan="3">24MSa/s</td></tr>
<tr><td>ADC input referred offset</td><td colspan="3"><500uV</td></tr>
<tr><td>Output data rate</td><td colspan="3">32 (output pins) X 24 Mb/s</td></tr>
<tr><td rowspan="3">Estimated Power (Binary imager)</td><td></td><td>One column</td><td>1Gjot
(42K column)</td></tr>
<tr><td>Array</td><td>50uW</td><td>2.1W</td></tr>
<tr><td>ADC</td><td>15uW</td><td>0.63W</td></tr>
</table>

Design in progress, tapeout end of June

Single Bit v. Multi-bit

Single Bit

- Each jot produces 1 bit
- 1 bit ADC
- For same flux of photoelectrons, need higher frame rate readout
- Conceptual simplicity
- Easier on chip digital electronics

Multi-bit

- Each jot produces n bits
- n-bit ADC
- For same flux of photoelectrons, lower relative frame rate $1/2^{(n-1)}$
- Like current CMOS APS but low FW capacity and high conversion gain (quantized digital integration sensor qDIS*)

*S, Chen, A. Ceballos, E.R. Fossum, 2013 IISW

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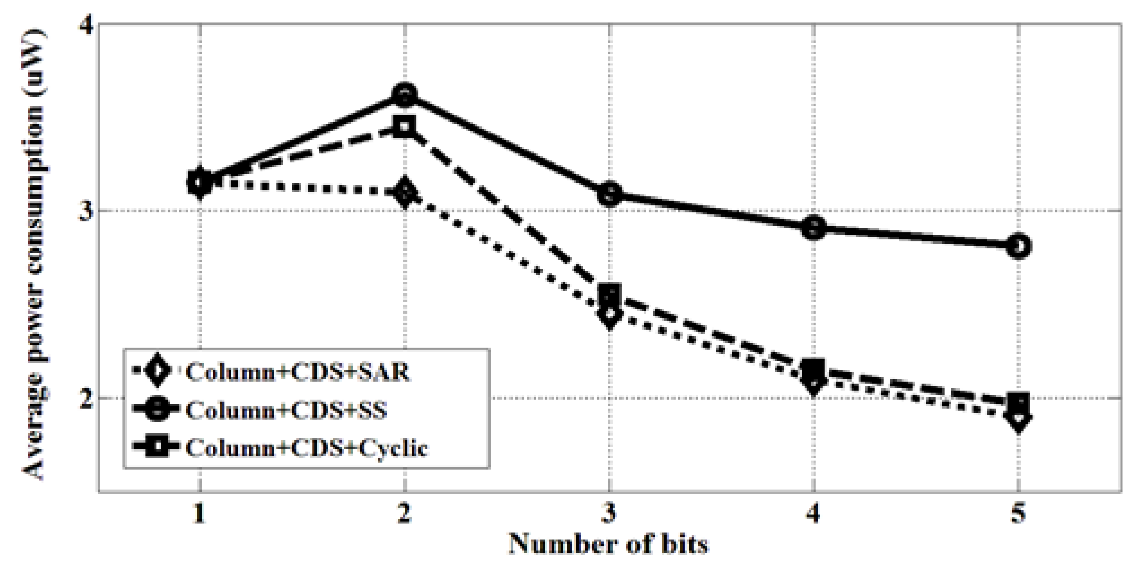
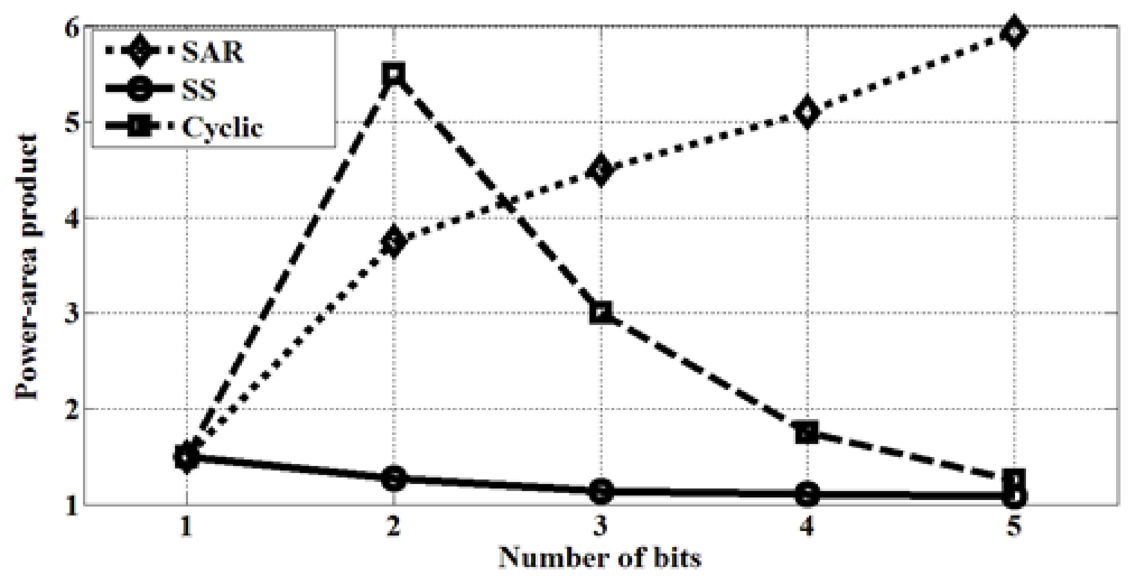
Single Bit v. Multi-bit Power Comparison





Jots

Jiaju Ma, Donald Hondongwa and E.R. Fossum

Jot Device Considerations

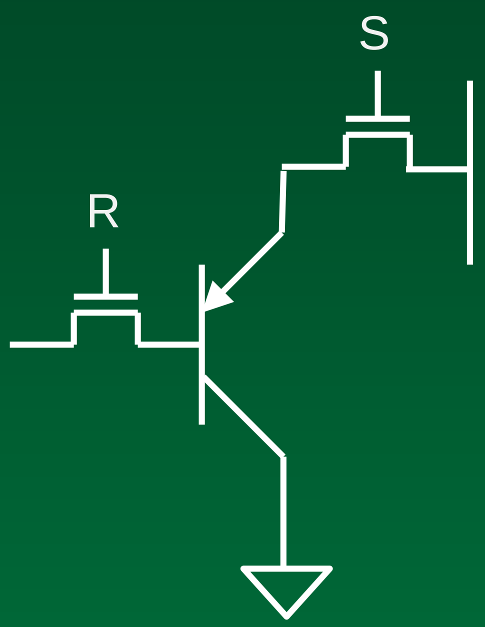
General requirements:

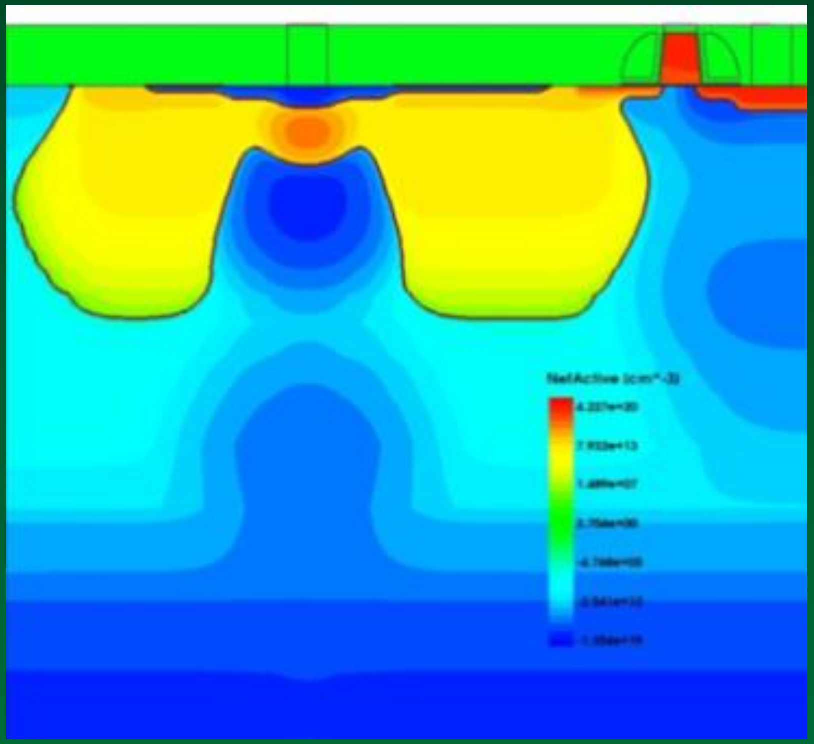
- 200 nm device in 22 nm process node (“10L”)
- High conversion gain > 1 mV/e- (per photoelectron)
- Small storage well capacity ~1-100 e-
- Complete reset for low noise
- Low active pixel transistor noise <150 uV rms
- Low dark current ~ 1 e-/s
- Not too difficult to fabricate in CIS line

For early investigation

- Cobbled together an imaginary 85 nm process
- Students learned to use TCAD tools etc.
- Anticipated that device principles can be migrated to real process

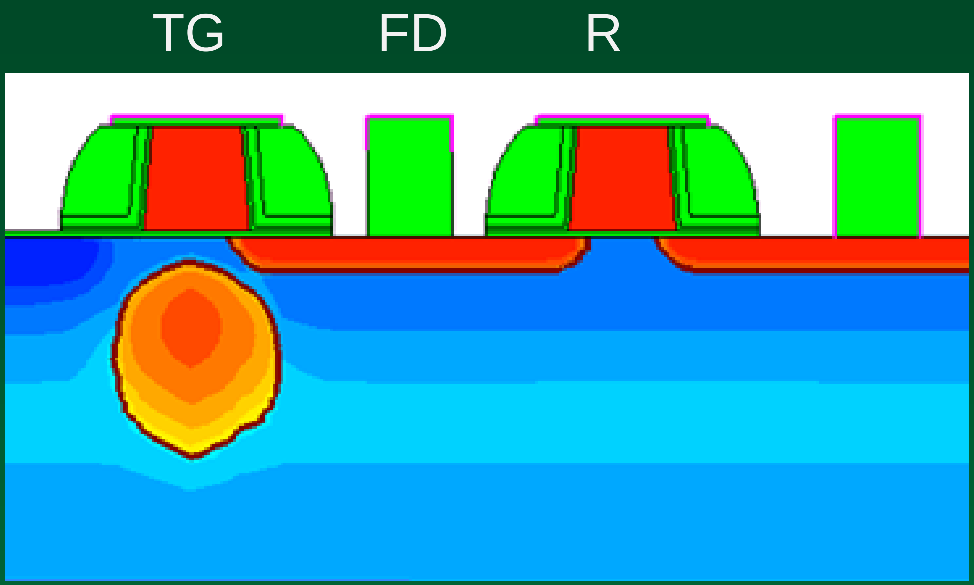
Bipolar Jot Concept





- CMOS APS but use pinning layer as emitter, storage well as base
- Complete reset of base using “TG”
- Emitter follower to reduce base-emitter cap

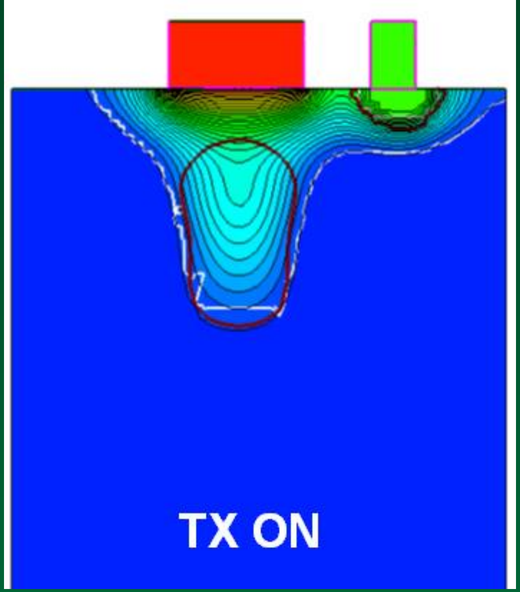
BSI CMOS APS Jot with Storage under Transfer Gate

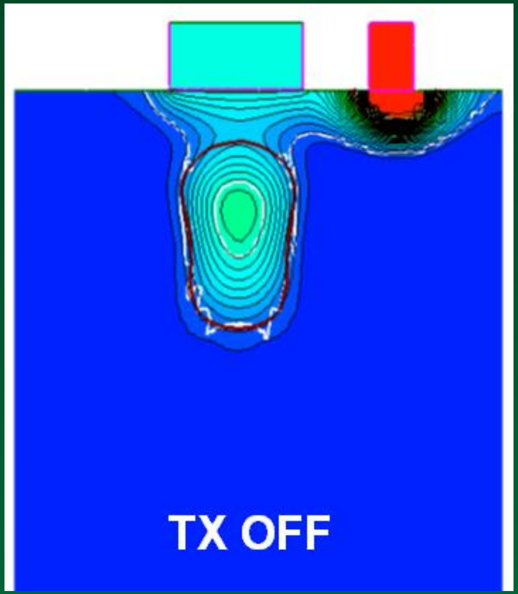


- Low capacity storage gate makes barrier easier to overcome with low TG voltage
- Minimum FD size to increase conversion gain

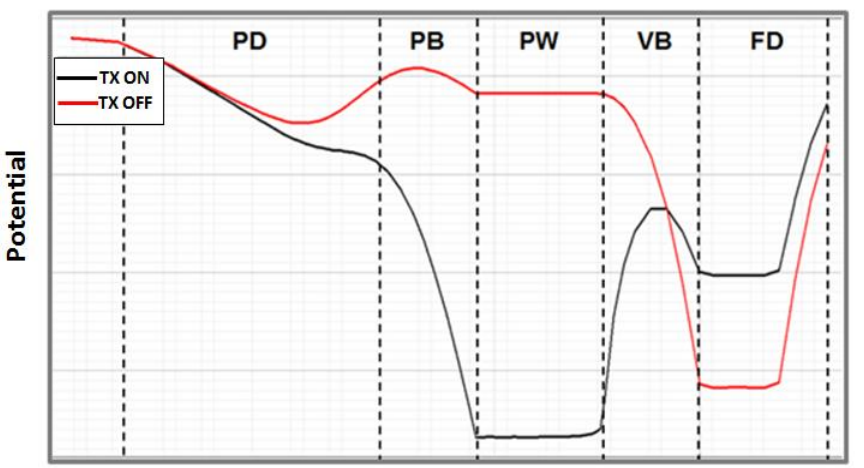
Storage under transfer gate first proposed in
Back Illuminated Vertically Pinned Photodiode with in Depth
Charge Storage, by J. Michelot, et al., 2011 IISW

Pump-gate Jot Device
To Increase Conversion Gain





- 65 nm Node
- 1.4 um pitch
- 3.3 V operation
- 200 e- FW
- >300 uV/e-

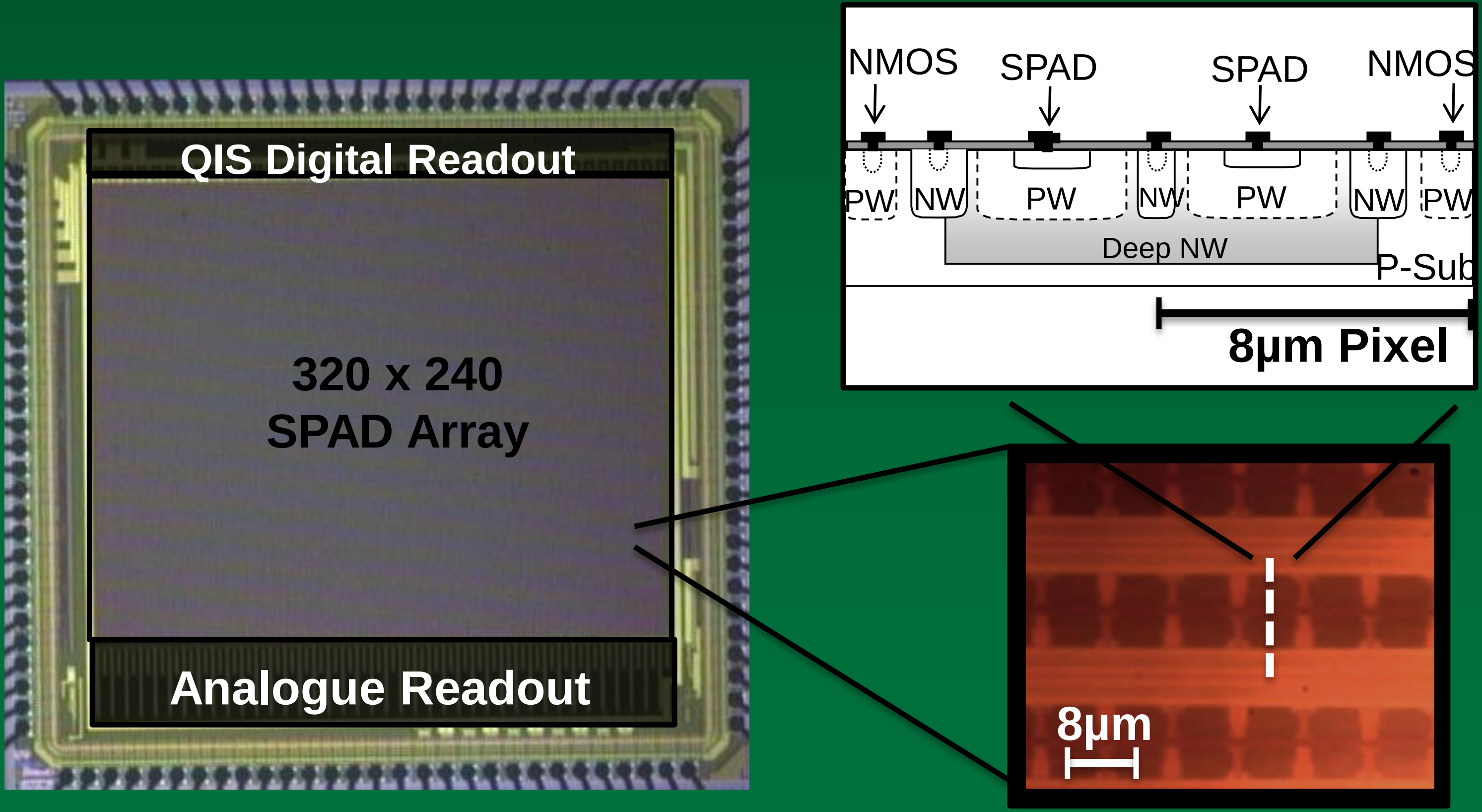


Test array tapeout
June 2014

SPAD Implementation of QIS At Univ. Edinburgh

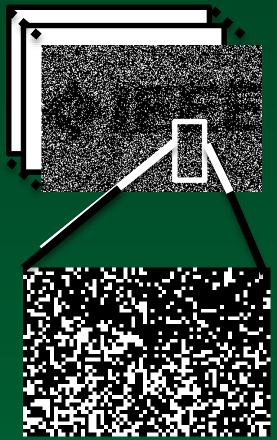
320x240 SPAD-based QIS

- Dutton et al. *IEEE VLSI Symposium* 2014
- University of Edinburgh & ST Microelectronics
- 8µm SPAD-based Pixel with 26.8% FF



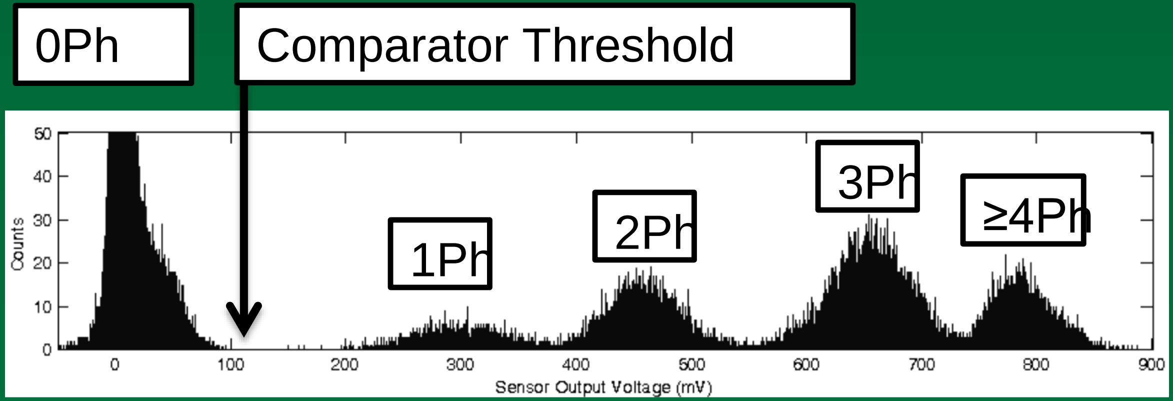
320x240 SPAD-based QIS

Dutton et al. *IEEE VLSI Symposium* 2014



5k FPS
Binary Frames

20 FPS 8b DR
(256 frames summed)



Summary

- Good progress in understanding response v. exposure, SNR, DR, etc. using photon statistics
- Early progress made on realizing Quanta Image Sensor
- >2 years support of Rambus (thanks Rambus!)
- Students up to speed and making great headway
- Challenges don’t look as challenging
- Lots of work still to do!