Quanta Image Sensor (QIS) - an oversampled visible light sensor

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  - Dr. Igor Carron (the net)
  - Prof. Atsushi Hamasaki
  - Rambus Inc.
Motivation for this work

• Pixel shrink yields smaller full-well capacity which impacts dynamic range and maximum SNR.
• Photons, or quanta, are digital in nature according to particle view of light and can be represented by binary data.
• Better images can be obtained by oversampling in time and space.
Original goal for QIS was to make a very tiny, specialized pixel ("jot") which could sense a single photoelectron.

Jots would be readout by scanning at a high frame rate to avoid likelihood of multiple hits in the same jot and loss of accurate counting.

Image pixels could be created by combining jot data over a local spatial and temporal region using image processing.

The first proposed algorithm was the "digital film sensor" using a "grain" and "digital development" construct.
Jot = specialized sub-diffraction limit (SDL) pixel, sensitive to a single photoelectron with binary output, “0” for no photoelectron, “1” for at least one photoelectron.

Many jots are needed to create a single image pixel.

e.g. 16x16x16 = 4,096

A QIS might have 1G jots, read out at 1000 fields/sec or 1.0 Tbits/sec
Problems we have been working on

1. Photons to photoelectrons
   - Just starting – how does light get absorbed by small semiconductor jot structures

2. Photoelectrons to jot signal
   - Invent and evaluate candidate jot devices
   - TCAD modelling of those devices

3. Readout of jot signal to digital circuits
   - Low power, single-bit ADC-per-column

4. Getting massive amounts of data off-chip
   - Compression and compressive sensing?

5. Transforming jot data cube into image
   - Algorithms

6. Understanding imaging characteristics
Understanding QIS Imaging Characteristics

September 2013.
Photon and photoelectron arrival rate described by Poisson process

Define *quanta exposure* \( H = \Phi \tau \) \( H = 1 \) means expect 1 arrival on average.

Probability of \( k \) arrivals

\[
P[k] = \frac{e^{-H} H^k}{k!}
\]

Monte Carlo

For jot, only two states of interest

\[
P[0] = e^{-H}
\]

\[
P[k > 0] = 1 - P[0] = 1 - e^{-H}
\]

For ensemble of \( M \) jots, the expected number of 1’s: \( M_1 = M \cdot P[k > 0] \)
Bit Density

\[ Bit \text{ Density} \; D \triangleq \frac{M_1}{M} = 1 - e^{-H} \]

Can determine \( H \) from measured \( D \)

\[ H = \ln \left[ \frac{1}{1 - D} \right] \]

\( D \approx H \) \( \text{(linear)} \)
Film-like Exposure Characteristic

QIS D – log H

Film D – log H

Bit Density vs. Exposure

Film Density vs. Exposure
1890 Hurter and Driffield
Raindrops on Ground

H~ 0.3?
Multi-Arrival Threshold (Binary Sensor but not QIS)

Binary output of sensor = “1” when # of arrivals \( k \geq k_T \)

Results in reduced higher slope and less overexposure latitude

![Graph showing Overexposure Latitude](image)
“Shot” Noise

Variance of a binomial distribution

\[ \sigma_1^2 = M \cdot P[0] \cdot P[k > 0] \]

SNR \(\to\) \(\infty\) ?
\[ \sigma_H = \sigma_1 \frac{dH}{dM_1} \]

\[ SNR_H = \frac{H}{\sigma_H} = \sqrt{M} \frac{H}{\sqrt{e^H - 1}} \]

Exposure-Referred Noise

\[ M = 4096 \]

SNR_H \to 0
Exposure-Referred Noise

\[ \sigma_H = \sigma_1 \frac{dH}{dM_1} \]

\[ \text{SNR}_H = \frac{H}{\sigma_H} = \sqrt{M} \frac{H}{\sqrt{e^H - 1}} \]

\( M = 4096 \)

51.5 dB
34.2 dB
Readout Assumption for Read Noise

- \(~ 1000 \text{ uV/e-}\)
- \(~ 150 \text{ uV rms} = 0.15 \text{ e- rms}\)
- "1" = 3.3 V

Jot Array

Sense Amps
Read Noise and Bit Error Rate (BER)

Probability of reading signal voltage with no photoelectron, assuming read noise $n_r = 0.5 \text{ e- rms}$

Comparator threshold

Area is probability that a ZERO is misquantized as a ONE

$V_{signal}/CG = \text{Number of Electrons}$
What is an acceptable bit error rate?

\[
BER = \frac{1}{2} \text{erfc} \left( \frac{1}{\sqrt{8n_r}} \right)
\]
BER vs. Read Noise

Bit Error Rate (BER)

Read Noise (e- rms)

1 / 20

1 / 2,500

1 / 3,000,000

Fossum 2011
Fossum 2013
Teranishi 2012

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Increased Dynamic Range

Sum of 16 fields
4@ T=1.0
4@ T=0.2
4@ T=0.04
4@ T=0.008

120 dB
Multi-bit Pixels

Counting low number of photoelectrons, e.g. 4b yields FW = 15 e-

Sum $4 \times 4 \times 16 = 256$ pixels
Max $= 15 \times 256 = 3840$

QIS: $M=4096$
4b: $M=273$

1b v. 4b
"Shot" Noise

\[ \sigma^2 = <k^2> - <k>^2 \]

Read Noise (Gaussian model)

\[ P[k] = \frac{e^{-H} H^k}{k!} \]
Effect of Read Noise on Photoelectron Counting for Multi-bit Pixel

Note “peak” for H=5 is not at 5 e-
Transforming the Jot Data Cube into Images

Yue Song and E.R. Fossum
End to End System Simulation

Input Image
256x256 8b = 0.5 Mb

→ 4096x4096 1b x 16 fields = 256 Mb

in this example
1 pixel = \( \sum 4 \times 4 \times 16 \) jots

\( SNR \leq \sqrt{256} \)
Convolution

2D Examples:

Binary valued filter

Binary-weighted filter

-26-
Synthetic input image

After DFS development

Plus filter with dynamic kernel size

Digital Film Sensor Algorithm

Threshold
e.g. 3 hits
in 4x4

“gain”
Readout of Jot Signal to Digital Circuits
Readout Signal Chain
Strawman Design

General requirements:
• Need to scan 0.1-10 Gjots at 100-1000 fields per sec
• 8k – 80k jots per column → 0.8 – 80M jots/sec

Assumptions:
• 0.1 Gjot at 100 fps → 1Mjot/sec
• 1 mV/e- conversion gain
• 150 uV rms noise on column bus (0.15 e- rms)
• 0.18 um process
• Vdd = 1.8V
Readout Signal Chain

<table>
<thead>
<tr>
<th>Process</th>
<th>$V_{DD}$</th>
<th>Jot array</th>
<th>Column Speed</th>
<th>Column power</th>
<th>Comp power</th>
<th>Total</th>
<th>Array Power</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CURRENT DESIGN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.18um</td>
<td>1.8V</td>
<td>0.001 Gjots</td>
<td>1MJ/s</td>
<td>0.71uW</td>
<td>1.28uW</td>
<td>1.99uW</td>
<td>1.99mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(1k X 1k)</td>
<td>(1000fps)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.18um</td>
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<td>1MJ/s</td>
<td>6.44uW</td>
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<td>77.2mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(10k X 10k)</td>
<td>(100fps)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SCALED DESIGN</strong></td>
<td></td>
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</tr>
<tr>
<td>45nm</td>
<td>1.1V</td>
<td>1 Gjots</td>
<td>24MJ/s</td>
<td>57uW</td>
<td>2.9uW</td>
<td>59.9uW</td>
<td>2.5W</td>
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<tr>
<td></td>
<td></td>
<td>(24k X 42k)</td>
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<tr>
<td>22nm</td>
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<td></td>
<td></td>
<td>(75k X 133k)</td>
<td>(1000fps)</td>
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<tr>
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<td>75MJ/s</td>
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<td>2.3uW</td>
<td>199.3uW</td>
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Adapted from Kotani et al. 1998
## Readout Signal Chain

Adapted from Kotani et al. 1998

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1000fps 1 Mjot binary pixel image sensor

<table>
<thead>
<tr>
<th>Process</th>
<th>XFAB-XC018, 0.18um, 6M1P</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1.8V (Analog), 3.3V (Array)</td>
</tr>
<tr>
<td>Pixel type</td>
<td>3T-APS</td>
</tr>
<tr>
<td>Pixel pitch</td>
<td>3.6um</td>
</tr>
<tr>
<td>Photo-detector</td>
<td>Photodiode</td>
</tr>
<tr>
<td>Conversion gain</td>
<td>200uV/e-</td>
</tr>
<tr>
<td>Array</td>
<td>1376(H) X 768(V) (WXGA 16:9 ratio)</td>
</tr>
<tr>
<td>Frame rate</td>
<td>1000fps</td>
</tr>
<tr>
<td>Column noise</td>
<td>&lt; 150uV</td>
</tr>
<tr>
<td>ADC sampling rate</td>
<td>768KSa/s</td>
</tr>
<tr>
<td>ADC input referred offset</td>
<td>&lt;500uV</td>
</tr>
<tr>
<td>Output data rate</td>
<td>32 (output pins) X 33 Mb/s</td>
</tr>
<tr>
<td>Power (Binary imager)</td>
<td></td>
</tr>
<tr>
<td>Array</td>
<td>2.3mW</td>
</tr>
<tr>
<td>ADCs</td>
<td>2.5mW</td>
</tr>
<tr>
<td>Digital</td>
<td>5mW</td>
</tr>
<tr>
<td>Total</td>
<td>9.8mW</td>
</tr>
<tr>
<td>I/O pad power</td>
<td>50mW</td>
</tr>
</tbody>
</table>

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1000fps 1 Mjot binary pixel image sensor
1000fps 1 Mjot binary pixel image sensor

Chips are just back and packaged but untested
65nm pathfinder for 1 Giga jot at 1000fps

- 1Gjot imager has a 24,000 X 42,000 pixel array
- Limited space for Dartmouth on multi-project chip on multiproject wafer so only 32 columns
- There are 24,000 pixels in each column.
- Power consumption per column is multiplied by 42,000 to get the power consumption of a 1Gjot imager.
### 65nm Pathfinder for 1 Giga Jot at 1000fps

<table>
<thead>
<tr>
<th>Process</th>
<th>65nm, 1P5M</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1.2V (Analog), 2.5V (Array)</td>
</tr>
<tr>
<td>Pixel type</td>
<td>4-shared PPD, 1.75T/pixel</td>
</tr>
<tr>
<td>Pixel pitch</td>
<td>1.4um</td>
</tr>
<tr>
<td>Array</td>
<td>32(H) X 24000(V)</td>
</tr>
<tr>
<td>Frame rate</td>
<td>1000fps</td>
</tr>
<tr>
<td>Column noise</td>
<td>&lt; 150uV</td>
</tr>
<tr>
<td>ADC sampling rate</td>
<td>24MSa/s</td>
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<td>&lt;500uV</td>
</tr>
<tr>
<td>Output data rate</td>
<td>32 (output pins) X 24 Mb/s</td>
</tr>
</tbody>
</table>

#### Estimated Power (Binary imager)

<table>
<thead>
<tr>
<th></th>
<th>One column</th>
<th>1Gjot (42K column)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array</td>
<td>50uW</td>
<td>2.1W</td>
</tr>
<tr>
<td>ADC</td>
<td>15uW</td>
<td>0.63W</td>
</tr>
</tbody>
</table>

Design in progress, tapeout end of June

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Single Bit v. Multi-bit

**Single Bit**
- Each jot produces 1 bit
- 1 bit ADC
- For same flux of photoelectrons, need higher frame rate readout
- Conceptual simplicity
- Easier on chip digital electronics

**Multi-bit**
- Each jot produces n bits
- n-bit ADC
- For same flux of photoelectrons, lower relative frame rate $1/2^{(n-1)}$
- Like current CMOS APS but low FW capacity and high conversion gain (quantized digital integration sensor qDIS*)

Single Bit v. Multi-bit Power Comparison

Average power consumption (μW)

Number of bits

Power-area product

Number of bits
Jot Device Considerations

General requirements:
- 200 nm device in 22 nm process node (“10L”)
- High conversion gain > 1 mV/e- (per photoelectron)
- Small storage well capacity ~1-100 e-
- Complete reset for low noise
- Low active pixel transistor noise <150 uV rms
- Low dark current ~ 1 e-/s
- Not too difficult to fabricate in CIS line

For early investigation
- Cobbled together an imaginary 85 nm process
- Students learned to use TCAD tools etc.
- Anticipated that device principles can be migrated to real process
• CMOS APS but use pinning layer as emitter, storage well as base
• Complete reset of base using “TG”
• Emitter follower to reduce base-emitter cap
Storage under transfer gate first proposed in
Back Illuminated Vertically Pinned Photodiode with in Depth Charge Storage, by J. Michelot, et al., 2011 IISW

- Low capacity storage gate makes barrier easier to overcome with low TG voltage
- Minimum FD size to increase conversion gain
Pump-gate Jot Device To Increase Conversion Gain

- 65 nm Node
- 1.4 um pitch
- 3.3 V operation
- 200 e⁻ FW
- >300 uV/e⁻

Test array tapeout June 2014
SPAD Implementation of QIS
At Univ. Edinburgh
320x240 SPAD-based QIS

- Dutton et al. *IEEE VLSI Symposium* 2014
- University of Edinburgh & ST Microelectronics
- 8µm SPAD-based Pixel with 26.8% FF
320x240 SPAD-based QIS

Dutton et al. *IEEE VLSI Symposium* 2014

5k FPS Binary Frames

Comparator Threshold

20 FPS 8b DR (256 frames summed)
Summary

- Good progress in understanding response v. exposure, SNR, DR, etc. using photon statistics
- Early progress made on realizing Quanta Image Sensor
- >2 years support of Rambus (thanks Rambus!)
- Students up to speed and making great headway
- Challenges don’t look as challenging
- Lots of work still to do!