2nd Generation Cameras for LCLS and the New Challenges of High Repetition Rates at LCLS-II

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Outline

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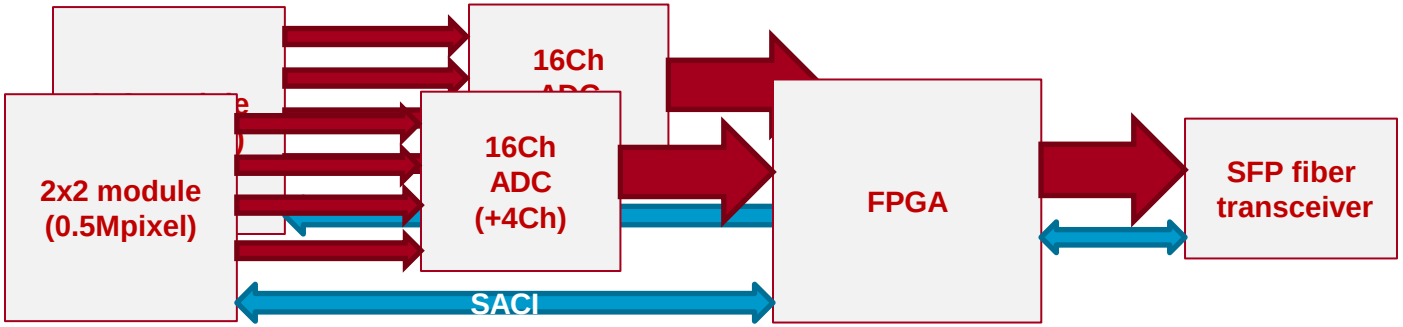
2nd generation cameras for LCLS:

- ePIX camera concept
- the ePIX ONE camera
  - design, features, capabilities
  - ePIX ONE camera results with ePIX-100p
- next steps
  - ePIX FOUR camera and bigger …

New Challenges of High Repetition Rates at LCLS-II :

- Frontend, backend, DAQ – blurring the lines
- ROI, triggering and read during capture support
- The binning photon counter pixel architecture
- Parallelization, pipelining, Superpixels

ePIX camera electronics - concept

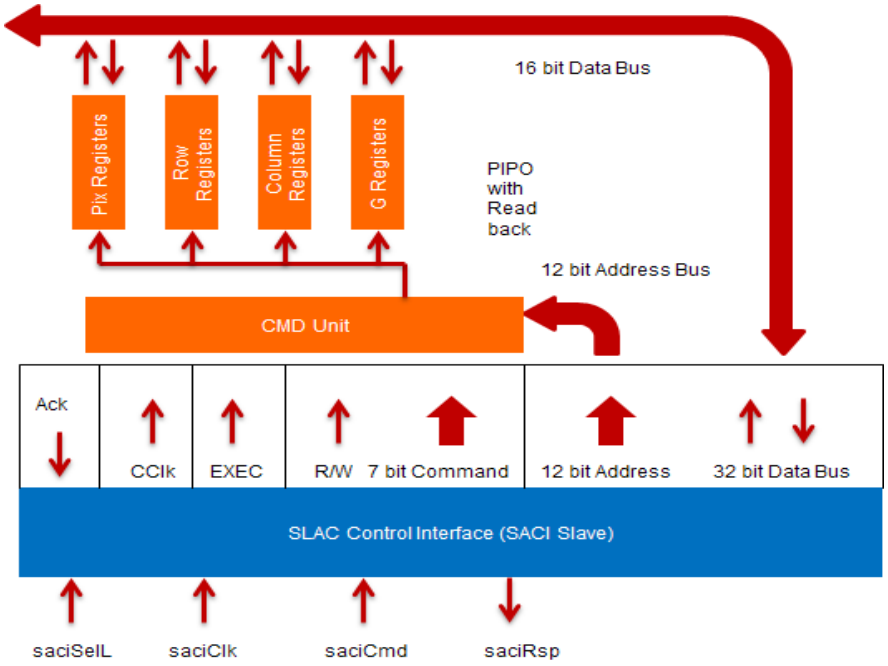


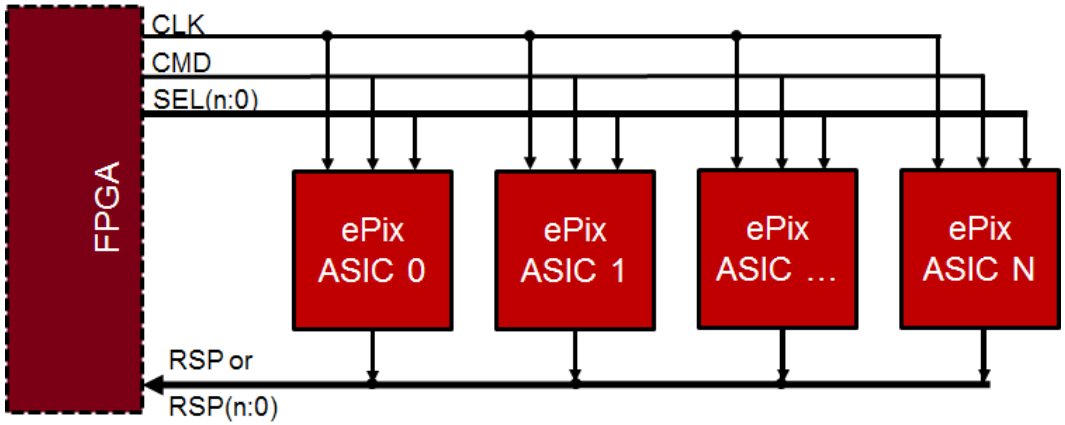
- **ASIC tests, detector tests and science camera will use same hardware and similar software components**

- camera electronics and DAQ system development based on proven CSPAD components (improved next generation)

- PCB level A/D converters sample the analog multiplexed data from the front end ASICs
- supports 2x2 ASIC arrangement with 0.5M-pixel and >120Hz frame rate
- needs only 3 power supplies: digital, analog, high voltage bias
- fully digital interface: data over a fiber link (SLAC PGP based)
- supports dedicated abstract slow control interface for housekeeping / telemetry (via virtual channels on PGP link, for EPICS controls)
- unique serial numbers for DAQ configuration, calibration and data management
- compatible with ePIX100p, ePIX100a, ePIX10kp, ePIX10ka …

SACI ASIC slow control interface

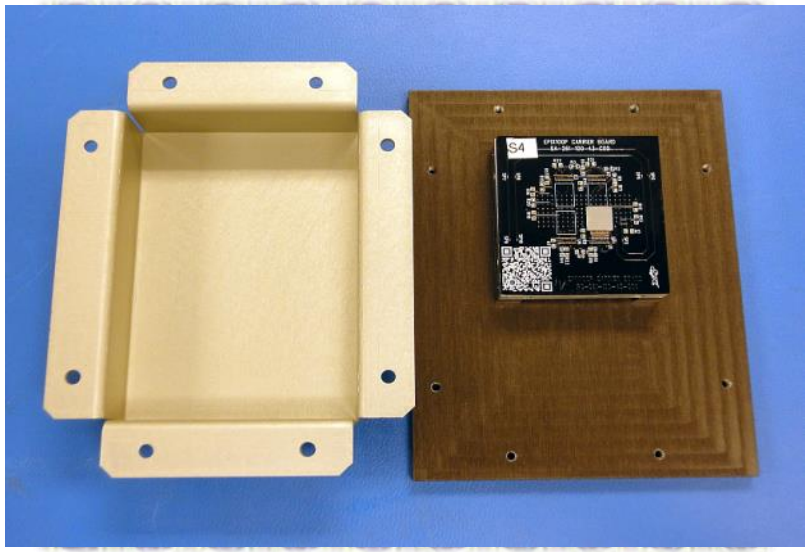


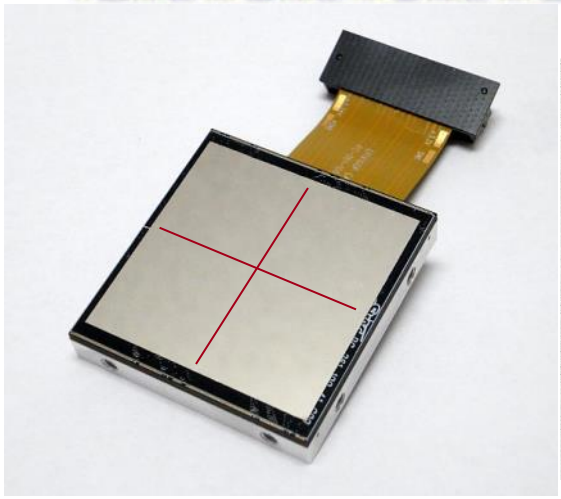


- Master/Slave Serial Interface with 4 signals
  - 3 can be bused:
    - saciClk
    - saciCmd
    - saciRsp
  - 1 dedicated select line per slave:
    - saciSelL
    - (sacRsp)

- Allows multiple slaves on same SACI bus. (Similar to SPI)
- Serial data transmitted on rising edge of clock and sampled on falling edge. MSB first.
- Toggling saciSelL resets slave state machine in case of lockup.
- No errors seen in over 10^7 transactions at 62.5 MHz saciClk.

ePIX hybrid pixel detector carriers



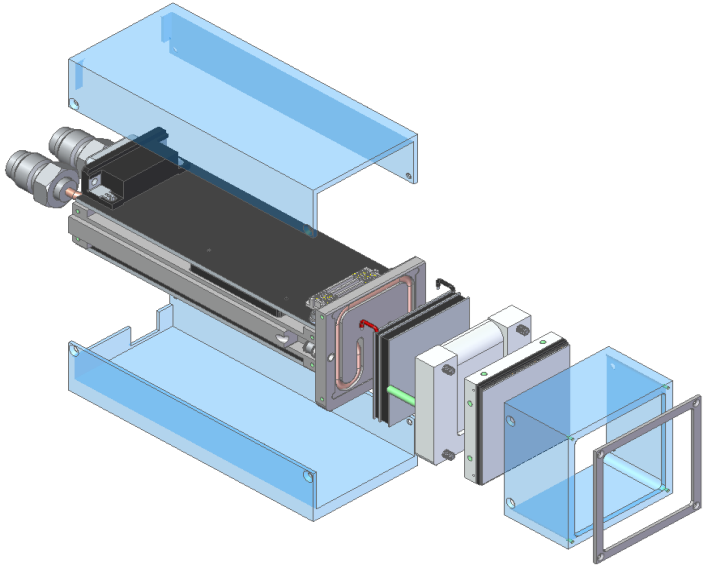


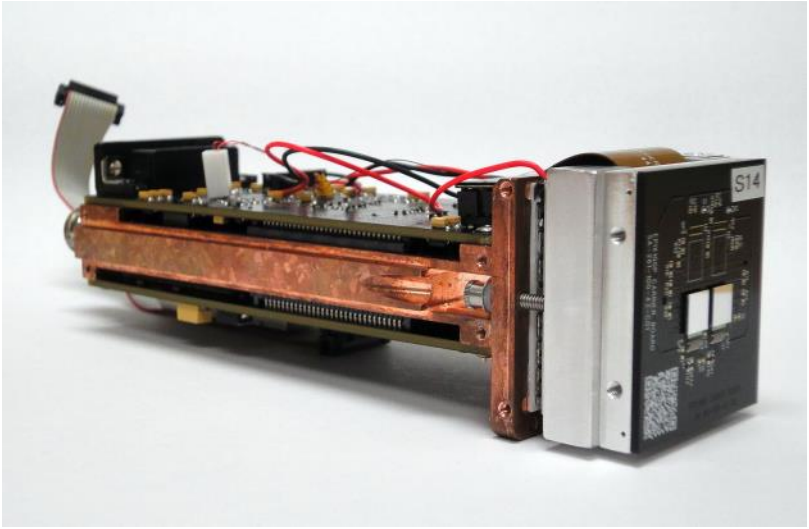
- same form factor as new 2x2 CSPAD carriers
- -> can use same tools, boxes and assembly and handling procedures

- 2x2 ASIC carrier
  - supports monolithic 2x2 sensor
  - or two 2x1 sensors
  - 768 x 704 pixels
    -> **0.5M-pixel** for ePIX100a
  - SACI of all 4 ASICs is bussed
- one backside connector
  - 160 pins
  - 2 A rated per pin
  - 10 GHz differential bandwidth
  - not too small / fragile

- flex between front- and backend electronics
- low noise performance demands better cooling capability than CSPAD

ePIX ONE camera - concept



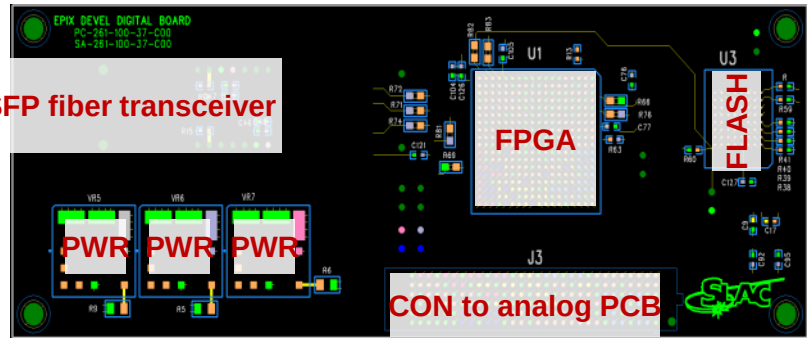


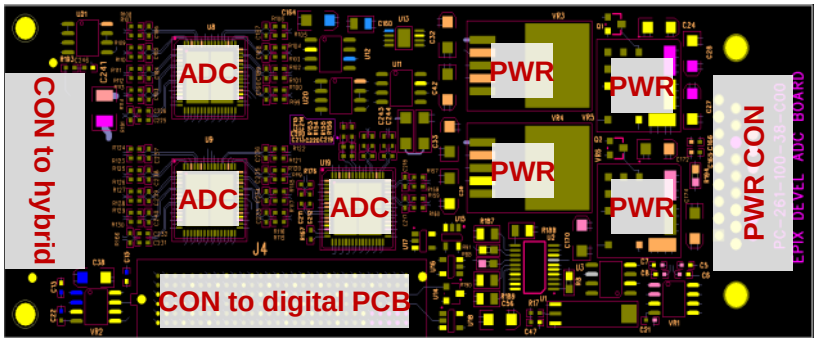
- Compact
- easy to use
- vacuum compatible design
- DSUB-26 power connector
- fiber pair for data & communication
- water cooling

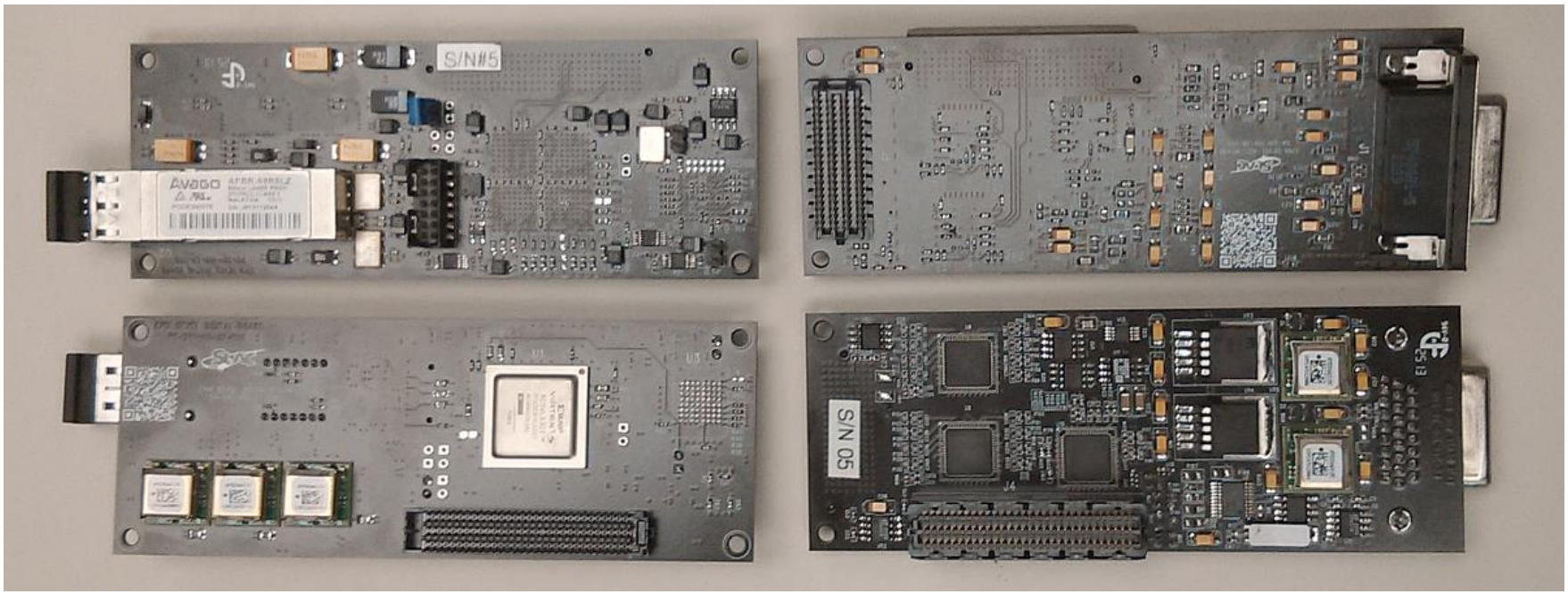
- water cooled baseplate between analog and digital PCB
- high power PCB components cooled by baseplate

- TEC cooling for detector assembly
- detector hoody can be N2 purged

ePIX ONE camera - PCBs

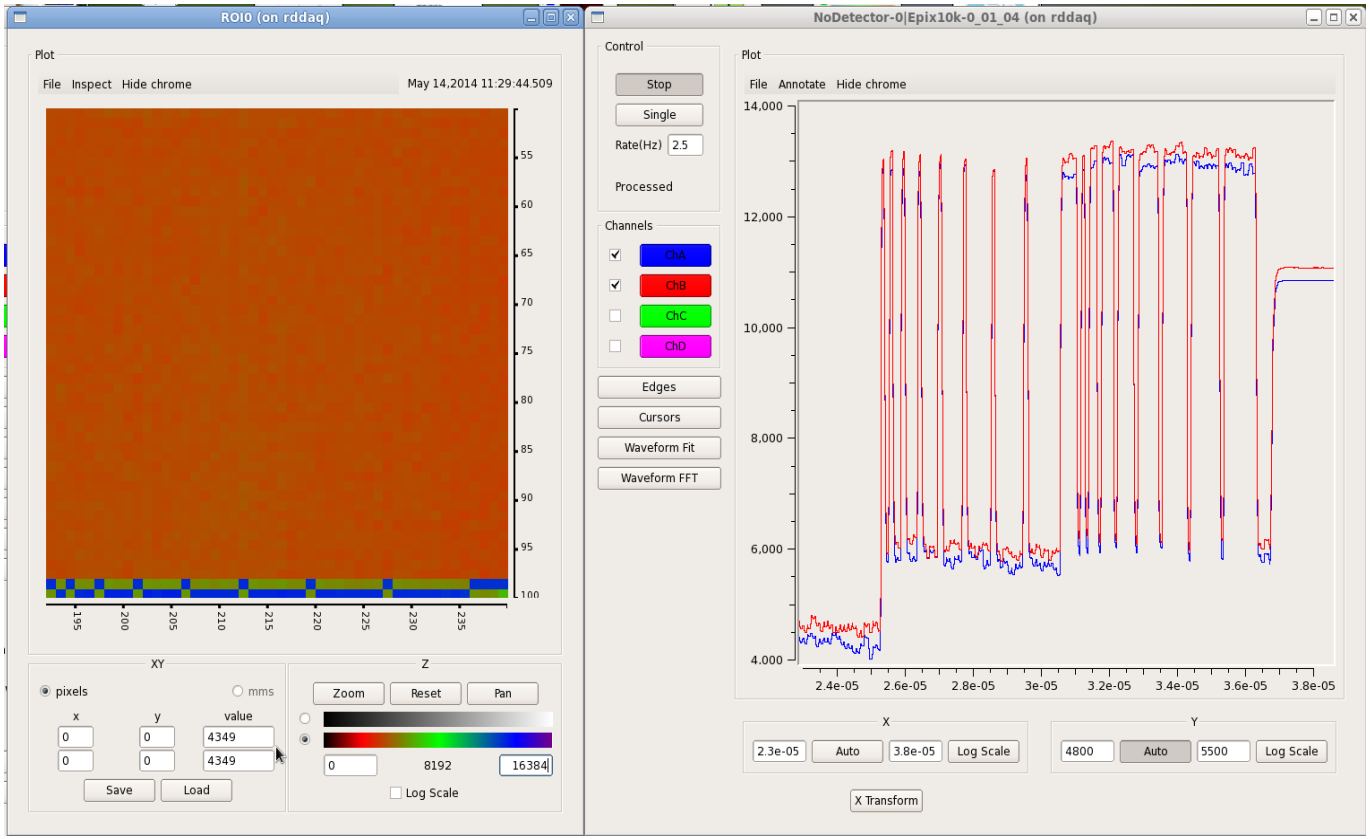






ePIX ONE camera - housing
for ePIX10k (135kpixel) and ePIX100 (0.5Mpixel)

ePIX camera features - scope mode



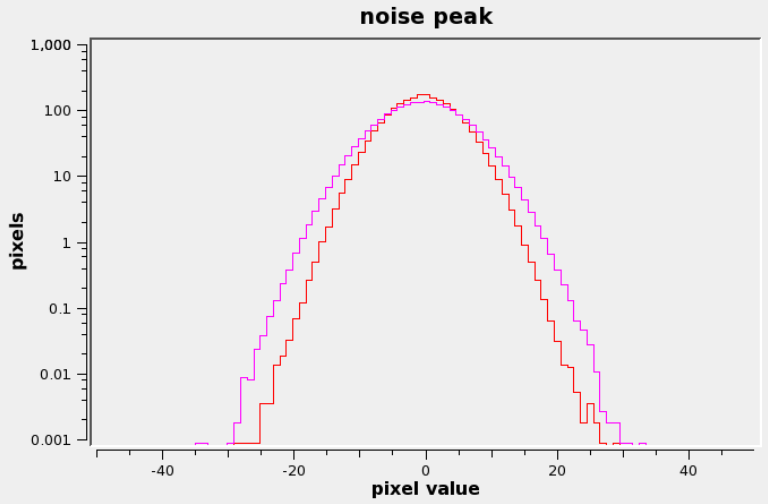
- ePIX ASICs include 2 extra lines which can be set to high or low level per pixel

used to monitor:

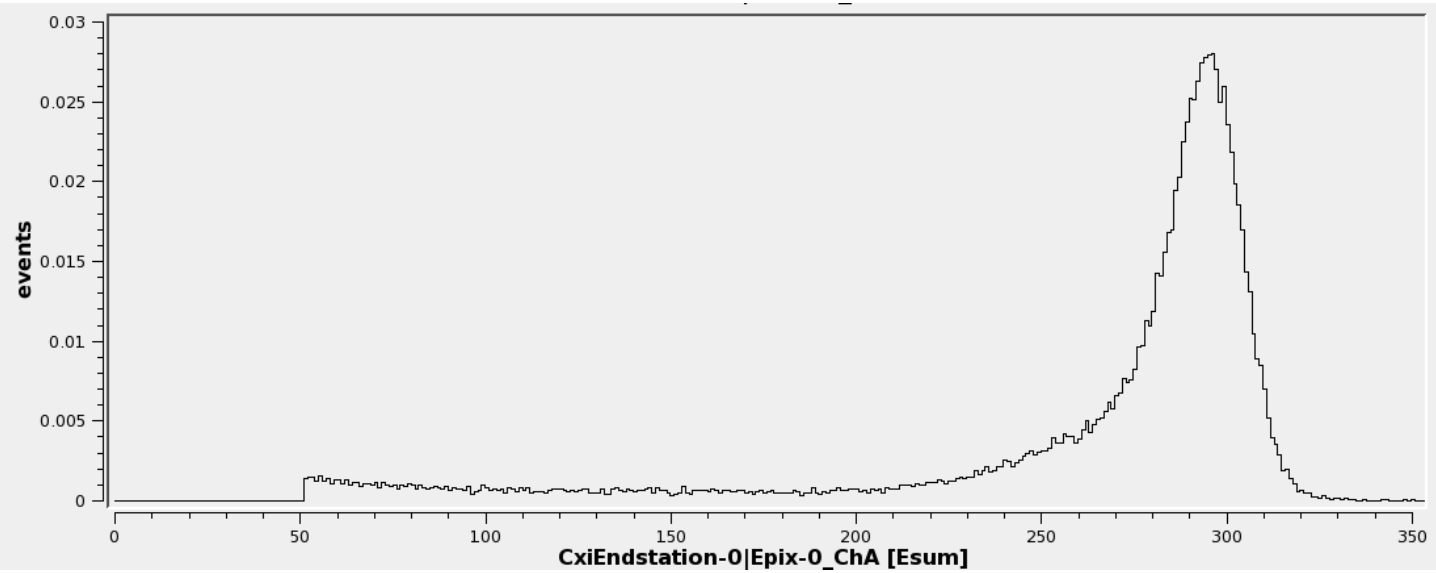
- baseline and gain drift
- multiplexer timing and readjust ADC sampling

ePIX camera features - scope mode zoom

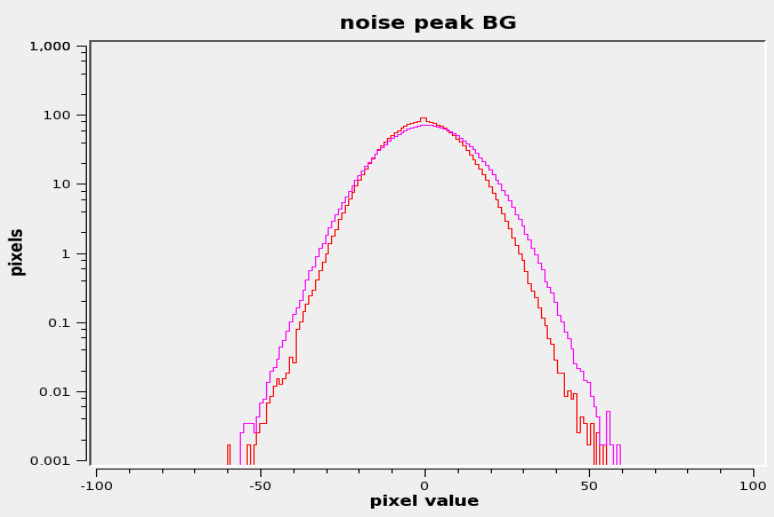
ePIX-100p noise peak performance



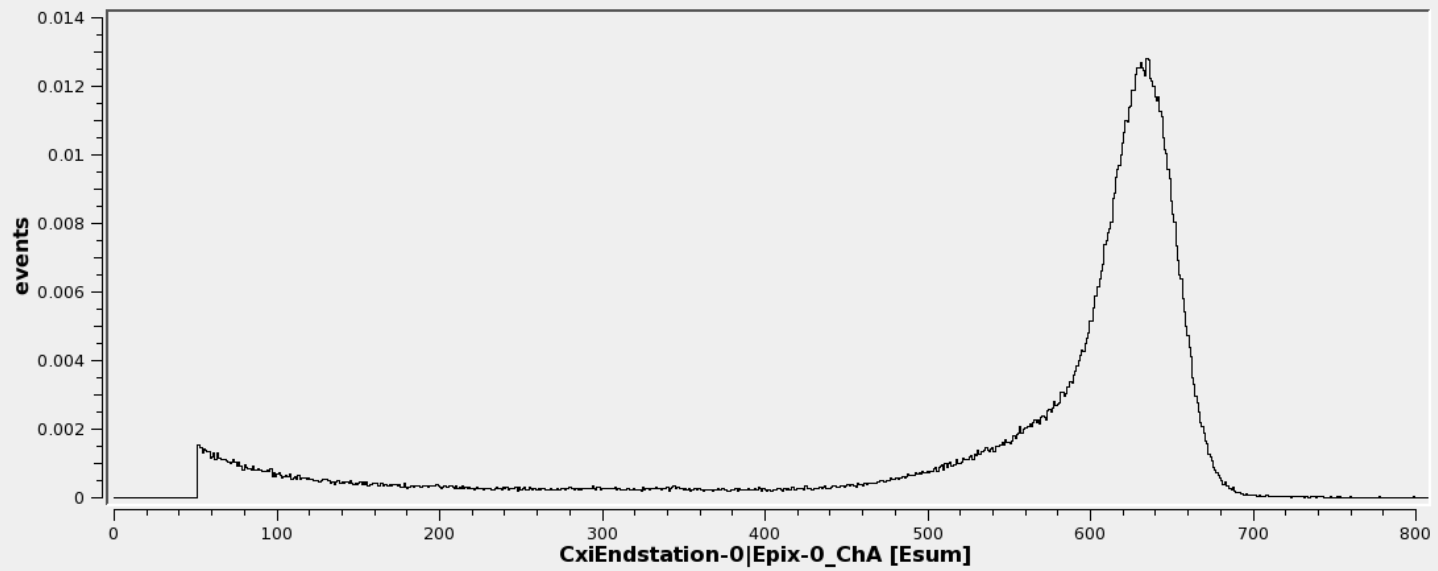
- T= ca -8 C
- Tint = 260us
- gain for Mo (17.44keV) singles at 295 ADU
  - 16.2 electrons / ADU
- noise without LCN correction at 5.20 ADU
  - 84 electrons RMS
- noise with LCN correction at 4.75 ADU
  - 77 electrons RMS



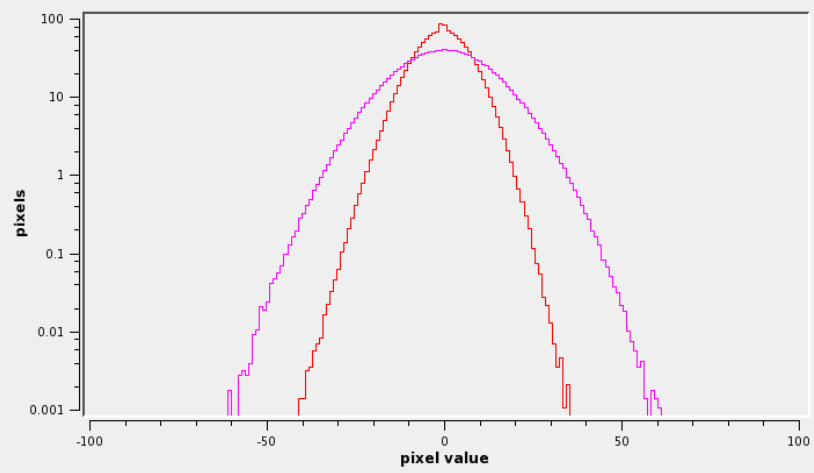
ePIX-100p noise peak performance in boosted gain operation



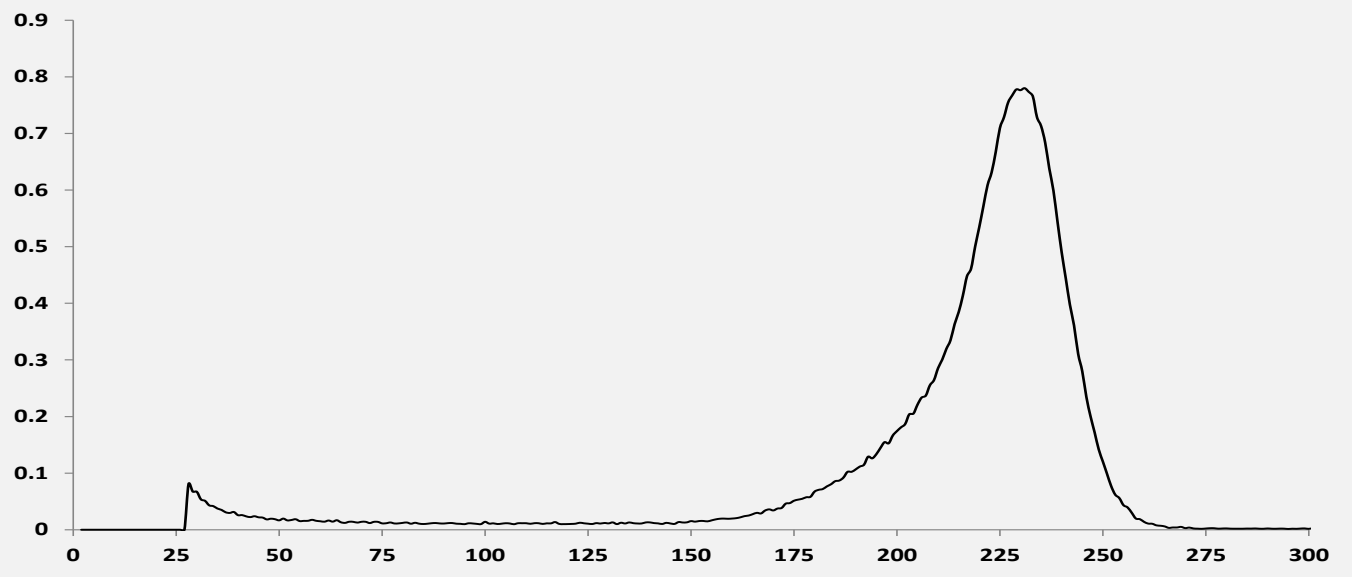
- T= ca -8 C
- Tint = 260us
- gain for Mo (17.44keV) singles at 635ADU
  - 7.52 electrons / ADU
- noise without LCN correction at 10.35 ADU
  - 78 electrons RMS
- noise with LCN correction at 9.85 ADU
  - 74 electrons RMS



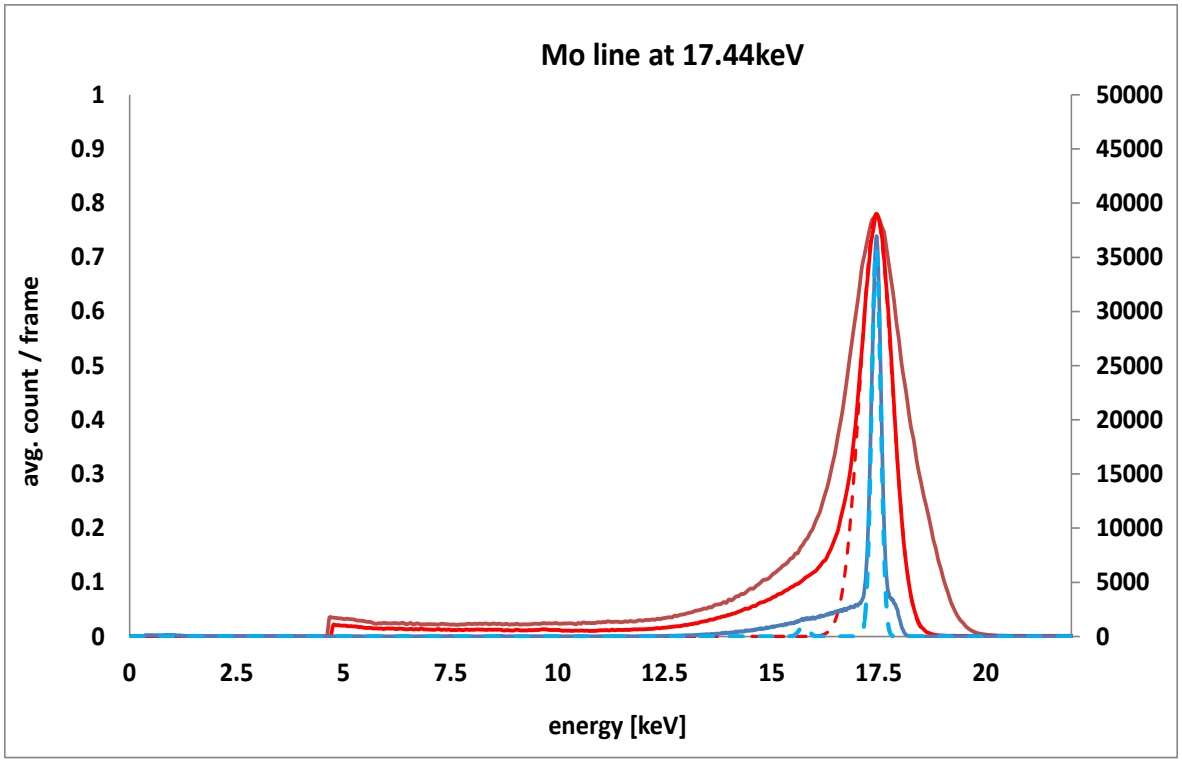
ePIX-10kp noise peak performance



- T= ca -8 C
- Tint = 300us
- gain for Mo (17.44keV) singles at 225 ADU
  - 21.2 electrons / ADU
- noise without LCN correction at 12.4 ADU
  - 263 electrons RMS
- noise with LCN correction at 6.8 ADU
  - 144 electrons RMS



ePIX-100p Mo line performance



- T= ca -8 C
- Tint = 260us
- X-ray tube with Mo target

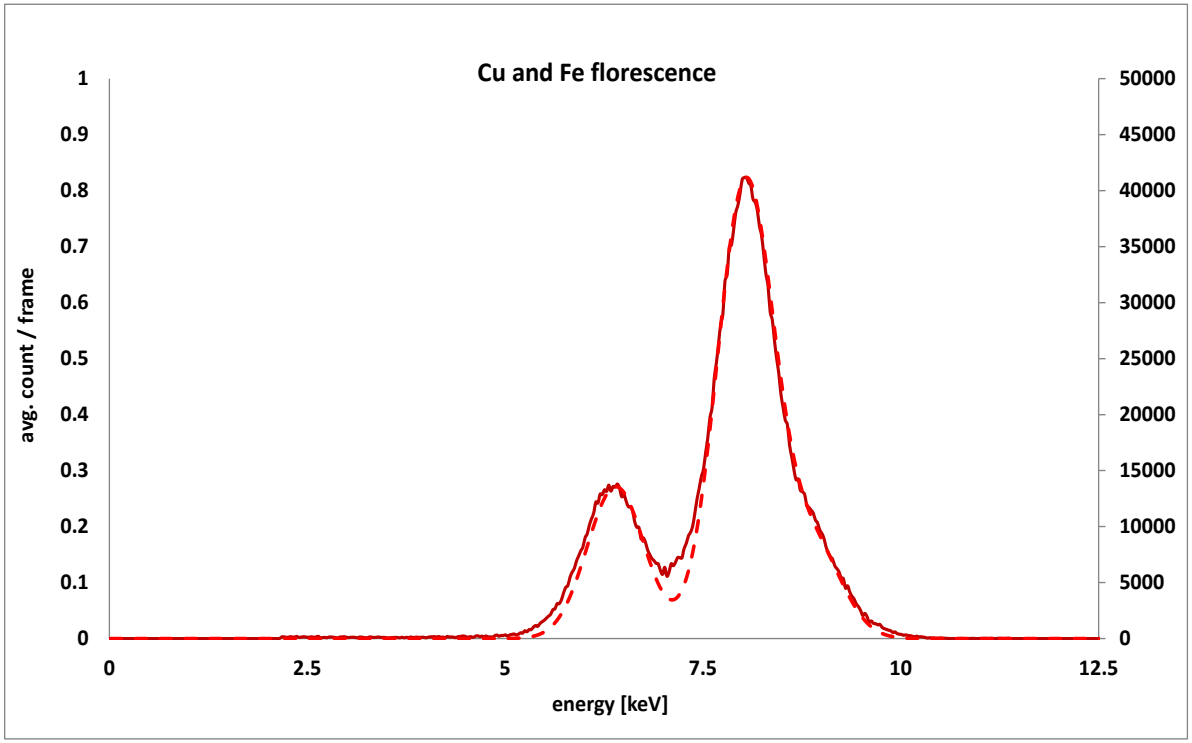
- SDD (blue) line width
  250eV @ 17.44keV

ePIX 100a single pixel hits (red) :

- ePIX100 without gain correction
  - 1.75 keV FWHM
    -> 204 e- ENC

- ePIX100 with gain correction
  - 0.88 keV FWHM
    -> 102 e- ENC

ePIX-100p Cu and Fe line



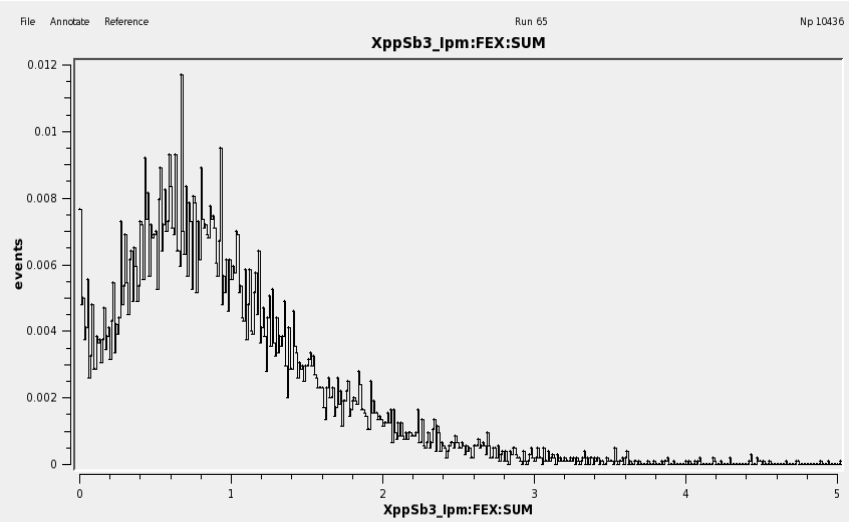
- T= ca -8 C
- Tint = 260us
- Measured at LCLS

- Cu target and Fe foil
  (Ka: 8.0keV and 6.4keV)

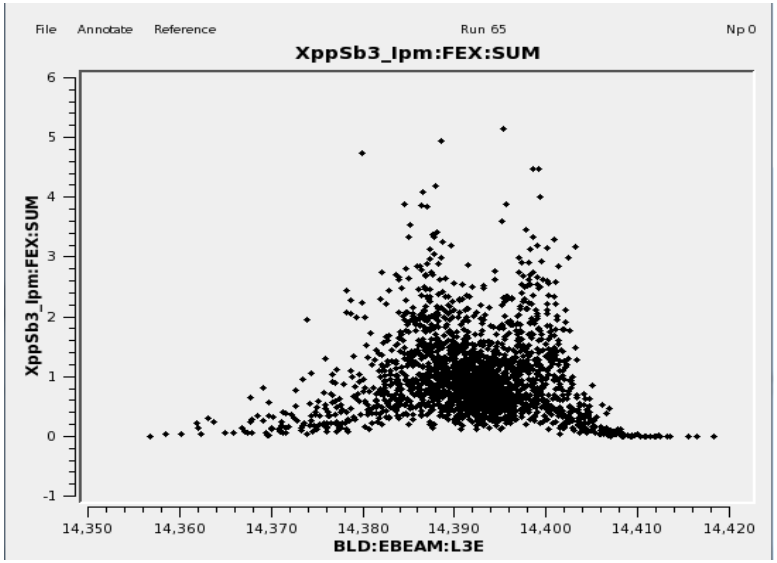
- single pixel hits, gain corrected:
  0.85keV FWHM
  -> 99 e- ENC

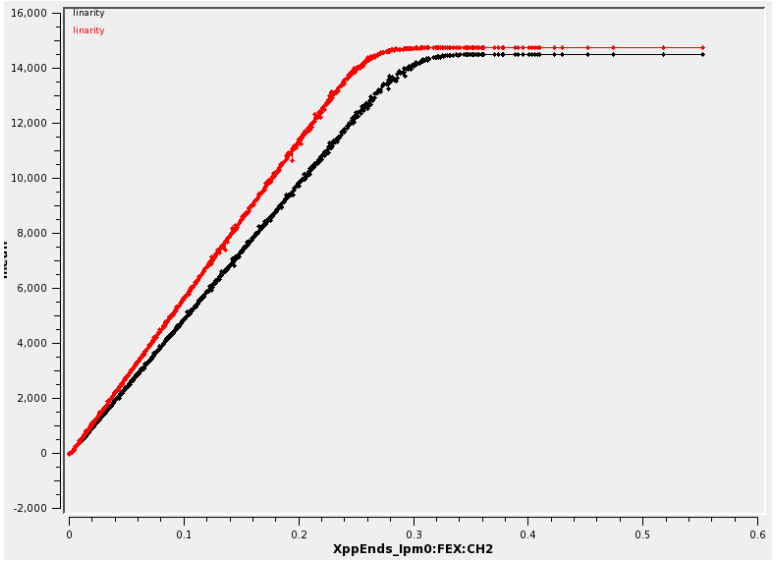
- 50um pixels
  and low noise performance
  -> allows sub-pixel resolution

ePIX-100p linearity @LCLS

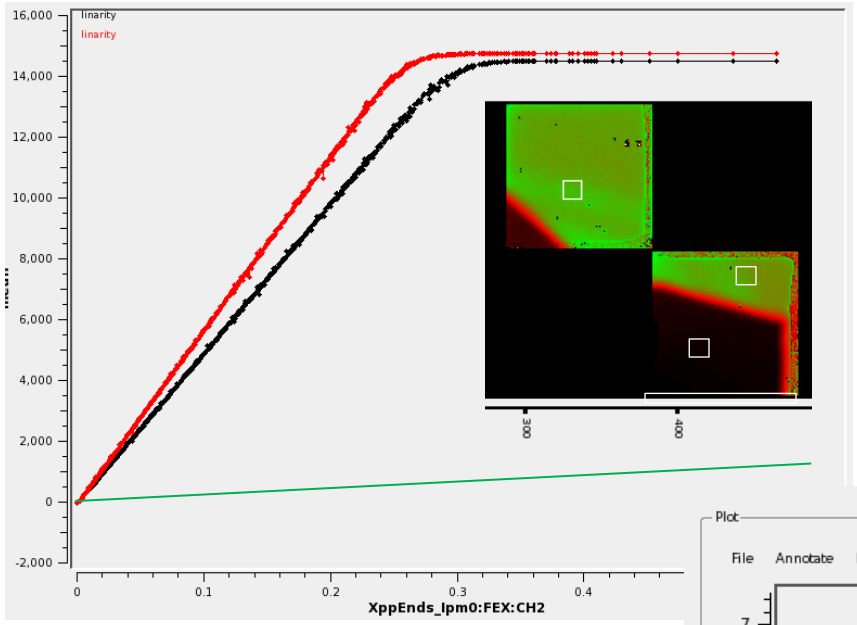


- large intensity fluctuations from shot to shot
- detector signal has to be correlated with beam data or second detector
- linearity of secondary detector not guaranteed (i.e. beam intensity monitor upstream of a beamline slit will report different intensity than intensity at the sample due to small variations in beam profile and pointing)

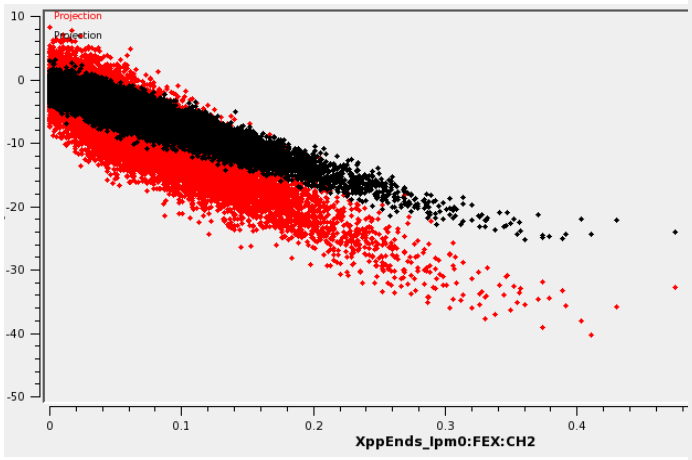


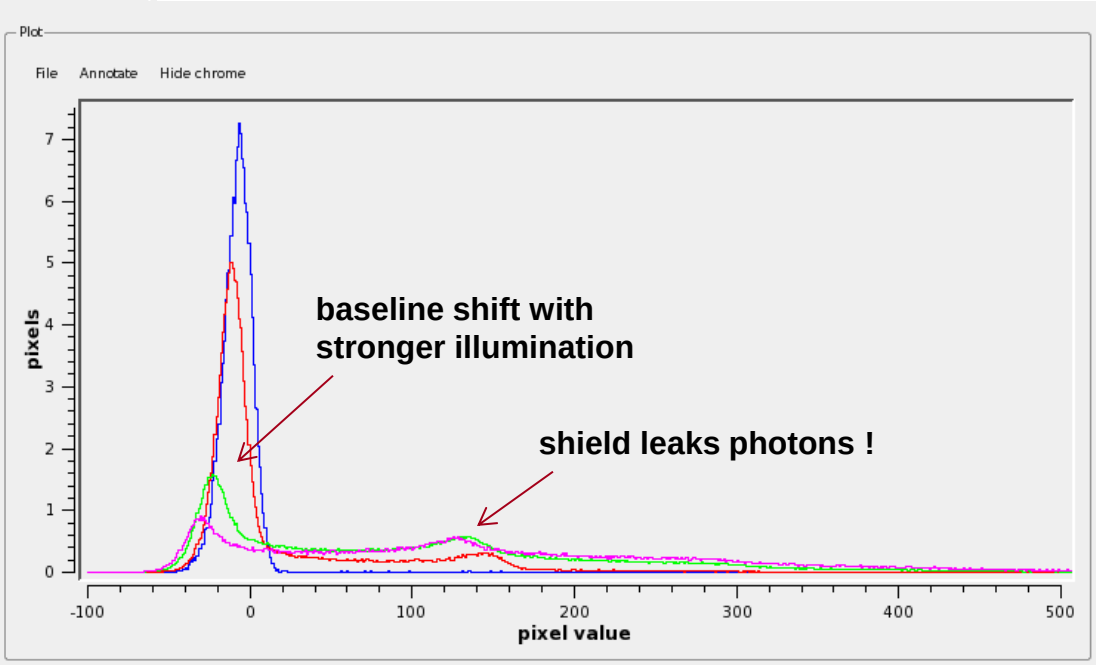


ePIX100p linearity @LCLS - x-talk

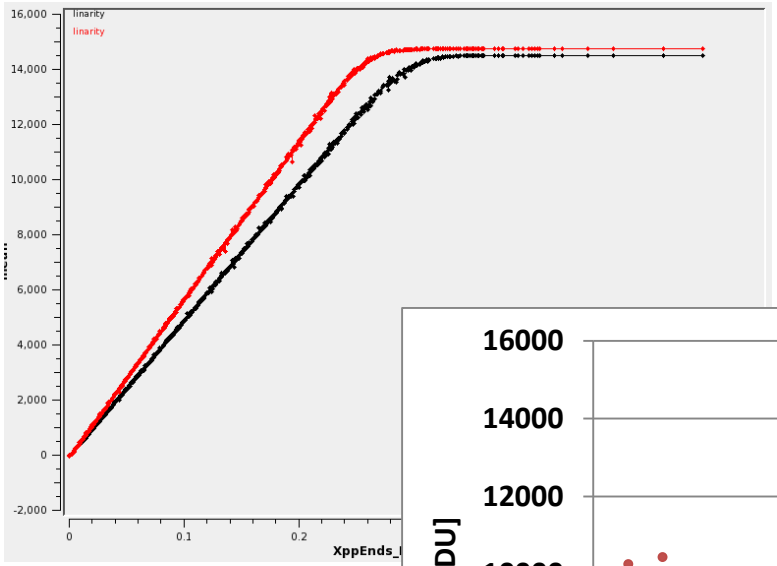


- T= ca -8 C
- Tint = 260us
- measured at LCLS (9180eV)
- 1 photon -> ca 150 ADU
- good linearity up to 12000ADU





ePIX-100p linearity @LCLS - results



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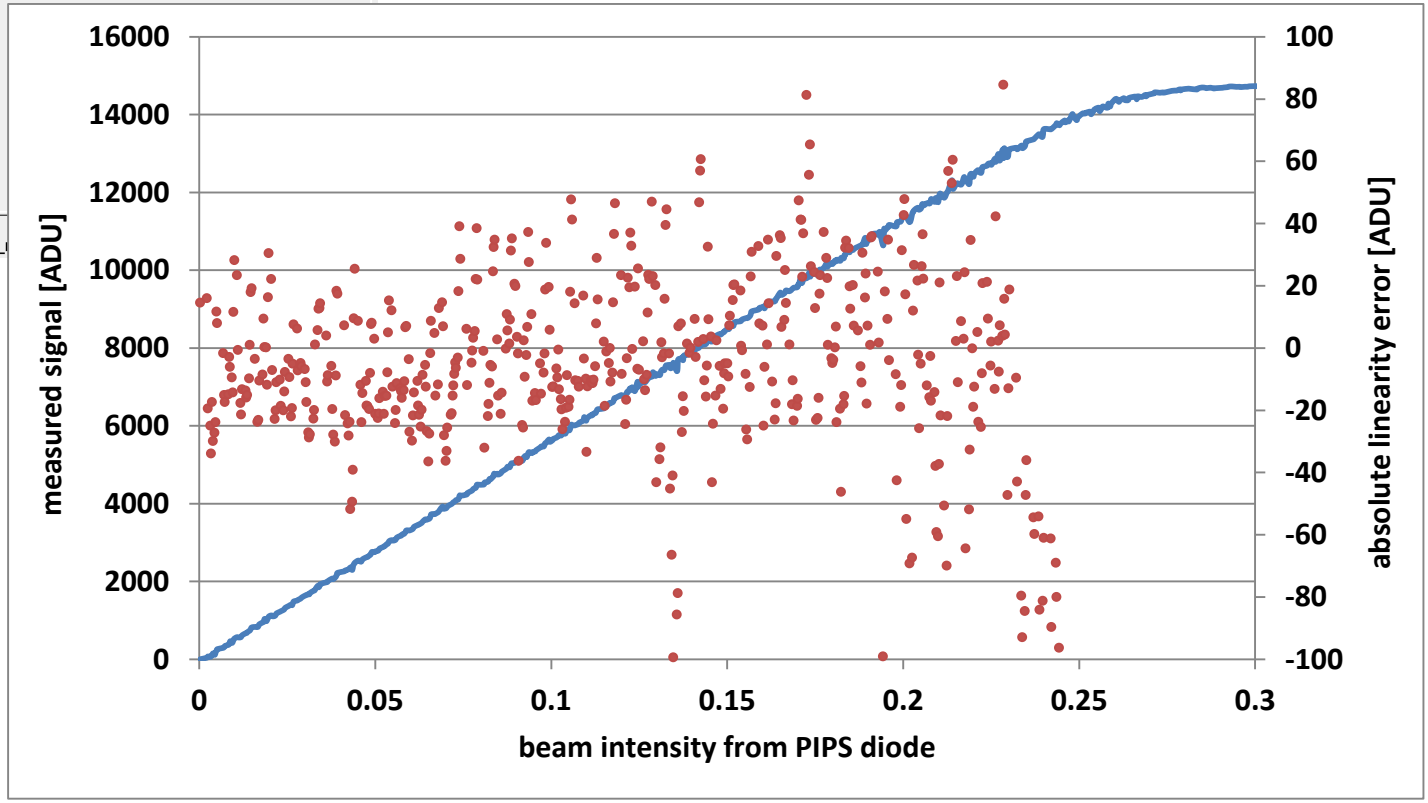
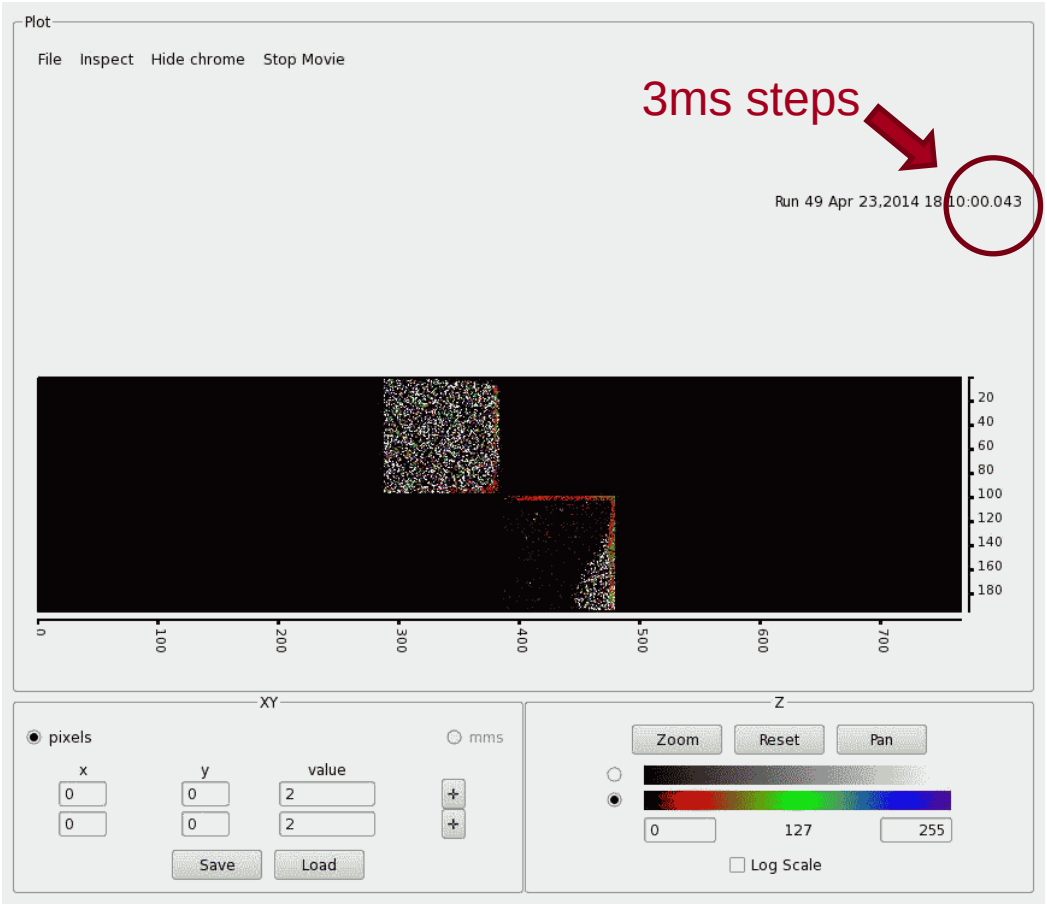
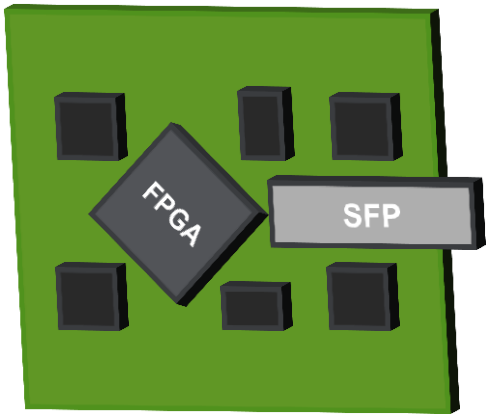
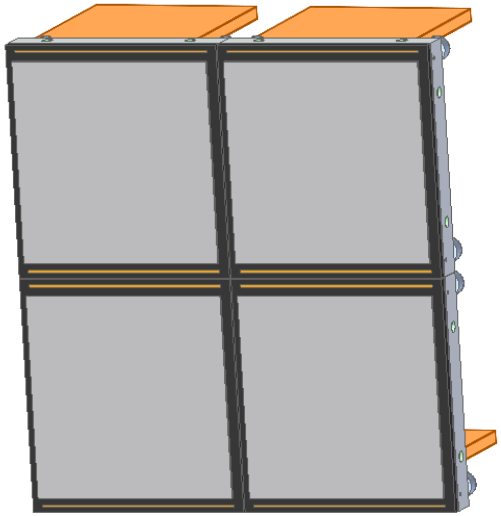


ePIX ONE camera with ePIX-100p ROI @ 360 FPS



Next steps –
ePIX ONE deployment & ePIX FOUR camera





ePIX10k module: 135k-pixel

ePIX100 module: 540k-pixel

Future ePIX cameras – 2 to 20Mpixel for protein crystallography and imaging

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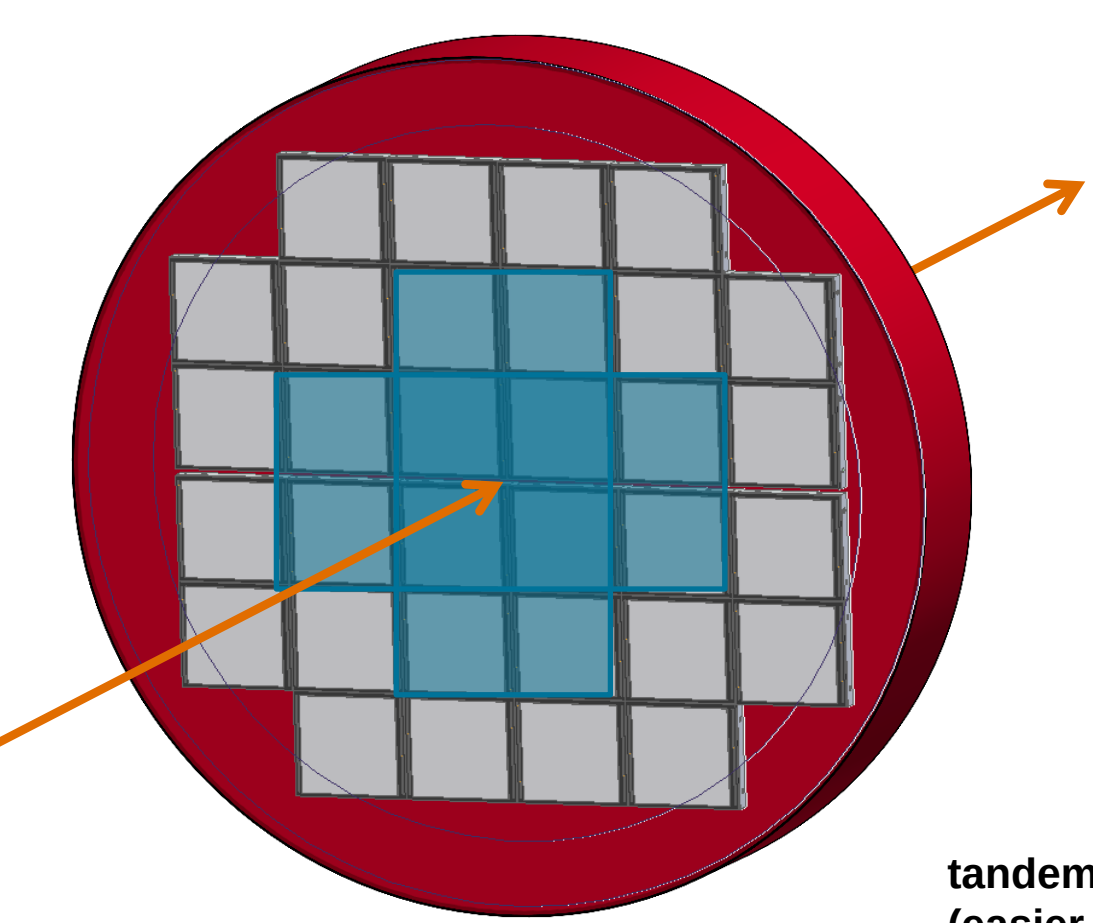

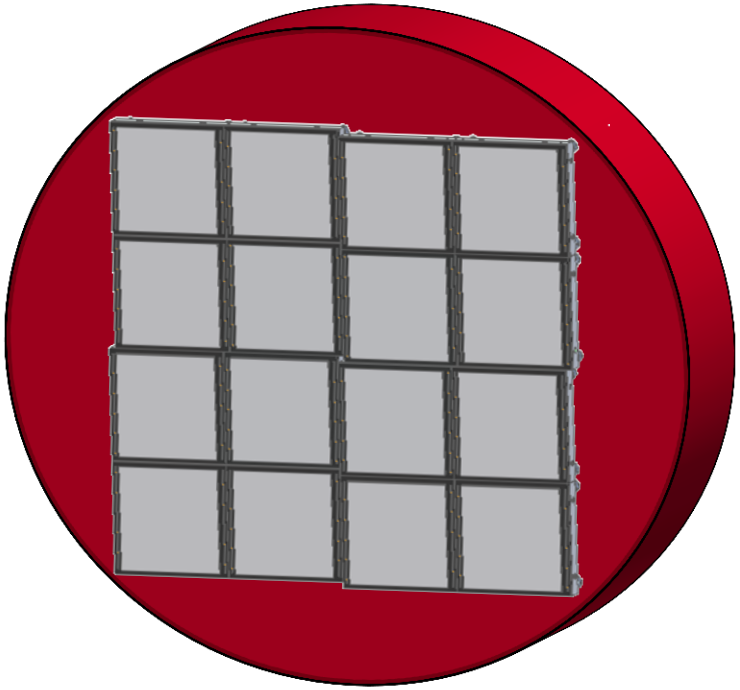

ePIX10k module: 135k-pixel

ePIX100 module: 540k-pixel

tandem operation on single optical bench (easier alignment and metrology)

- **back detector for low q signal**
- **front detector for high q signal**

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- ROI, triggering and read during capture support
- The binning photon counter pixel architecture
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FEL Science with LCLS-II New Capabilities

High repetition rate; 0.2-5 keV

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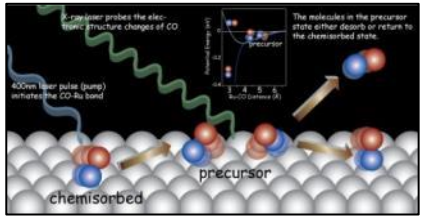
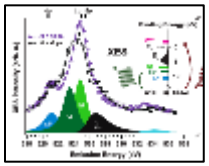
High repetition rate lower peak power science: 0.2-5keV

Catalysis (CO on Ru)

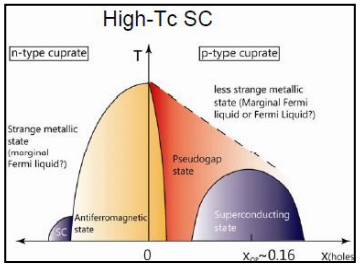


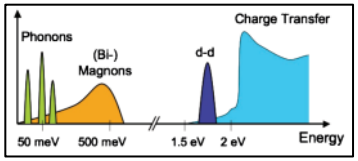


C K edge
0.284 keV

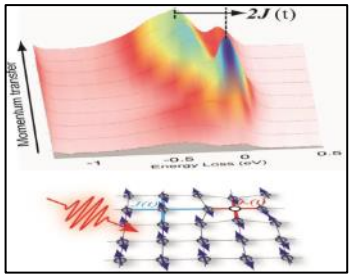
Cu L_{III} edge
0.932 keV

High T_C Superconductors





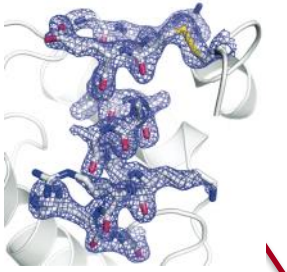
Correlated Electron Systems



Time resolved RIXS

Ru L_{III} edge
2.838 keV

de novo phasing using
Single Wavelength Anomalous Diffraction
from Sulfur: 4-5 keV

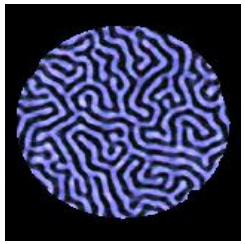


0.2 keV

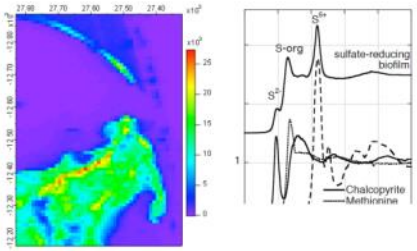
Gd M_V edge
1.190 keV

S K edge
2.472 keV

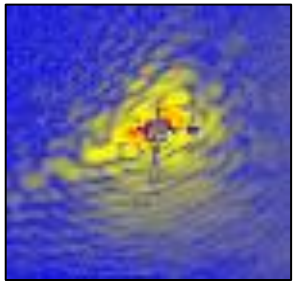
5.0 keV



Coherent X-ray Imaging of magnetic domain in Gd/Fe



Sulfur spectro-microscopy in bio/environmental science



Non-periodic imaging: 2-5 keV

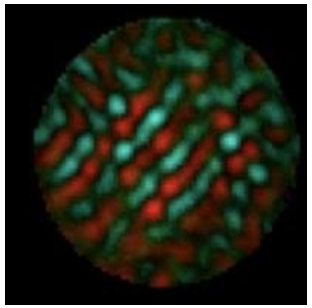
FEL Science with LCLS-II New Capabilities

High pulse energy 5-25 keV

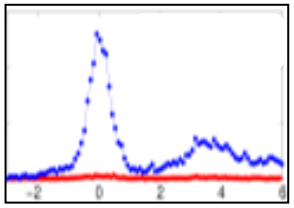
SLAC

High energy per pulse science 5.0-20.0 keV

Magnetic polarities of a cobalt alloy

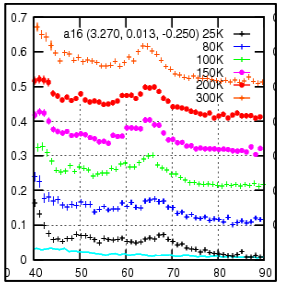


Iridates: model strongly correlated materials

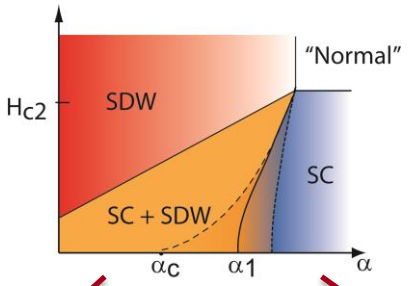


Energy Loss (eV)

Phonons in superconductivity



High magnetic fields 14-20 KeV disentangle competing orders



Fe K edge 7.112 keV

Co K edge 7.712 keV

Ir L_{III} edge 11.215 keV

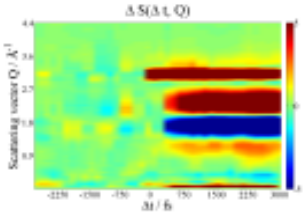
Si(777) backscatter 13.84 keV

Se K edge 12.658 keV

5 keV

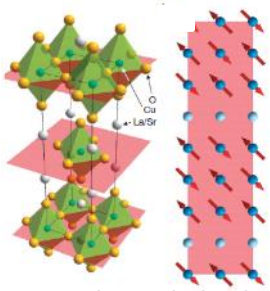
25 keV

Solute-solvent interactions in photo-excited reactions

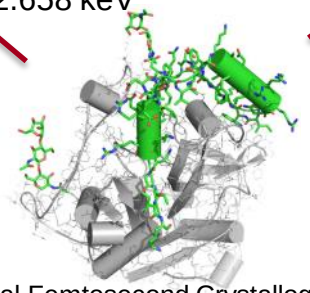


Time resolved Resonant solution scattering

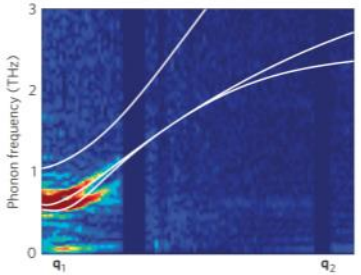
Cu K edge 8.979 keV



Charge-stripe ordering in LSCO superconductor

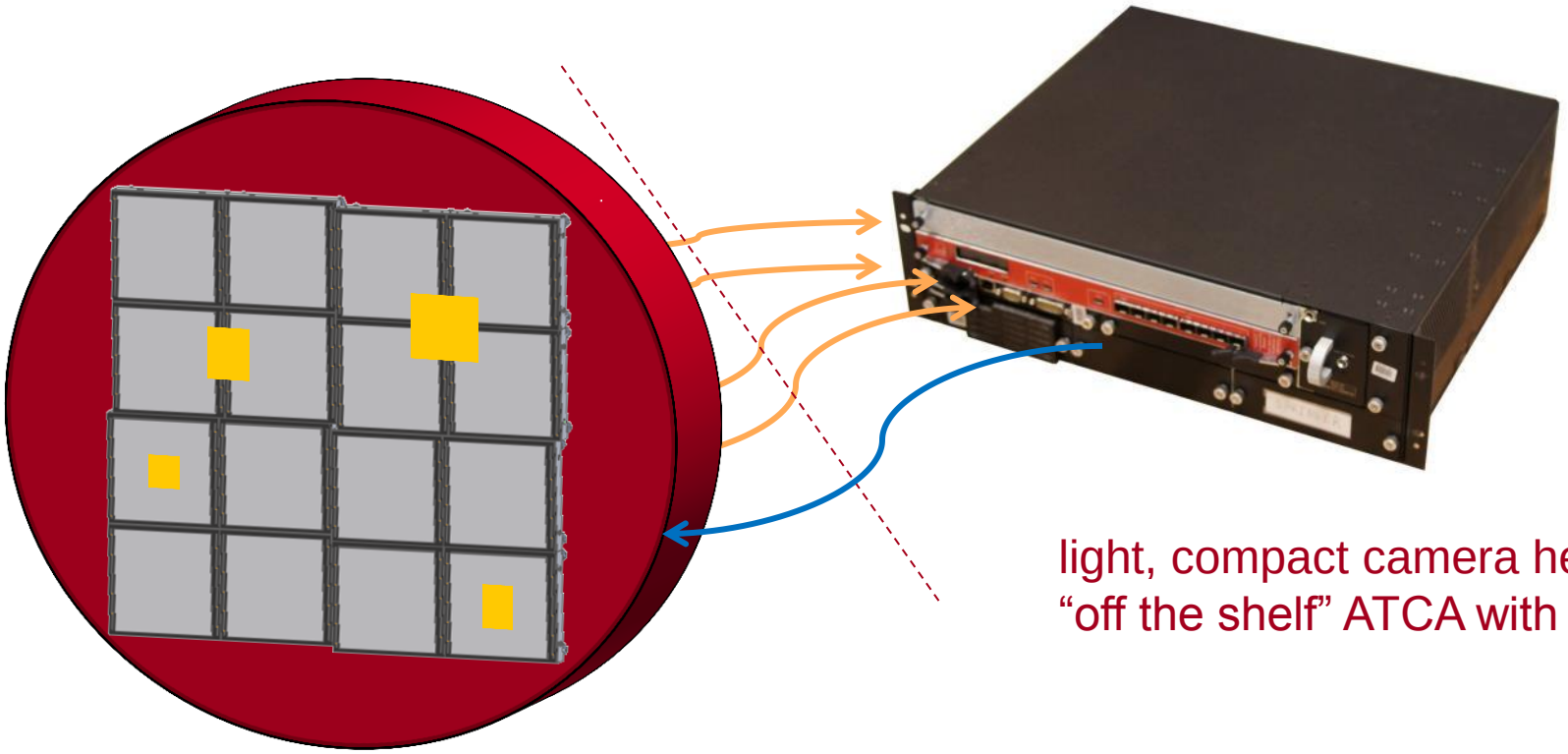


Serial Femtosecond Crystallography *de novo* phasing using Multiple Wavelength Anomalous Diffraction from Selenium



Dynamics of excited states in the time domain

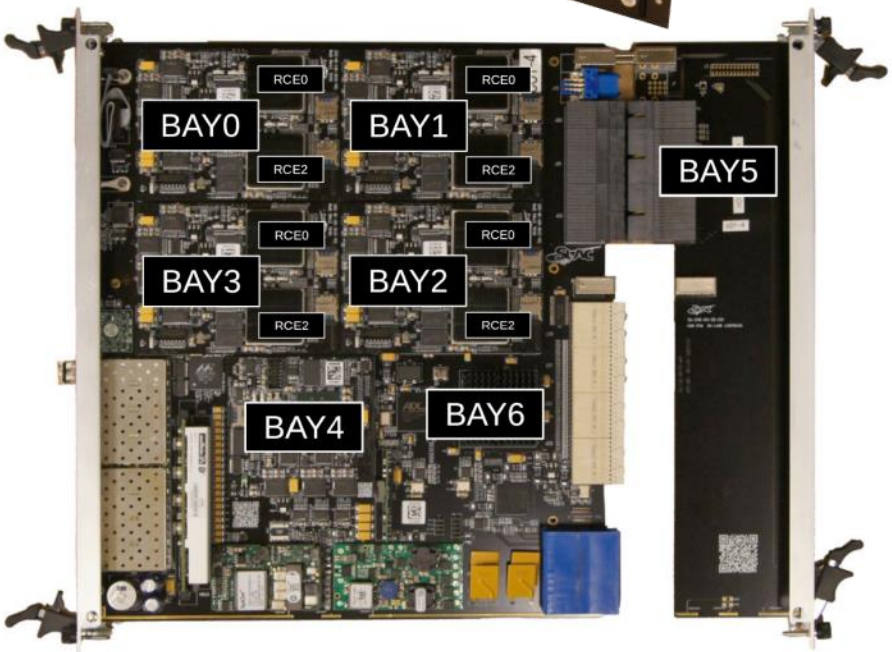
Camera PCB level electronics and DAQ integration



light, compact camera head with “off the shelf” ATCA with RCE

- To limit the complexity of the cameras PCB level electronics one could aggregate the detector module data and hand it over via next generation high speed serial links to ATCA crates and RCEs which can be located up to 20m away from the camera head.
- The RCE nodes could perform data processing on raw data for the purpose of calibration, online visualization, event selection, binning, averaging and triggering before the final data stream is send to the DAQ system.

2 slot ATCA with COB/RCE



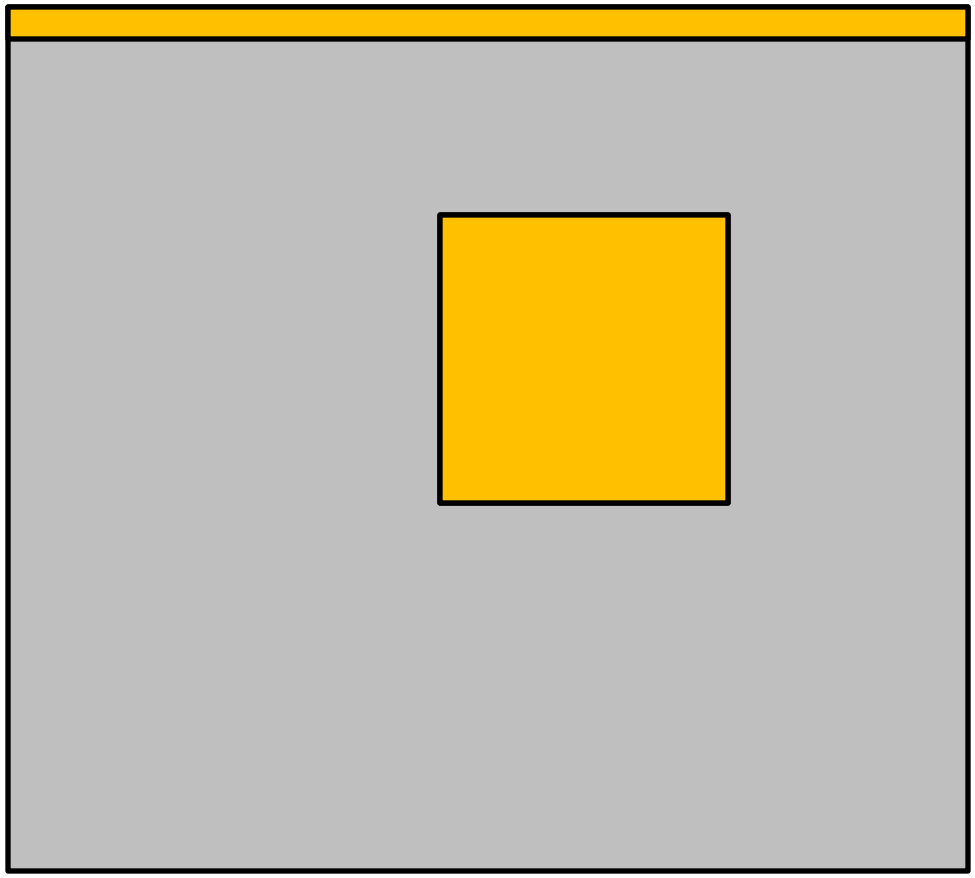
ATCA crate can house multiple COBs (cluster on a board)

1 COB has:

- 1 DTM (data transport module)
- 1 CEN
- 1 RTM (rear transition module)
  - optical link(s) to the detector front end
- 4 DPM (data processing module)
  - each has 2 RCE (reconfigurable cluster element)
    - FPGA with multi-core ARM
    - 1Gbyte DDR3 RAM
    - 64Gbyte Flash
    - Up to 40Gbit Ethernet to cluster interconnect switch
    - 12 MGT lanes to RTM

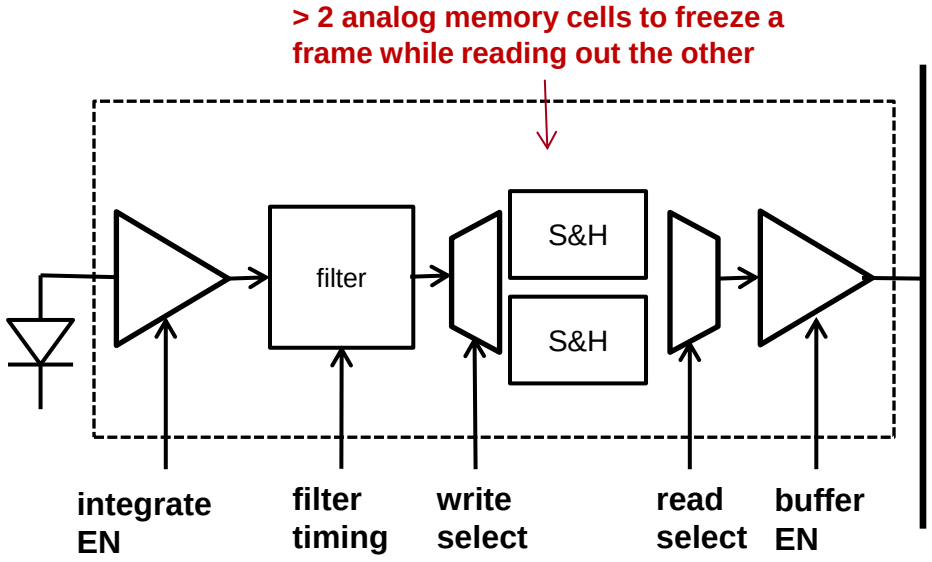
- RTEMS or LINUX as operation system
- software / firmware development environment

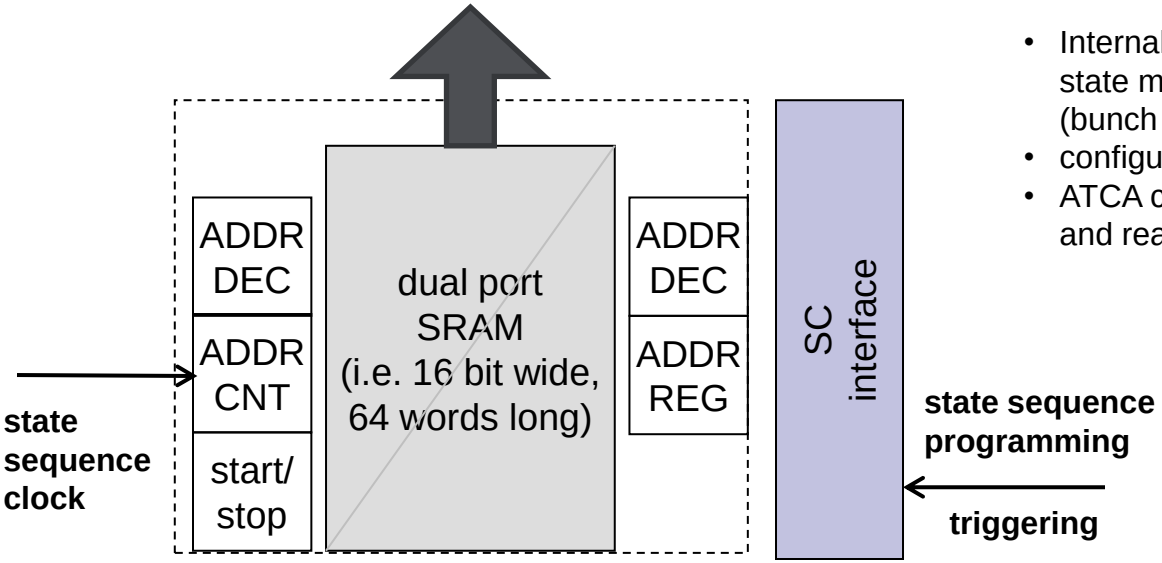
ROI, triggering and read during capture



- small region of interest (ROI) is readout at high frame rate
- In every frame of the RIO another small section of the full matrix is readout
- after a number of n frames we collected n ROI frames at high frame rate
- and one full frame at low frame rate
- supporting the acquisition of a slower full frame readout is useful for to observe in “real-time” if alignment or sample properties are drifting.

ROI, triggering and read during capture

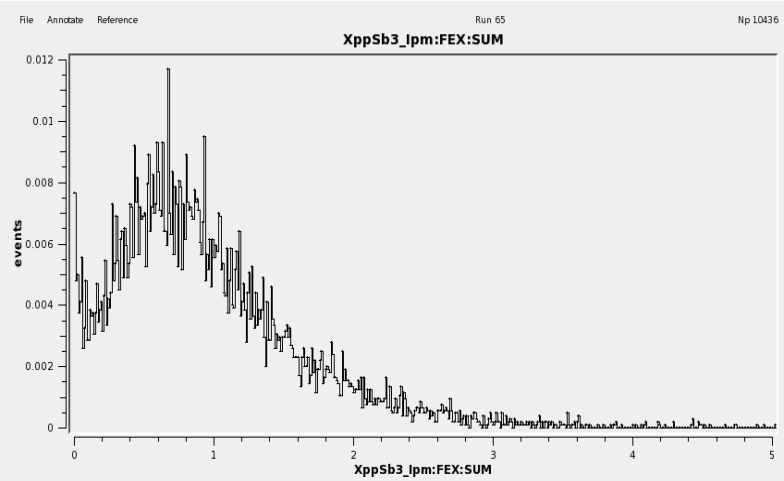


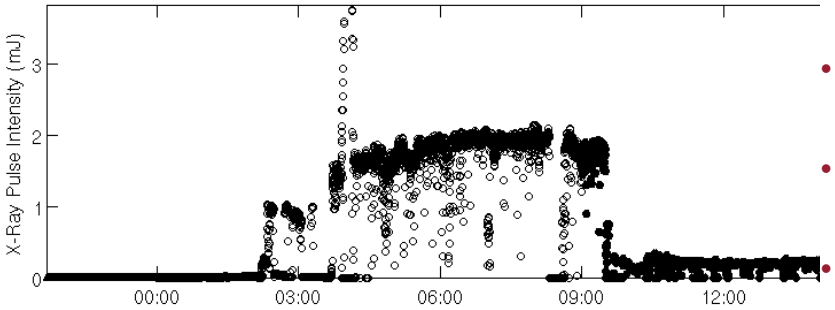


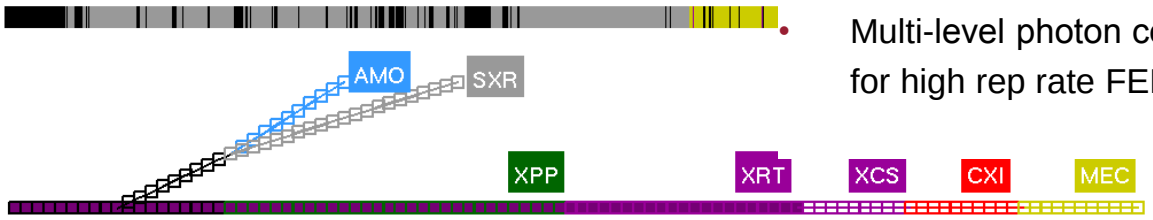
- In a hybrid pixel detector the (full parallel) pixel circuitry can operate faster than the ASIC / DAQ readout
  - -> region of interest readout can increase the effective frame-rate
  - supporting at the same time a slower full frame readout capability is useful for to observe in real-time if alignment or sample properties are drifting
  - -> triggering capability can increase the effective hit-rate or yield of science data
  - single frame freeze or integrate until freeze enables ROI driven full frame triggering
- Internal switch sequencing controlled by programmable state machine with external (bunch or RF synchronous) sequence clock
- configuration and trigger signals via SC
- ATCA crate generate the address information for storage and readout depending on trigger conditions

summing up bunches intelligently

binning detectors for pump-probe experiments at very high rep. rates

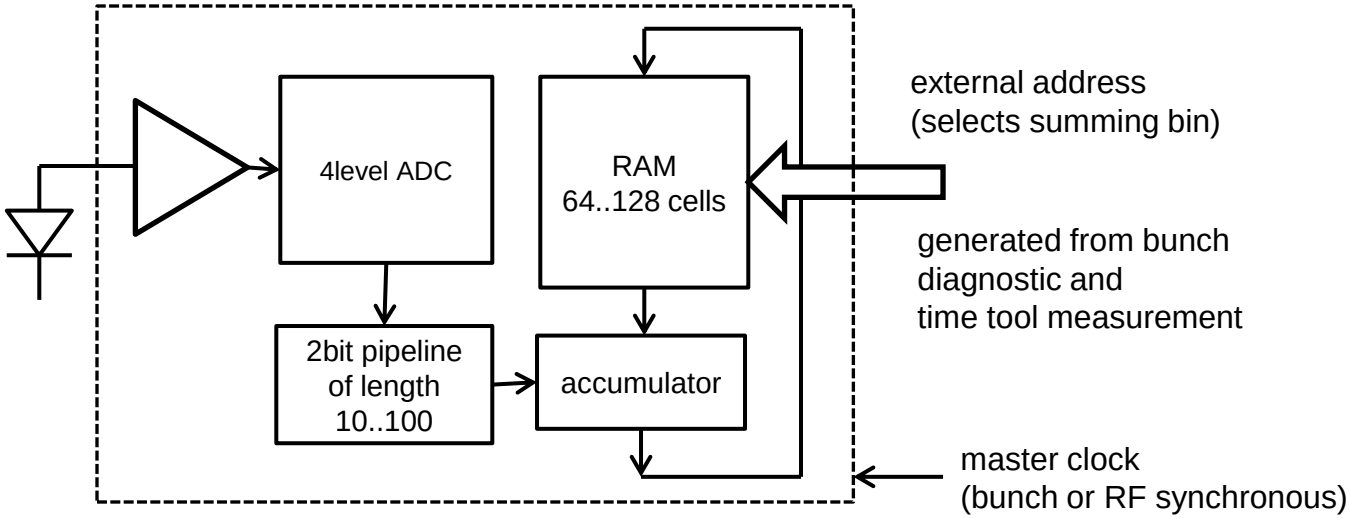






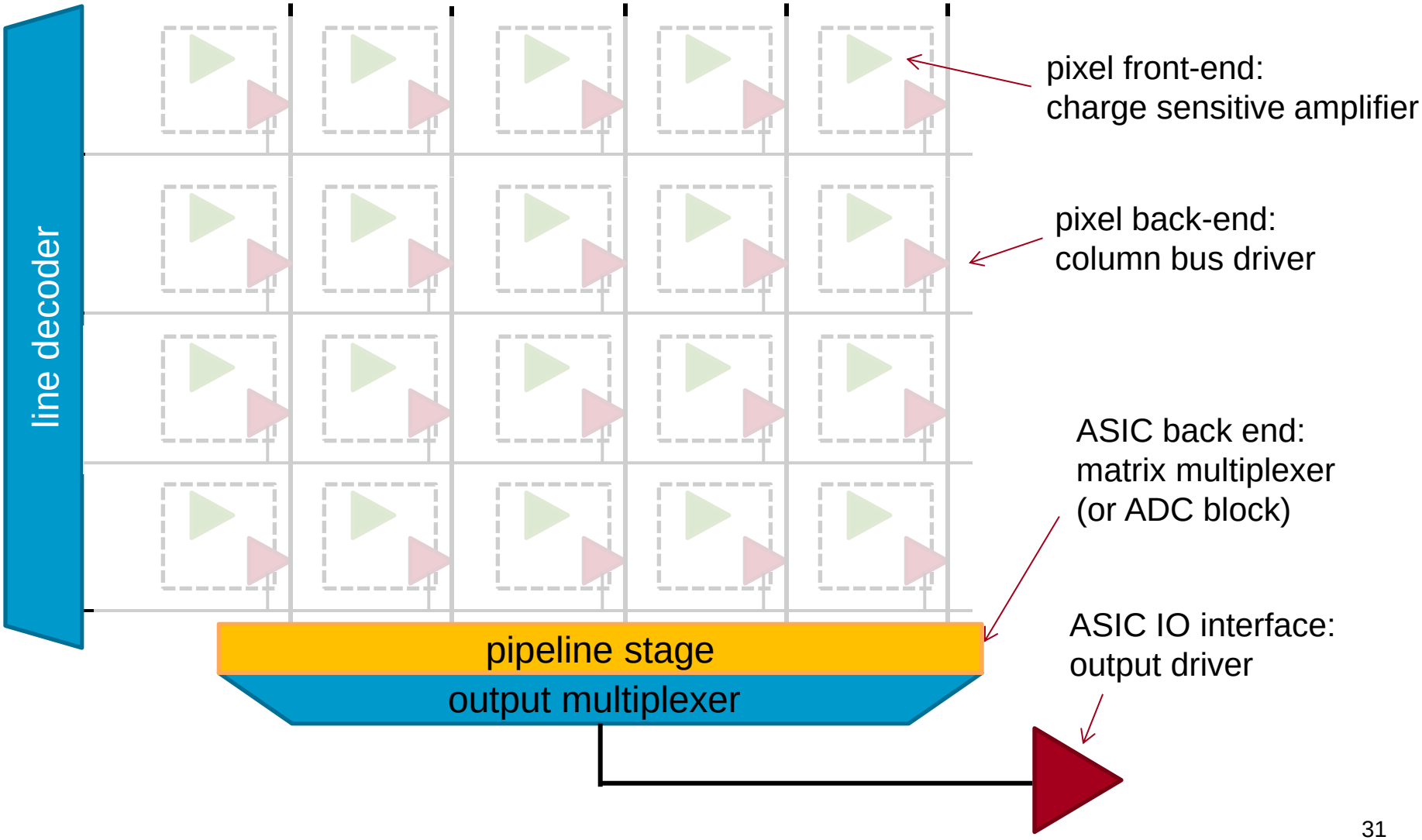
- For pump probe experiments data gets usually binned and averaged. Typical binning parameters are:
  - **sample parameters**
  - **FEL intensity**
  - **FEL vs pump LASER timing**
  - **FEL pointing (position on sample)**
- FEL vs LASER timing gets measured via time tool.
- At very high frame rates readout of raw data might be no longer feasible.
- Binning could be implemented within the detector
- The detector could provide a number of storage cells for averaging
- Which FEL shot goes into which storage cell is defined by an external supplied address signal
- A pipeline defines the maximum allowed latency for the external address
- Averaging is reasonably easy to implement with photon counters
- Multi-level photon counters (0,1,2,3,…) might be an option for high rep rate FELs

The binning photon counter pixel architecture

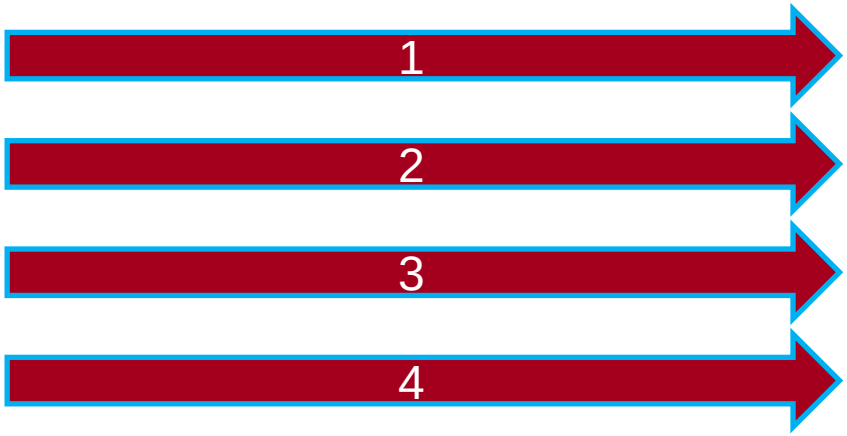


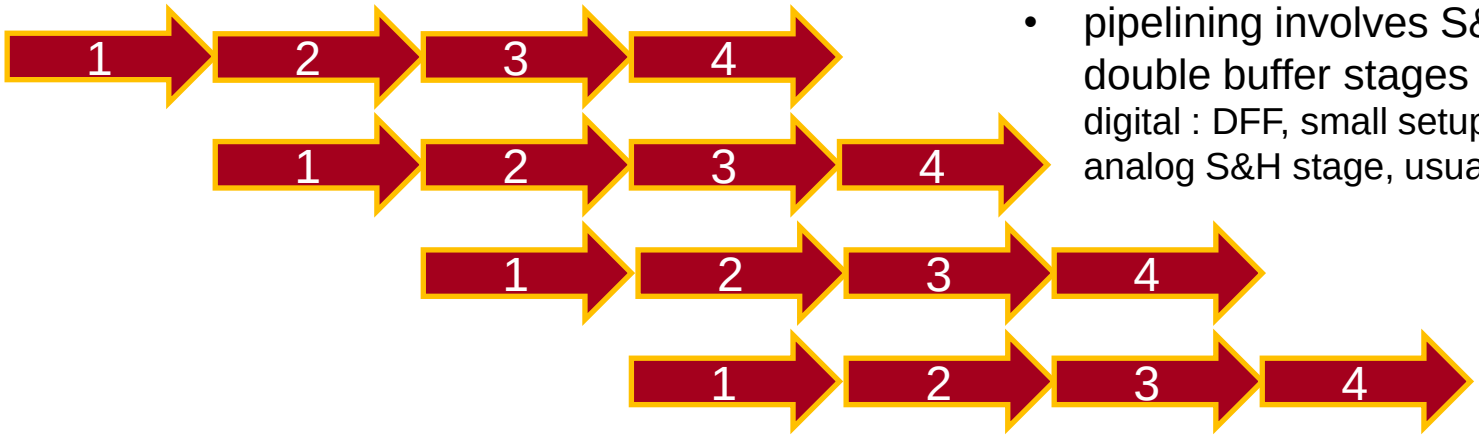
- "slow" synchronous front end amplifier (cycling time of 10us for 100kHz) for low noise operation down < 2 keV
- try to minimize charge sharing (large pixels, hexagonal pixels, thin pad sensor:100um for soft-xrays)
- multi level comparator to handle 0,1,2 and more photon events (potential with out of range flag)
- only one accumulator with compact RAM to mimic many virtual counters
- accumulator can sum 0,1,2, … photon events
- memory could be between 64 and 128 cells enabling a corresponding number of binning.
- pipeline can be dynamic logic for compactness
- at 100 kHz a 100 element pipeline will give 1ms of time for the external address signal (i.e. from XPP time tool)
- 200um pixels in 110nm technology might be reasonable

The “standard” active pixel matrix – single line readout



How to speed things up: parallelization and pipelining



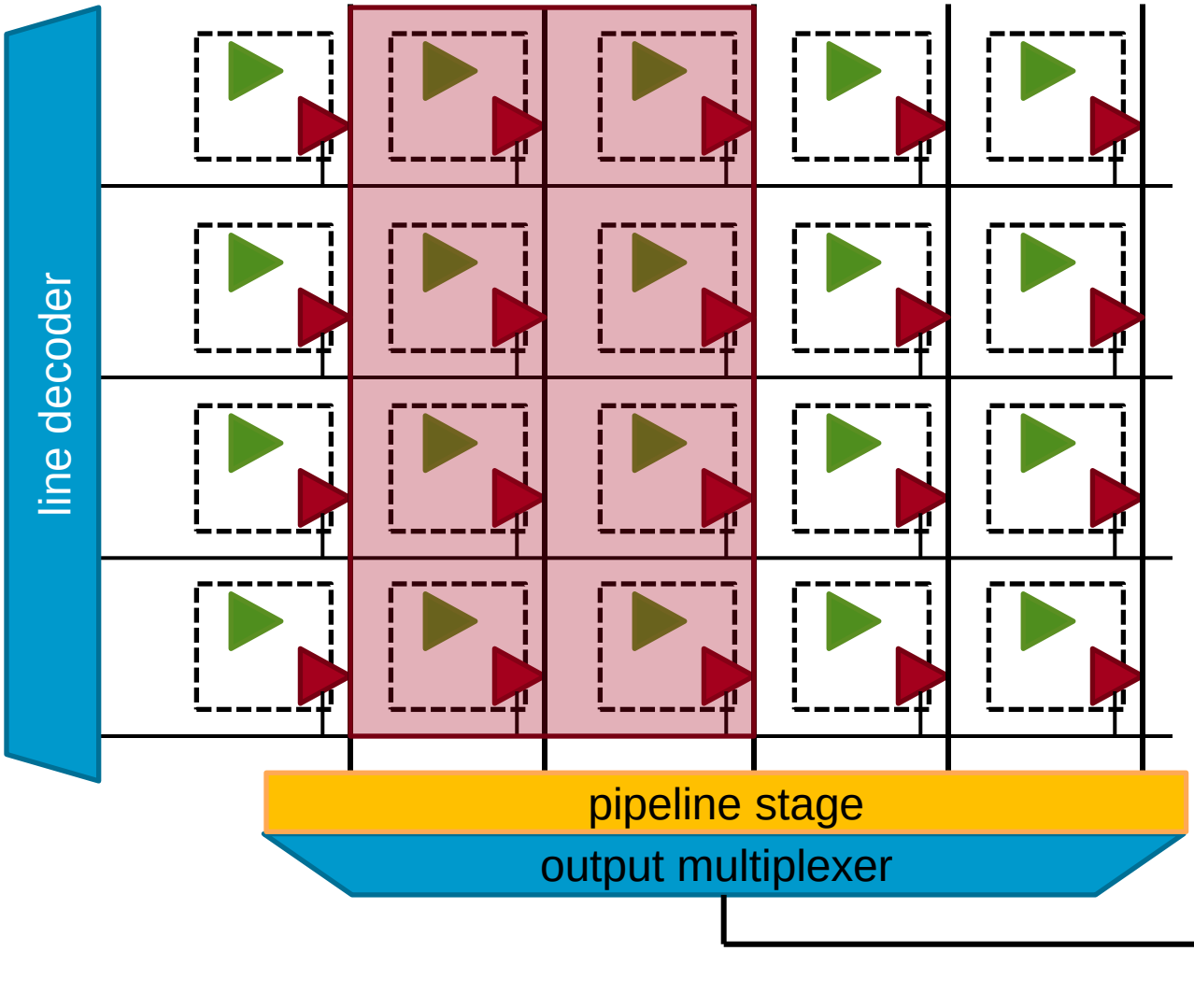


- fastest way from n to 1 is a balanced tree
- **parallelization** often means simply more hardware units
  - multiple bus lines active at the same time
- **pipelining** implies to reorganize, divide and rescale
  - pixel pooling
  - buffer sizing
  - bus length sizing
- pipelining involves S&H double buffer stages

  digital : DFF, small setup time requirement

  analog S&H stage, usually long setup time

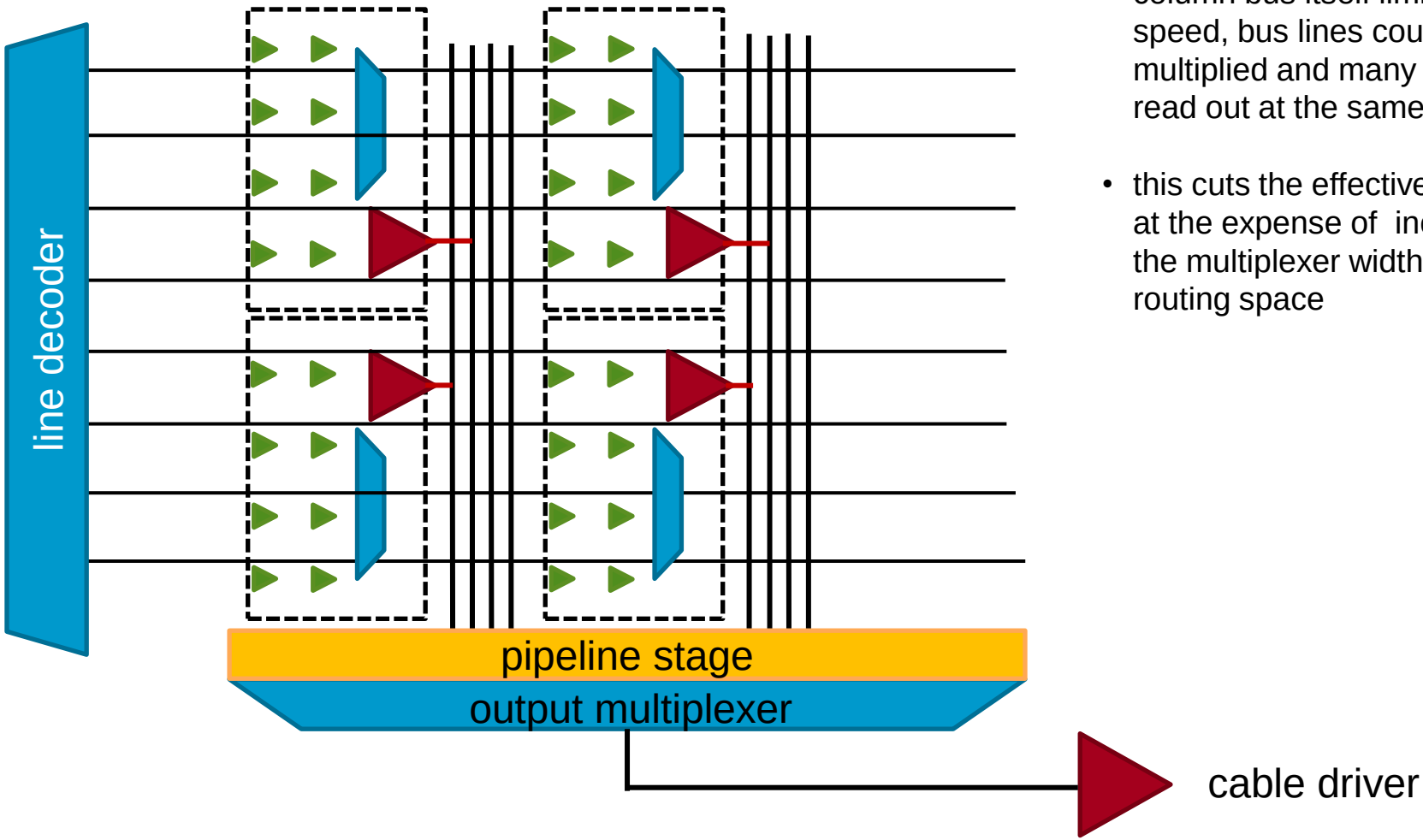
Pooling pixels into Superpixels



tree segmentation of matrix:

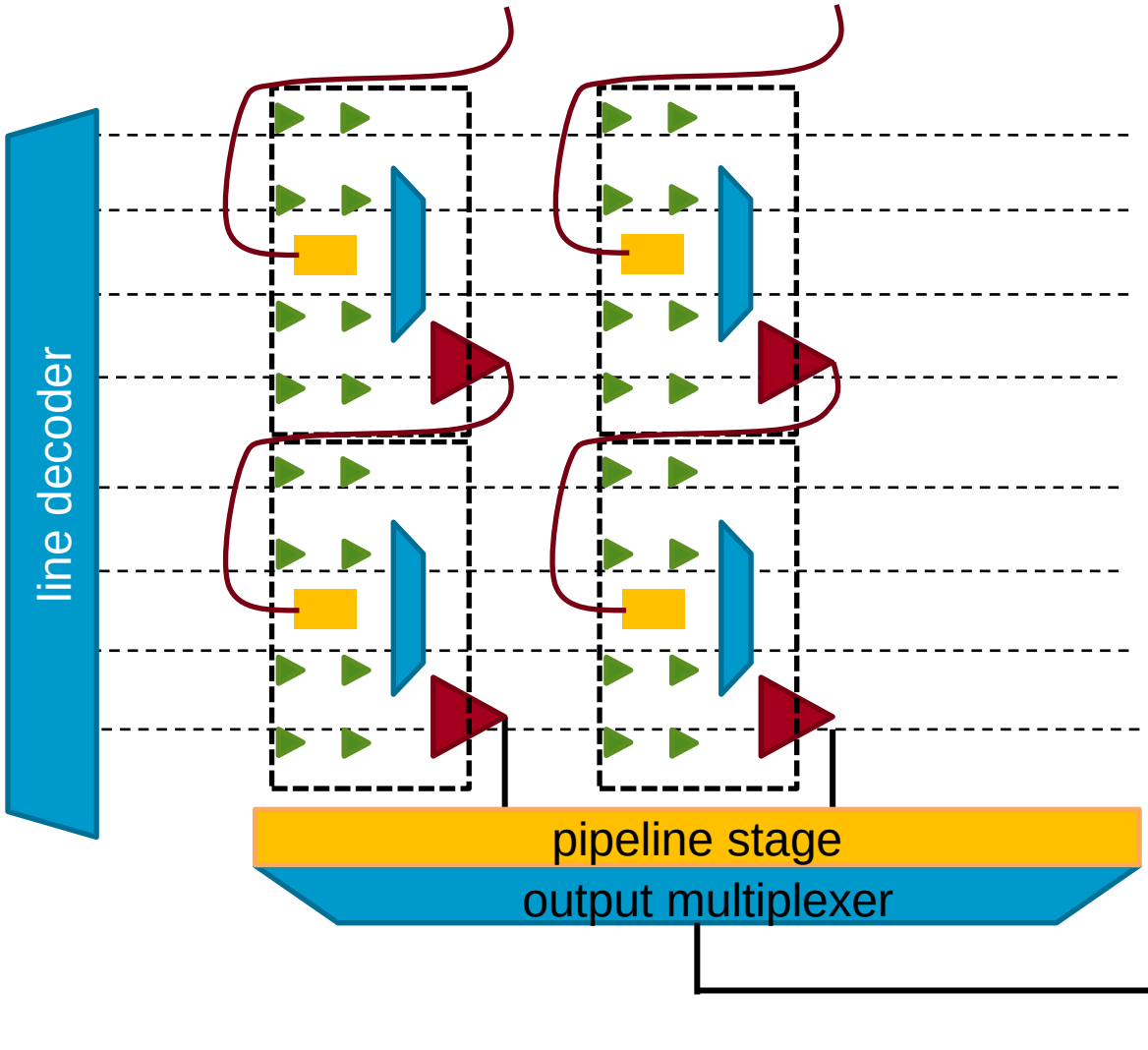
- every pixel has only to provide the signal to the Superpixel buffer
- buffer is shared between pixels and therefore can be stronger (larger, more current) and more complex (fully differential)

Superpixel with multiple column buses



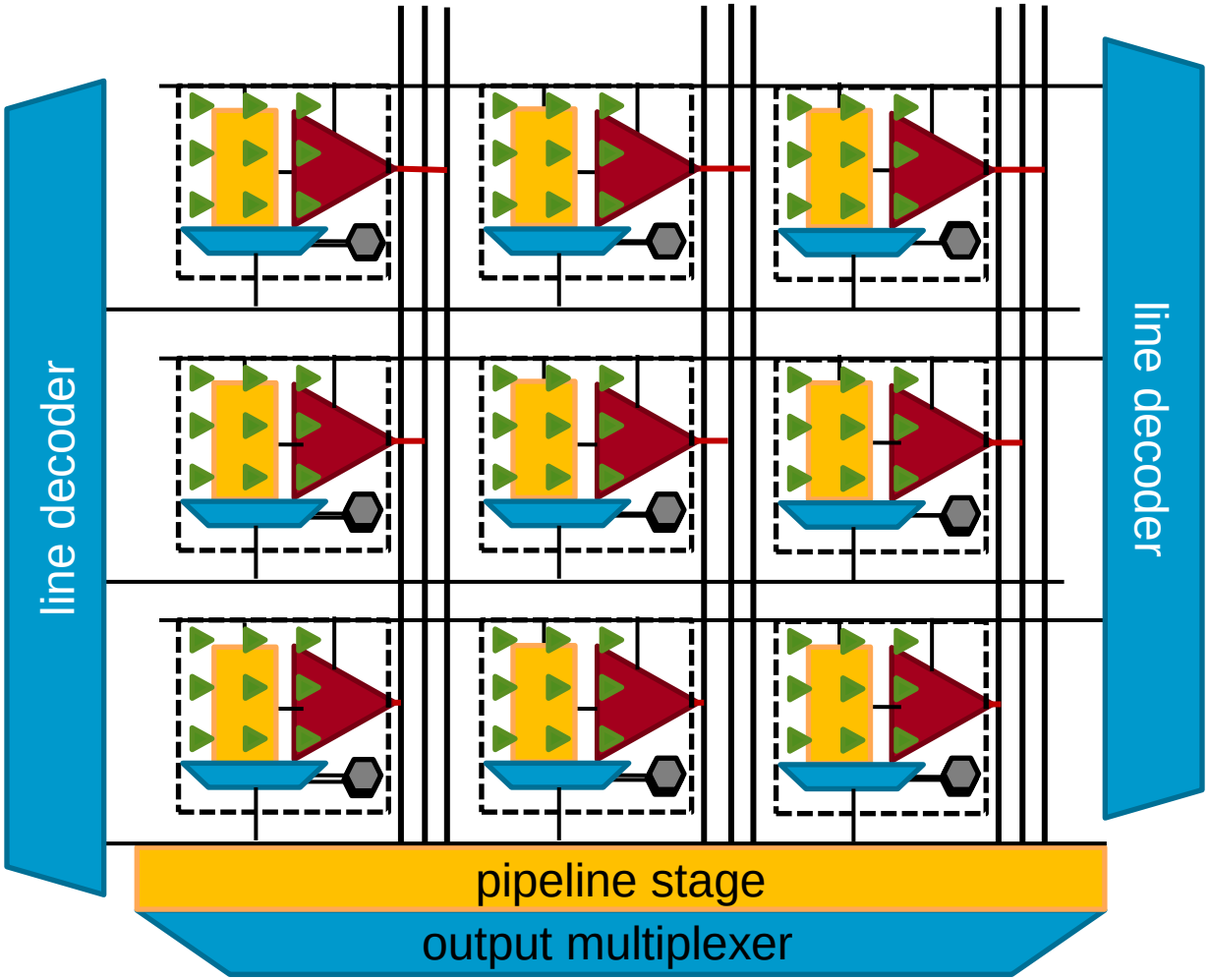
- In cases the RC time of the column bus itself limits the speed, bus lines could be multiplied and many pixels read out at the same time.
- this cuts the effective line-rate at the expense of increasing the multiplexer width and routing space

Superpixel with mid-matrix pipeline stage



- Superpixels might be an “elegant” way of including mid-matrix pipeline stages (without 3D technology)
- the matrix data is transferred one short segment at a time like CCD
- Once a ROI is set up we can keep the pipeline filled with ROI data (but having more than 1 frame of lag in readout)

Superpixels and 3D integration



- Superpixel column bus drivers are in a second tier of electronics
- Superpixels drive only the TSV and the pipeline stage in the second tier -> more space for better amplifiers
(soft x-rays)
- 3D technology enables the effective use of heterogeneous integration: front-end and back-end can be two different process technologies:
i.e. SiGe amplifiers in the first tier and CMOS for ADCs and logic in the second tier.
- for digital data communication RC bus time is not as important (unsettled operation possible)

Conclusions

- first cameras will be deployed in summer
- bigger cameras under development
- ePIX family can cover most of the needs particularly in the energy range between 2 – 18 keV.
- higher frame rate ePIX members are being developed
- ATCA COB as standardized backend electronics
  - for camera operation
  - data readout and aggregation
  - low level data processing (analog multiplexer waveform digital signal processing)
  - calibration, frame generation, real time monitoring
  - sub pixel resolution
  - real time triggering