The RD53 Project

Pixel Readout Chips for Extreme Rate and Radiation

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on behalf of the RD53 collaboration

RD53: an ATLAS-CMS-LCD collaboration

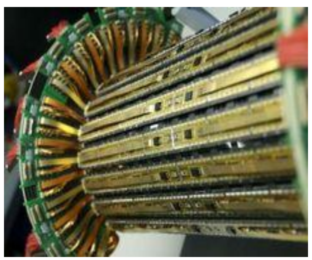
- RD53 was organized to tackle the extreme and diverse challenges associated with the design of pixel readout chips for the innermost layers of particle trackers at future high energy physics experiments (LHC – phase II upgrade of ATLAS and CMS, CLIC)

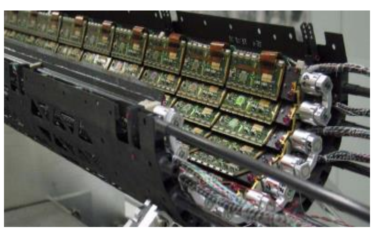
- ❑ Very high hit rates (1-2 GHz/cm^2), need of an intelligent data processing
- ❑ Very high radiation levels (1 Grad Total Ionizing Dose, 10^{16} neutrons/cm^2)
- ❑ Small pixel cells to increase resolution and reduce occupancy (~50x50um^2 or 25x100um^2)

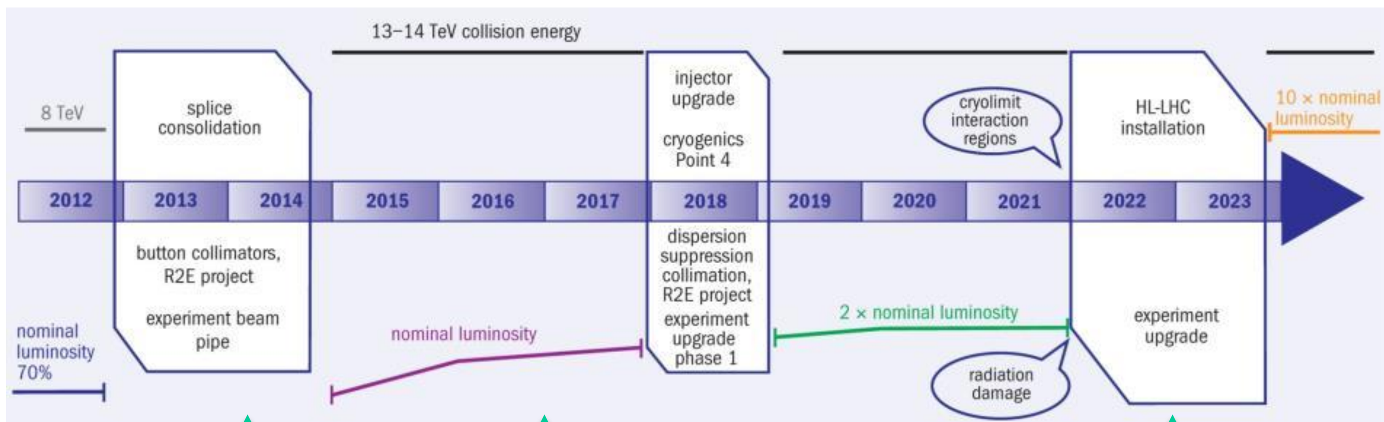
➔ Large chip: > 2cm x 2cm, ½ - 1 Billion transistors in a 65 nm CMOS technology

LHC pixel upgrades

- Current LHC pixel detectors have clearly demonstrated the feasibility and power of pixel detectors for tracking in high rate environments
- Phase1 upgrades: Additional pixel layer, ~4 x hit rates
  - ATLAS: Addition of Inner B Layer (IBL) with new 130nm pixel ASIC (FEI4)
  - CMS: New pixel detector with modified 250nm pixel ASIC (PSI46DIG)
- **Phase2 upgrades**: ~16 x hit rates, ~4 x better resolution, 10 x trigger rates, 16 x radiation tolerance, Increased forward coverage, less material, , ,
  - Installation: ~ 2022
  - Relies fully on significantly improved performance from next generation pixel chips.







ATLAS Pixel IBL

CMS Pixel phase1

CMS & ATLAS phase 2 pixel upgrades

100MHz/cm²

400MHz/cm²

1-2GHz/cm²

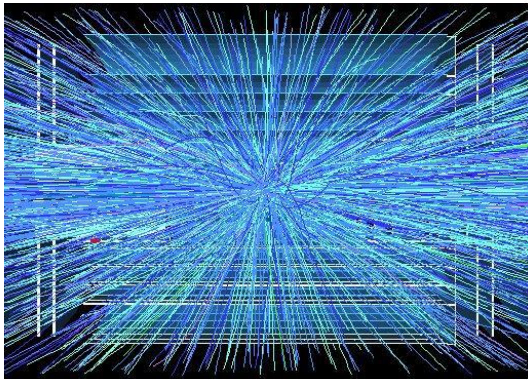
LHC- Phase II pixel challenges

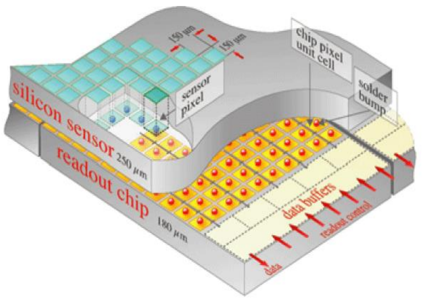
- ATLAS and CMS phase 2 pixel upgrades very challenging
  - Very high particle rates: 500MHz/cm^2
    - Hit rates: 1-2 GHz/cm^2 (factor ~16 higher than current pixel detectors)
  - Smaller pixels: ~¼ (~50x50um^2 or 25x100um^2)
    - Increased resolution
    - Improved two track separation (jets)
    - Outer layers can be larger pixels, using same pixel chip
  - Participation in first/second level trigger ? (no)
    A. 40MHz extracted clusters (outer layers) ?
    B. Region of interest readout for second level trigger ?
  - Increased readout rates: 100kHz -> ~1MHz
    - Data rate: 10x trigger X >10x hit rate = **>100x !**
  - Low mass -> Low power

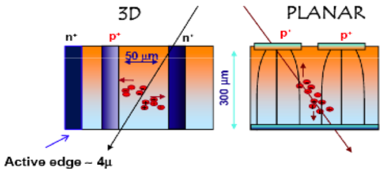
  Very similar requirements (and uncertainties) for ATLAS & CMS
- Unprecedented hostile radiation: 1 Grad, 10^{16} Neu/cm^2
  - Hybrid pixel detector with separate readout chip and sensor.
    - Monolithic seems unfeasible for this very high rate hostile radiation environment
  - Phase2 pixel will get in 1 year what we now get in 10 years

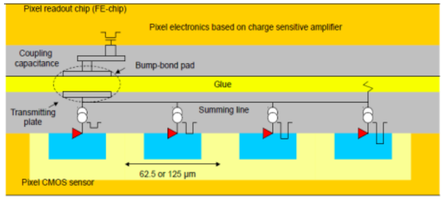
  (10.000 x more radiation than space/mil !)
- Pixel sensor(s) not yet determined
  - Planar, 3D, Diamond, HV CMOS, …
  - Possibility of using different sensors in different layers

Complex, high rate and radiation hard pixel chips required









CLIC vertex detector R&D

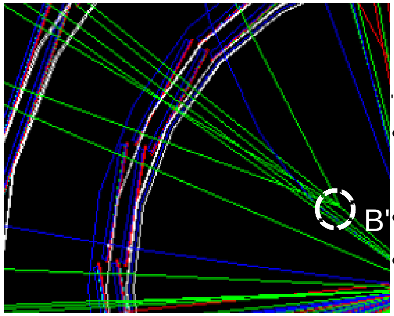
- The need of small pixel cells providing a fine time slicing may be also addressed by a 65nm CMOS readout chip ➔ **CLICpix prototype chip**

Vertex-detector requirements"

- Efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

$a \sim 5\ \mu m,\ \ b \sim 15\ \mu m$

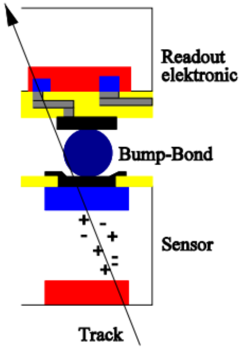


- ✎ good single point resolution: σ_{SP}~3 μm"
  - ✎ small pixels ~25x25 μm^2, analog readout"
- ✎ low material budget: X ≲0.2% X_0 / layer"
  - ✎ corresponds to ~200 μm Si, including supports, cables, cooling"
  - ✎ low-power ASICs (~50 mW/cm^2), power pulsing, air-flow cooling "

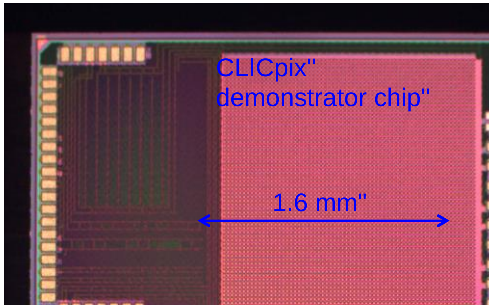
- Time slicing with ~10 ns accuracy, to suppress beam-induced backgrounds"
  - ✎ High-resistivity sensors, fast readout"
  - ✎ Hybrid concept (like for LHC detectors):
    "ultra-thin sensors
    "+ high-performance r/o ASICs"

- Trigger-less readout during 20 ms gaps between trains"

Hybrid pixel" technology"



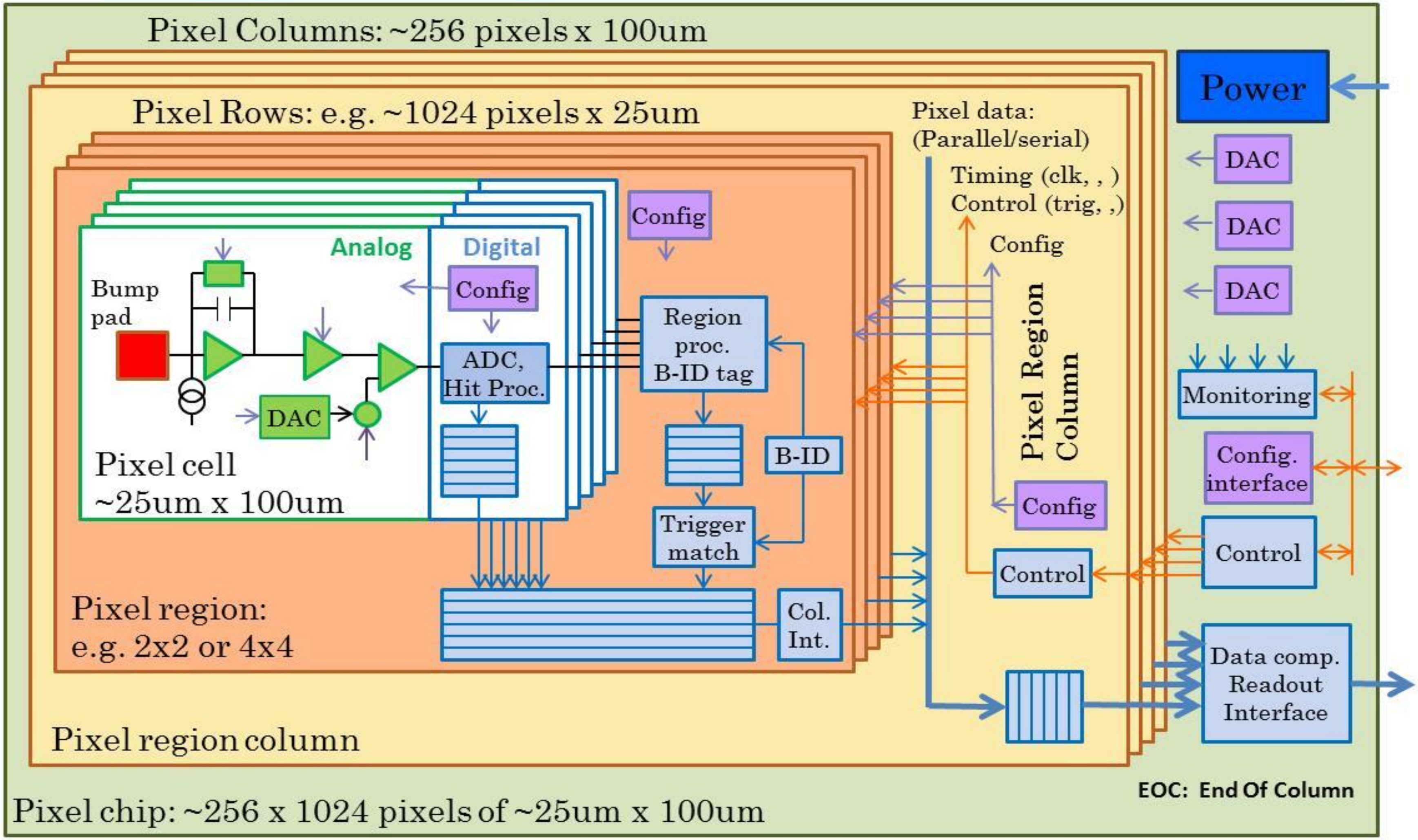
- **65 nm CMOS hybrid r/o chip**, targeted to CLIC vertex detectors"
- based on **Timepix/Medipix** chip family, synergy with HL-LHC pixel r/o projects (**RD53** collaboration on 65 nm r/o) "
- **demonstrator chip** produced with fully functional 64 x 64 pixel matrix"
- **25 μm** pixel pitch"
- simultaneous **4-bit time (TOA) and energy (TOT)** measurement per pixel"
- ✎ front-end **time slicing < 10 ns** "
- selectable **compression** logic: pixel, cluster + column-based"
- ✎ full chip r/o in less than 800 μs" (at 10% occup., 320 MHz r/o clk)"
- **power pulsing scheme"**
- ✎ P_{avg}< 50 mW/cm^2 "



A 65 nm CMOS pixel readout chip for HL-LHC

- Pixel readout chips critical to be ready for phase 2 upgrades
  - Technology: Radiation qualification
  - Building blocks: Design, prototyping and test
  - Architecture definition/optimization/verification
  - Chip prototyping, iterations, test, qualification and production
  - System integration
    - System integration tests and test-beams
  - Production and final system integration, test and commissioning
- Phase 2 pixel chip very challenging
  - Radiation
  - Reliability: Several storage nodes will have SEUs every second per chip.
  - High rates
  - Mixed signal with very tight integration of analog and digital
  - Complex: ~256k channel DAQ system on a single chip
  - Large chip: >2cm x 2cm, ½ - 1 Billion transistors.
  - Very low power: Low power design and on-chip power conversion
- ATLAS and CMS have evolved to similar pixel chip architectures and plans to use same technology (65nm) for its implementation.
- Experienced chip designers for complex mixed signal ICs in modern technologies that must work in a extremely harsh radiation environment is a scarce and distributed "resource" in HEP.

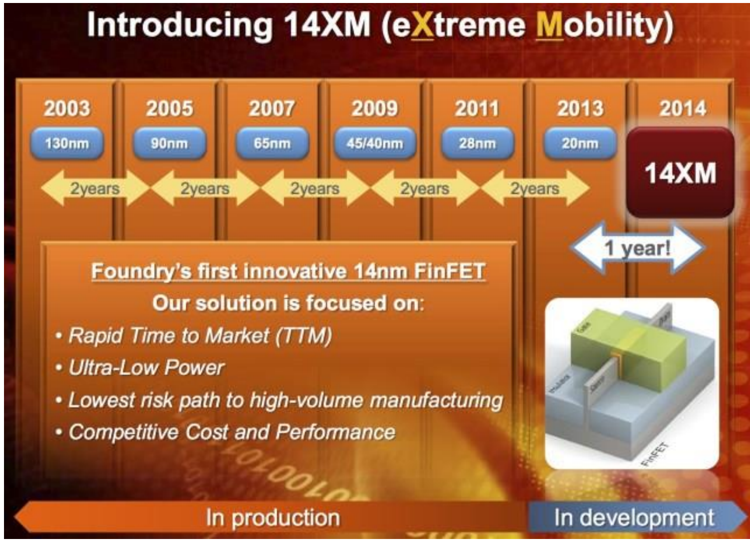
Chip architecture

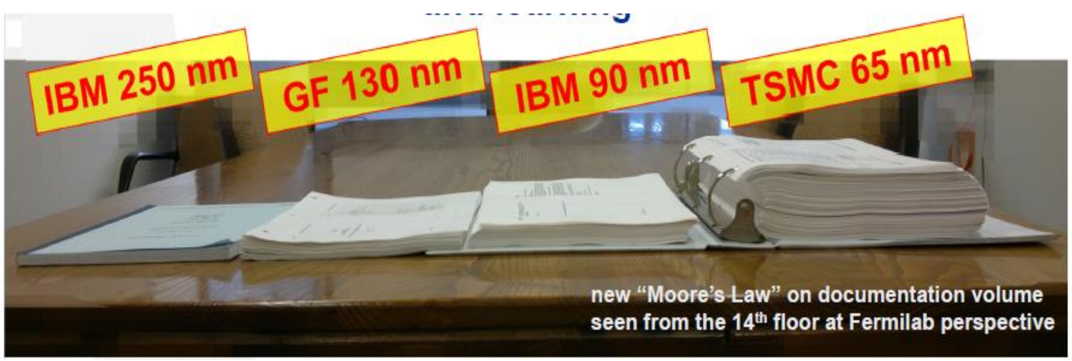


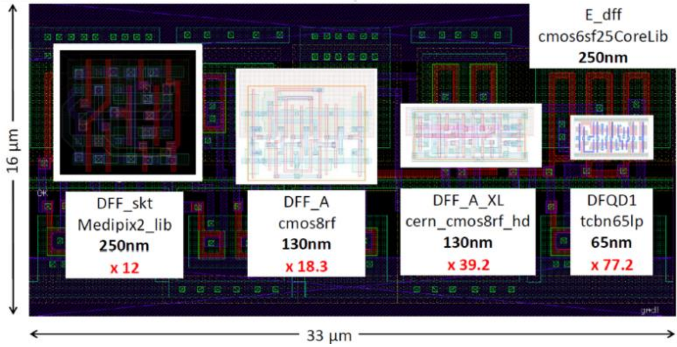
- 95% digital (as for FEI4)
- Charge digitization (TOT or ADC)
- ~256k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column
- Chip size: >20 x 20 mm^2

Low Power 65 nm CMOS

- Mature technology:
  - Available since ~2007
- High density and low power
  - High density vital for smaller pixels and ~100x increased buffering during trigger latency
  - Low power tech critical to maintain acceptable power for higher pixel density and much higher data rates
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Access: CERN frame-contract with TSMC and IMEC
  - Design tool set, Shared MPW runs, Libraries, Design exchange within HEP community
- Affordable (MPW from foundry and Europractice, ~1M NRE for final chips)
- Significantly increased density, speed, , , and complexity compared to 130nm !





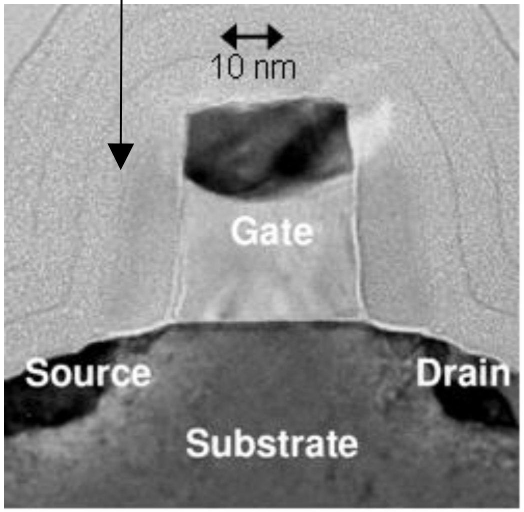


65 nm CMOS at extreme radiation levels

- Radiation hardness
  - Uses thin gate oxide
    - Radiation induced trapped charges removed by tunneling
    - More modern technologies use thick High K gate “oxide” with reduced tunneling/leakage ?.
  - Verified for up to 200 Mrad
  - To be confirmed for 1 Grad
    - PMOS transistor drive degradation, V_t shift, Annealing ?
  - CMOS normally not affect by NIEL
    - To be confirmed for 10^{16} Neu/cm^2
    - Certain circuits using “parasitic” bipolars to be redesigned ?
  - SEU tolerance to be built in (as in 130 and 250nm)
    - SEU cross-section reduced with size of storage element, but we will put a lot more per chip
  - All circuits must be designed for radiation environment (e.g. Modified SRAM)
- Annealing scenario critical
  - Detectors will run cold (~-20^{o}C)
  - Yearly annealing periods ? (room temp or higher ?)
- If unacceptable degradation then other technologies (alternative foundries, 40nm, etc.) must be evaluated and/or **a replacement strategy** must be applied for inner pixel layers.

Radiation effects in 65 nm CMOS

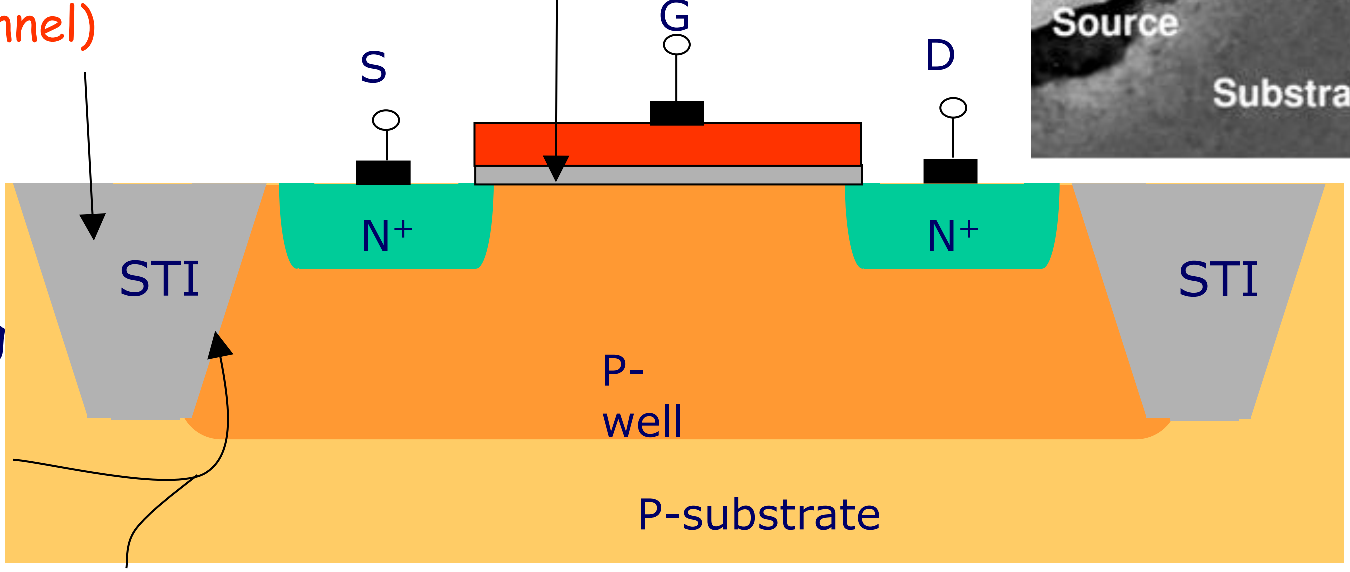
Spacer dielectrics may be radiation-sensitive



Thick Shallow Trench Isolation Oxide (~ 300 nm); radiation-induced charge-buildup may turn on lateral parasitic transistors and affect electric field in the channel)

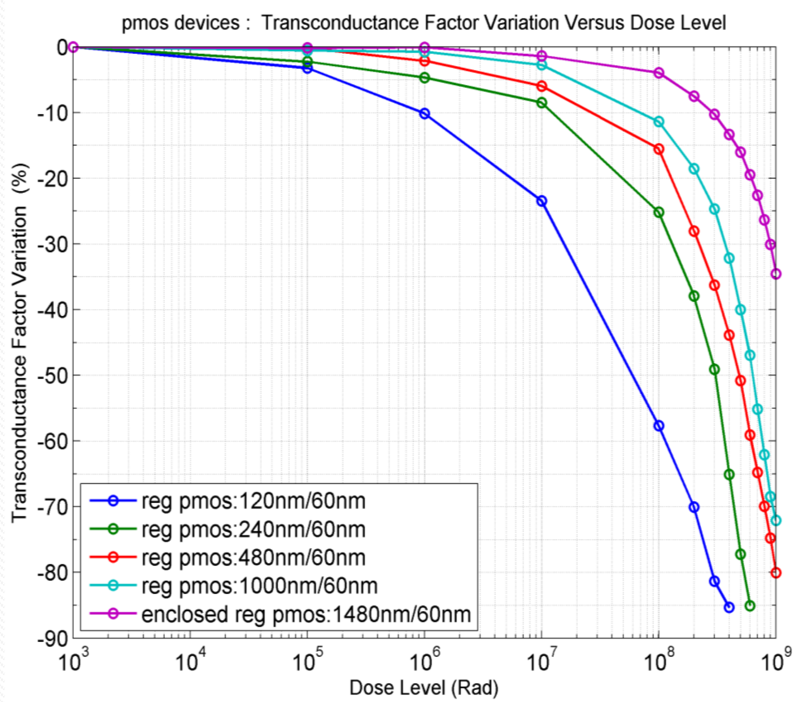
Thin (rad-hard) gate oxide for core devices, becomes thicker (and rad-softer) for I/O transistors

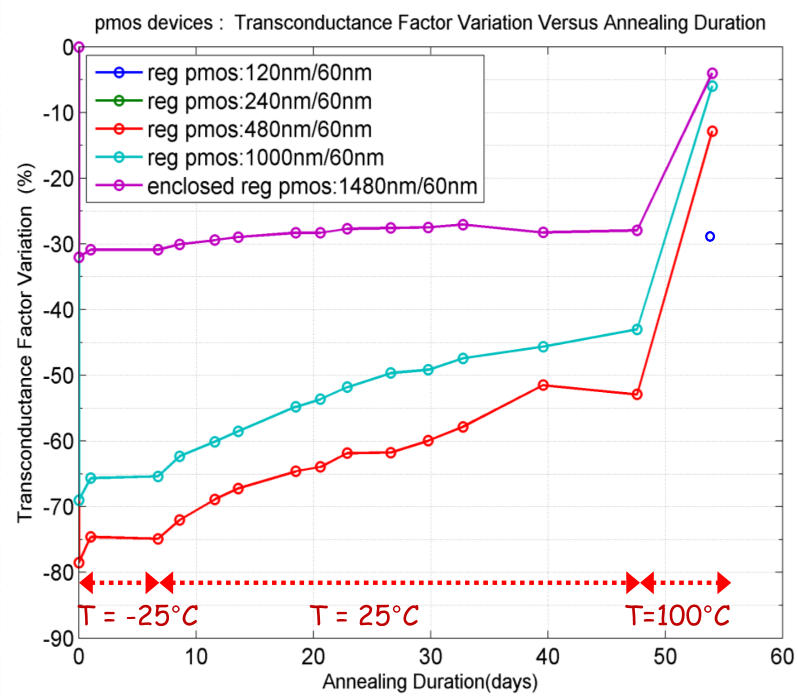
Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices



Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths)

65nm transistors at extreme total ionizing dose: the PMOS





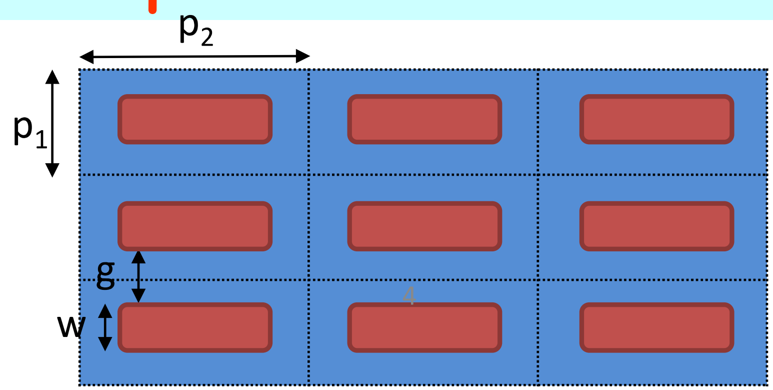
- Among other effects, PMOSFETs (especially minimum size ones) show a large transconductance degradation, which becomes very steep at TID > 100 Mrad (partial recover after annealing)
- Damage mechanisms have yet to be fully understood (including dependence on geometry and bias conditions under irradiation and annealing, dose rate, temperature, radiation source…)
- **See Marlon's presentation on Friday**

Interfacing the 65 nm readout chip with a pixel sensor

- The features of the pixel sensors have an obvious impact on the design of the readout chip.
- Several options are still open, in terms of sensor technology, geometry, pitch,…; choices will be driven by physics needs, radiation tolerance, cost,…
- The pitch of pixel readout cells will also be dependent on the available interconnection technology, which brings along many other features and constraints (minimum pitch and height of bumps, minimum sensor thickness,…)
- Pixel capacitance, leakage current, collected charge are among essential specifications for the design of the analog front-end.

Pixel sensor capacitance

n^+ Implant width (μm)	$C^{unirrad}$ (fF)
38	200 ± 5
32	153 ± 5
20	103 ± 5
14	88 ± 5



Inter-pixel capacitance C_p measured on a 400 x 50 μm² n-on-n Si pixel sensor

G. Gorfine et al. / Nuclear Instruments and Methods in Physics Research A 465 (2001) 70–76

		FE-I3	FE-I4	FE-x
Pixel geometry	p1, p2	400 x 50 μm²	250 x 50 μm²	125 x 25 μm²
Pixel area	A_p	20.000 μm²	12.500 μm²	3.125 μm²
Pixel perimeter	L_p	900 μm	600 μm	300 μm
Pixel density [#pixels/cm²]		5.000	8.000 X 4	32.000
Perimeter length per cm²	P_T	4.5 m	4.8 m	9.6 m
Pixel capacitance	C_d	150 fF (meas.)	110 fF (meas.)	52 fF (estim.)
Capacitance per cm²	C_{area}	750 pF	880 pF X 2	1.7 nF (estim.)

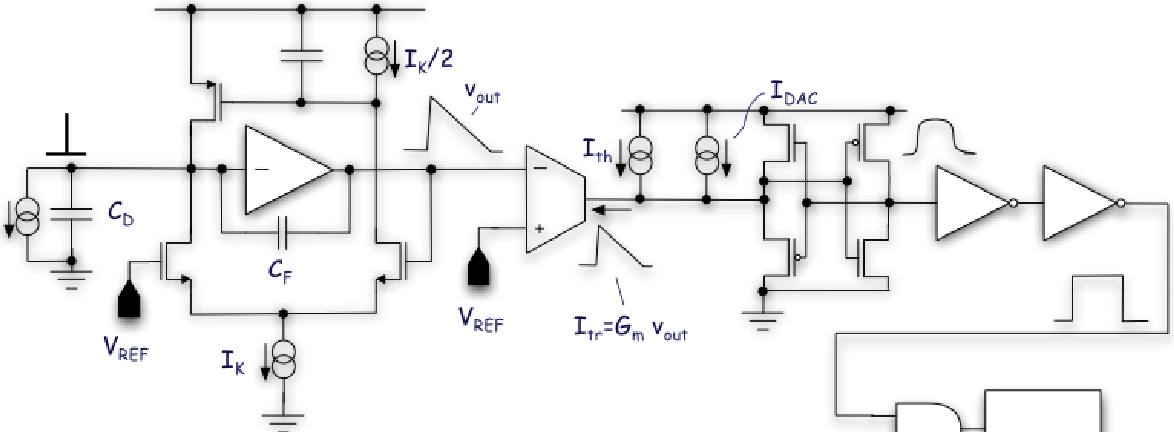
Hans Krueger, RD53 Analog WG meeting

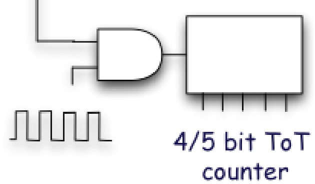
- Planar pixel capacitance dominated by capacitance to neighbor pixels $C_{perimeter}$
- Estimated perimeter capacitance (20μm gap between implants): 0.16 fF /μm
- Total capacitance per area scales approx. with $\sqrt{pixel\ density}$

Analog channel in the pixel readout cell: asynchronous or synchronous?

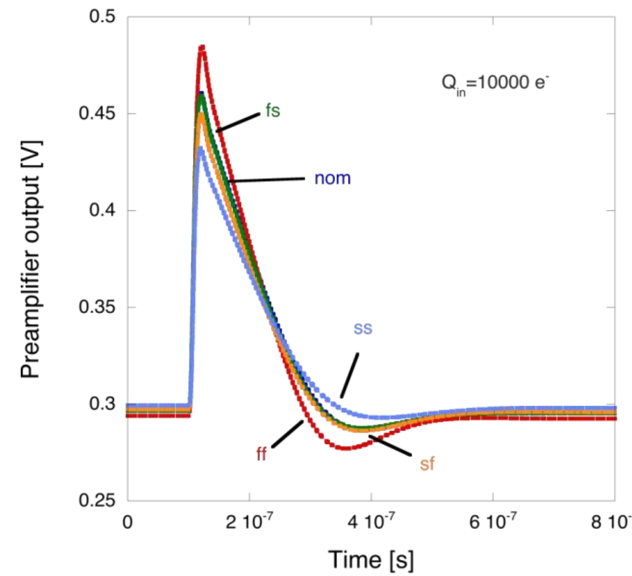
- The classical continuous-time analog processing channel is a well-established solution for pixel sensors in high-energy physics
- To reduce power (and area), this channel may include just two stages (charge-sensitive preamplifier + asynchronous comparator), and A/D conversion may be based on a time-over threshold measurement; **other A/D architectures will also be evaluated by RD53**
- In an advanced CMOS process, a synchronous architecture may be a good alternative, with self-calibration and discrete-time signal processing features (correlated double sampling, autozeroing) clocked by the bunch-crossing cadence **(see Farah's talk)**
- **Various options will be explored in the first year of RD53**

A continuous-time analog channel… (INFN-PV/BG)





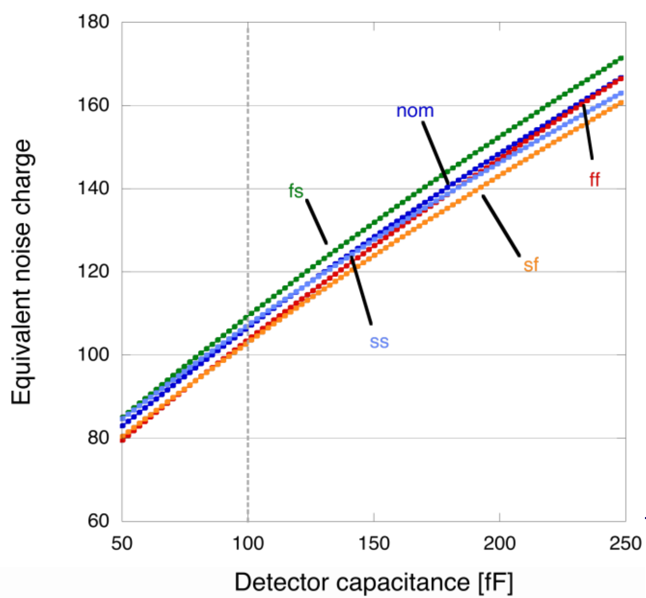
- Single amplification stage for minimum power dissipation
- Krummenacher feedback to comply with the expected large increase in the detector leakage current
- High speed, low power current comparator
- Relatively slow ToT clock – 40 (80) MHz
- 4/5 bit counter – 400 ns maximum time over threshold
- 30000 electron maximum input charge, ~500 mV preamplifier output dynamic range

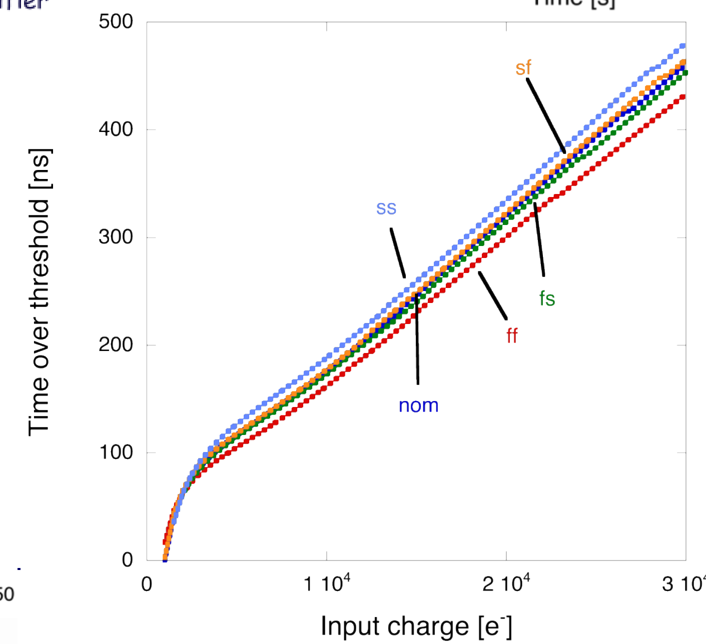


Current consumption:

3 μA in the preamp

1 – 1.5 μA in the discriminator

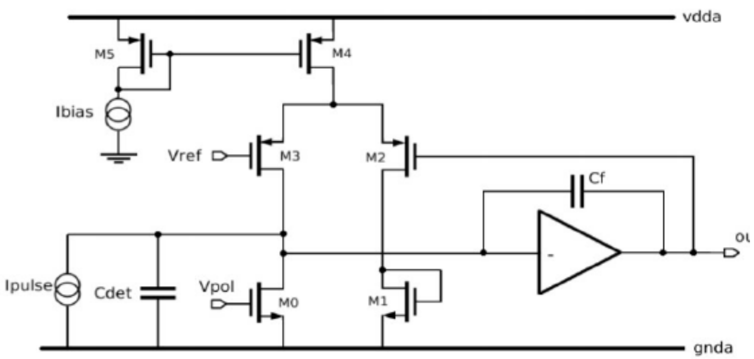




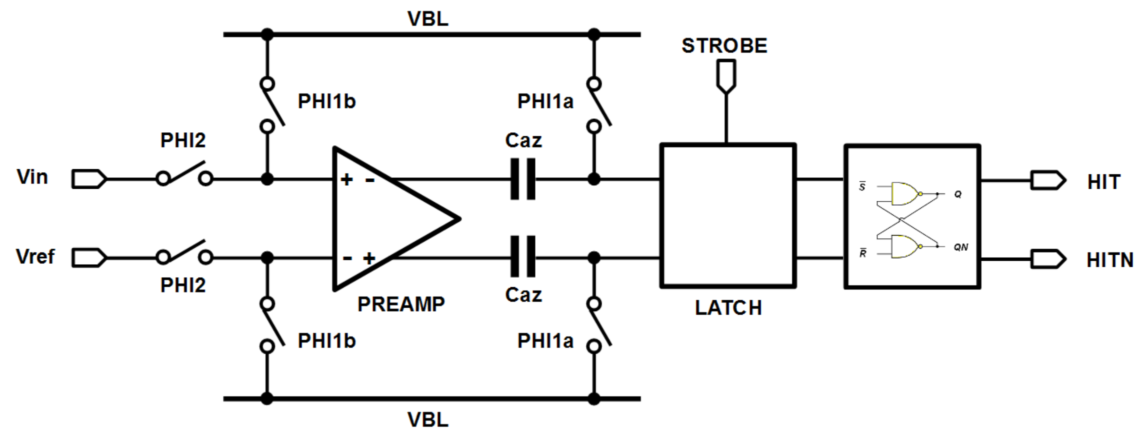
…and a synchronous one (INFN-TO)

Charge-sensitive preamplifier

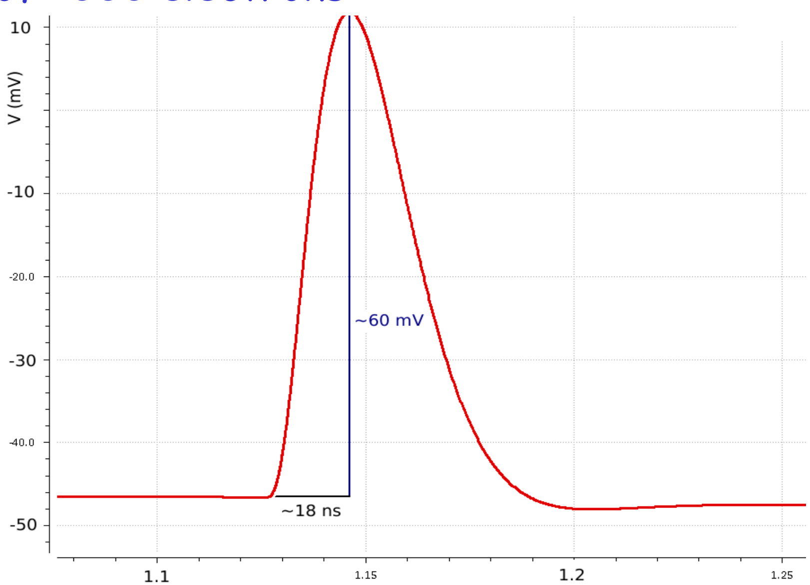
Krummenacher scheme (simplified)



Synchronous comparator



Latch input signal with input charge of 1000 electrons



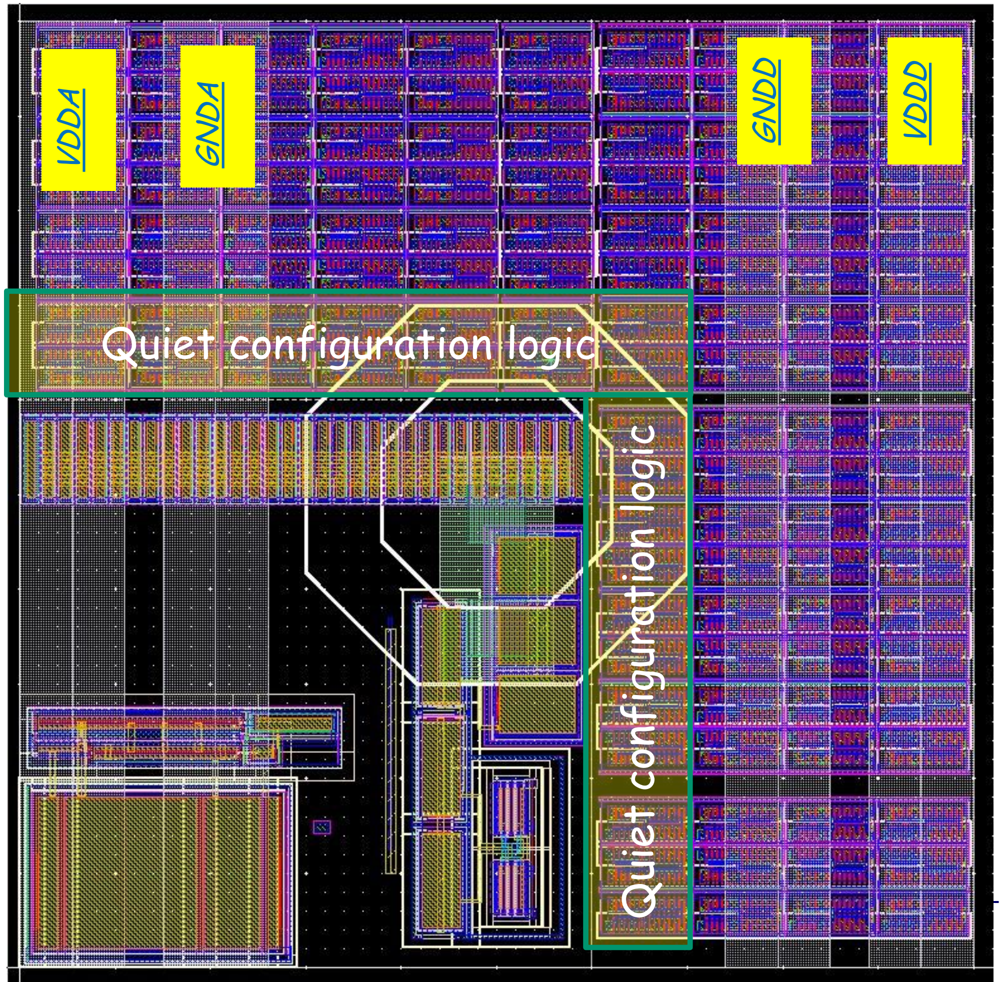
Power dissipation = 5 μW (preamp + synch-comp)

Design compatible with Fast-ToT.
Example: for Qin = 30ke$^-$, ToT = 250ns,
ENC = 110 e rms @ C_D = 100 fF

Integration of the analog readout cell in the (mostly digital) pixel matrix

- A correct layout is crucial to avoid digital interferences in the low-noise analog front-end

  - *FEI4 Bump geometry*
  - *Bias lines not shown*
  - *Needed shield under the bump not shown*
  - *Intelligent digital P/R is needed*
  - *~4000 Transistors (very rough estimate)*
  - *Front-end Pseudo real (preamp+ 5b DAC + comparator)*
  - *Work in progress*

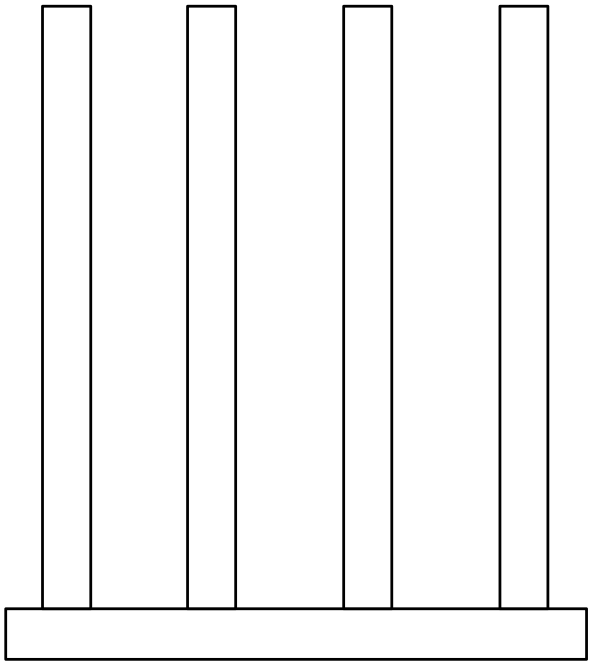


Abder Mekkaoui, RD53 Analog WG meeting

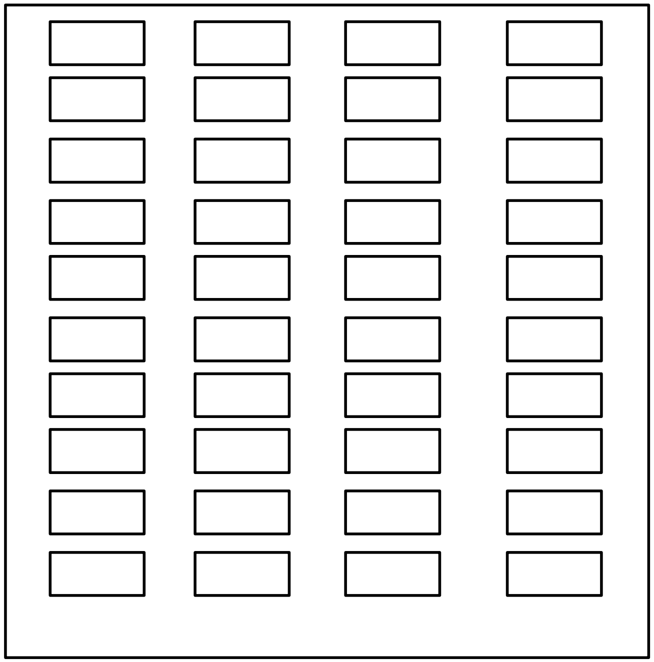
Matrix architecture: digital columns or digital cores?

- It may be best to distribute a large amount of digital logic into the pixel array and to store hits locally.
- The desire to minimize chip periphery area is likely to mean that chip design will be based on a distributed architecture as in FE-I4, which implies a tight and delicate integration with the low noise analog front-ends per pixel

Does digital array look like this?



Or like this?



Digital cores

- Just as for digital columns, digital cores can be subdivided into regions for hit and latency memory sharing.
- The core size has nothing to do with the optimum region size. The cores size has to do with
  - On-chip hit movement (bandwidth) and clock distribution
  - Power consumption
  - Layout constraints

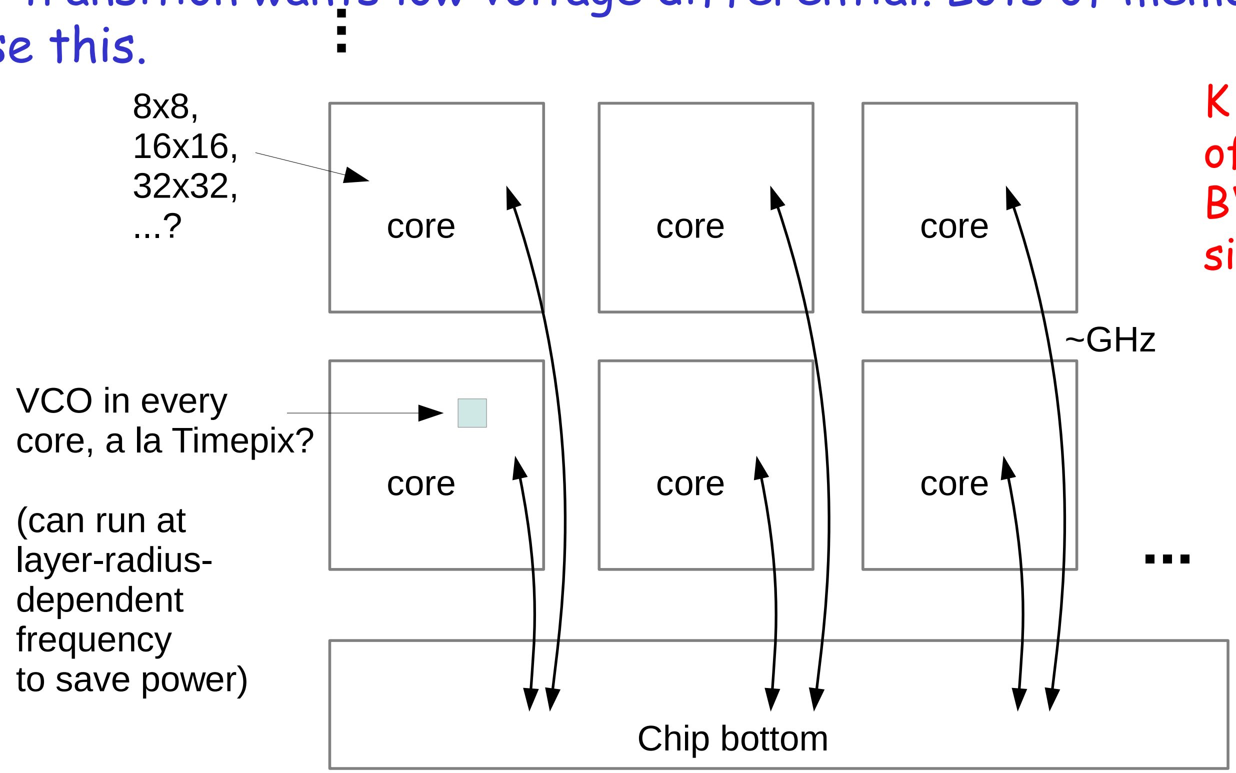
- How is each core connected to the bottom of chip?

  Point-to-point?
- What bandwidth and latency does this connection need?

  need physics simulation to understand readout efficiency vs. core BW
- Do cores talk directly to each other?
- What is the optimum core size (in pixel rows x pixel columns)?

Moving data at low power

- An important way to help low threshold may be to keep power constant
- This would imply using a DC-balanced protocol for moving data out of the cores
- So the power is constant regardless of now much data there is. This results in some parameters to optimize
- Total power in core->bottom links =
  power per transition * (chip output BW * K) * number of cores
- Low power per transition wants low voltage differential. Lots of memory/CPU applications use this.



K = fraction of chip output BW used by a single core

The RD53 collaboration

- Similar/identical requirements, same technology choice and limited availability of rad hard IC design experts in HEP makes this ideal for a close CMS – ATLAS R&D collaboration
  - Even if we do not make a common pixel chip
- Forming an R&D collaboration has attracted additional groups and collaborators
  - Synergy with CLIC pixel (and others): Technology, Rad tol, Tools, etc.
- RD53 collaboration recommended by LHCC June 2013
  - Institutes: 19
    - ATLAS: CERN, Bonn, CPPM, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Prague, RAL, UC Santa Cruz.
    - CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Torino.
  - Collaborators: ~100, ~50% chip designers
  - Collaboration organized by Institute Board (IB) with technical work done in specialized Working Groups (WG)
  - Initial work program covers ~3 years to make foundation for final pixel chips
  - Co-spokespersons: ATLAS: M. Garcia-Sciveres, LBNL. CMS: J. Christiansen, CERN
- RD53 web (new): www.cern.ch/RD53/

RD53 working groups

WG	Domain
WG1	Radiation test/qualification: M. Barbero, CPPM
	Coordinate test and qualification of 65nm for 1Grad TID and10^{16} neu/cm^2 Radiation tests and reports. Transistor simulation models after radiation degradation Expertise on radiation effects in 65nm
WG2	Top level: (M. Garcia-Sciveres, LBNL)
	Design Methodology/tools for large complex pixel chip Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization.
WG3	Simulation/verification framework: T. Hemperek, Bonn
	System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells
WG4	I/O : To be started
	Development of rad hard IO cells (and standard cells if required) Standardized interfaces: Control, Readout, etc.
WG5	Analog design / analog front-end: V. Re, Bergamo/Pavia
	Define detailed requirements to analog front-end and digitization Evaluate different analog design approaches for very high radiation environment. Develop analog front-ends
WG6	IP blocks: (J. Christiansen, CERN)
	Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, , Distribute design work among institutes Implementation, test, verification, documentation

IP blocks

- **IP block matrix: ~30 IPs** distributed across RD53 institutes

- Analog

temperature and radiation sensor, bandgap reference, analog buffers,…

- Mixed-signal and digital

biasing DAC, monitoring ADC, PLL, serializer,SRAM for pixel, SRAM for end-of-column, low-power clock driver/receiver, I/O cells, SLVS drivers, bond pads, LDO, DC-DC,…

Status and plans

- General
  - MOU in the pipeline
  - Some institutes have obtained funding thanks to RD53 (justified by the fact that it is for ATLAS & CMS)
  - First collaboration workshop: April 10-11 at CERN
  - **Define schedule for shared IC runs.**
- **Radiation: Urgent**
  - **Verify that 65nm is OK,** Evaluate alternatives (2014)
  - Radiation test campaigns have started
  - Simulation models after radiation (2015)
- **Analog**
  - Defining requirements
  - Defined alternative schemes to be evaluated: TOT, ADC, Auto-zero, Sync – Async, etc.
  - Design/test different implementations and choose (2015)
- **IPs: ~30 IP blocks**
  - Defined who makes what.
  - Define detailed specs, how to make/deliver IPs, start design (2014)
  - IP library with layouts, simulation models, documentation, , , , (end 2015)
- **Simulation:**
  - Defining simulation tool (SV + UVM), bench mark, Framework definition
  - Simulate different architectures and optimize
  - SEU immunity verification
- **Top: How to put such a chip together**
  - Global aspects: Metal stack, Mixed signal, Power distribution, Global integration, Bump-bonding pattern, ,
- **IO: To be started**

Conclusions

- Highly focused ATLAS-CMS-LCD/CLIC R&D collaboration to develop/qualify technology, tools, architecture and building blocks required to build next generation pixel chips for very high rates and radiation
- Synergy with other pixel projects when possible
- Centered on technical working groups
- Baseline technology: 65nm
  - CERN frame contract/NDA/design kit .
- 19 Institutes, 100 Collaborators
- Initial work program of 3 years
  - First round of submissions in 2014
  - Goal: Full pixel chip prototype 2016/2017
  - Working groups have gotten a good start.
  - Common or differentiated final chips to be defined at end of 3 year R&D

Backup slides

RD53 plans

- 2014:
  - Release of CERN 65nm design kit: Very soon !
  - Detailed understanding of radiation effects in 65nm
    - Radiation test of few alternative technologies.
    - Spice models of transistors after radiation/annealing
  - IP block responsibilities defined and appearance of first FE and IP designs/prototypes
  - Simulation framework with realistic hit generation and auto-verification.
  - Alternative architectures defined and efforts to simulate and compare these defined
  - Common MPW submission 1: First versions of IP blocks and analog FEs
- 2015:
  - Common MPW submission 2: Near final versions of IP blocks and FEs.
  - Final versions of IP blocks and FEs: Tested prototypes, documentation, simulation, etc.
  - IO interface of pixel chip defined in detail
  - Global architecture defined and extensively simulated
  - Common MPW submission 3: Final IPs and Fes, Small pixel array(s)
- 2016:
  - Common **engineering run**: Full sized pixel array chip.
  - Pixel chip tests, radiation tests, beam tests , ,
- 2017:
  - Separate or common ATLAS – CMS final pixel chip submissions.

IP blocks

Country	DE		FR	NL	IT - INFN						US	FR	UK	US	CZ	Comments			
Group	Bonn	CERN	CPPM	NIKHEF	Bari	Pav/ Berg	(Milano)	Padova	Pisa	Torino	LBNL	LPNHE	RAL	Santa Cruz	(Prague)				
ANALOG: Coordination with analog WG																			
Temperature sensor.			O			(P)				(P)					(P)				
Radiation sensor			(P)			(P)				O ?					(P)				
HV leakage current sensor.			O							(P)					(P)				
Band gap reference		O	O	(P)		O							(P)			3 Groups			
Self-biased Rail to Rail analog buffer	(P)		(P)	(P)									O		(P)				
MIXED																			
8 – 12 bit biasing DAC		(P)			O										(P)				
10 - 12 bit slow ADC for monitoring		O	O		O											3 Groups			
PLL for clock multiplication	O	(P)		(P)				(P)	(P)	(P)			(P)	(P)		Together			
High speed serializer (~Gbit/s)	O	(P)		(P)					(P)				(P)	(P)					
(Voltage controlled Oscillator)				(P)				O	(P)	(P)						Needed ?			
Clock recovery and jiter filter	O	(P)							(P)				(P)						
Programmable delay	O	(P)							(P)				(P)						
DIGITAL																			
SRAM for pixel region	(P)	(P)					O							(P)					
SRAM/FIFO for EOC.	(P)	(P)					(P)		(P)					O					
EPROM/EFUSE	(P)	O	(P)																
DICE storage cell / config reg	(P)		O				(P)		(P)					(P)		Or TMR ?			
LP Clock driver/receiver	(P)					O							(P)						
(Dedicated rad hard digital library)	(P)	(P)	(P)						O			(P)	(P)			If needed			
(compact mini digital library for pixels)	(P)	(P)	(P)						O			(P)	(P)			If needed			
IO: Coordination with IO WG																			
Basic IO cells for radiation	(P)	O																	
Low speed SLVS driver (<100MHz)	(P)	(P)				O			(P)	(P)					(P)				
High speed SLVS driver (~1Gbits/s)	(P)	(P)				O			(P)	(P)					(P)	Together			
SLVS receiver	(P)	(P)				O			(P)						(P)				
1Gbits/s drv/rec cable equalizer																New			
C4 and wire bond pads	(P)	O																	
(IO pad for TSV)	O		(P)									(P)		(P)					
Analog Rail to Rail output buffer	O		(P)									(P)		(P)					
Analog input pad	O											(P)							
POWER																			
LDO(s)		(P)	(P)	O					(P)	(P)			(P)						
Switched capacitor DC/DC		(P)									O				(P)				
Shunt regulator for serial powering				O															
Power-on reset																New			
Power pads with appropriate ESD	(P)	O																	
SOFT IP: Coordination with IO WG																			
Control and command interface		(P)			(P)				O			(P)							
Readout interface (E-link ?)		(P)			(P)				O			(P)							
Summary																			
ATLAS/CMS/Neutral	A	N	A	A	C	C	C	C	C	C	A	A	N	A	A		ATLAS	CMS	Neutral
O's	7	6	5	2	2	5	1	1	4	1	1		1	1			16	14	7
(P)'s	14	16	8	5	2	2	2	1	10	7		7	9	6	9		49	24	25