QIE10-11 Readout Chip Development

T. Zimmerman

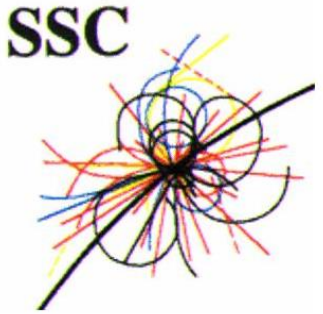
Fermi National Accelerator Laboratory

FEE 2014

Argonne National Laboratory

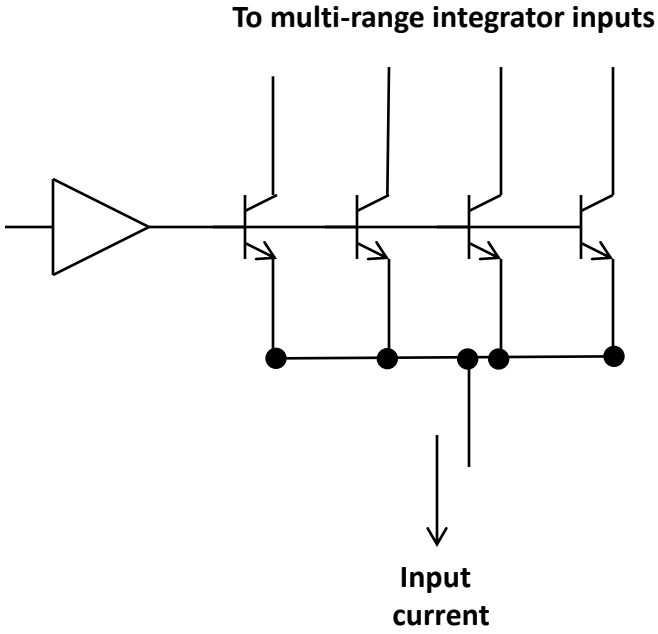
May 20, 2014

Overview of multi-decade QIE development



- The QIE [Charge (**Q**) **I**ntegrator and **E**ncoder] is a custom ASIC designed to **digitize wide dynamic range charge signals** from photo-detectors (PMTs, SiPMs), with approximately constant resolution and **no deadtime**
- A short history:
  - 1989: Originally conceived by Bill Foster for **SDC @ SSC**
  - 1995: 1st fully-functional chip designed by **Tom Zimmerman** for the **KTeV experiment @ FNAL (QIE5)**
    - 2 μm Orbit "Bi-CMOS", 3000 ch.
  - 1996: Front-end for calorimeters of **CDF @ FNAL (QIE6)**
    - 2 μm Orbit "Bi-CMOS", 10,000 ch.
  - 2002: Front-end for **MINOS Near Detector @ FNAL (QIE7)**
    - 2 μm Orbit "Bi-CMOS", 10,000 ch.
  - 2003: Front-end for **CMS HCAL @ CERN (QIE8)**
    - 0.8 μm AMS BiCMOS, 10,000 ch. .
  - 2004: Front-end for **BTEV @ FNAL** (cancelled) **(QIE9)**
    - 0.8 μm AMS BiCMOS
  - 2013-14: Front-end for **CMS** forward calorimeter **(QIE10)**
    Barrel and endcap calorimeters **(QIE11)**
    - 0.35 μm AMS SiGe BiCMOS

All QIE chips are based on the NPN bipolar current splitter concept:



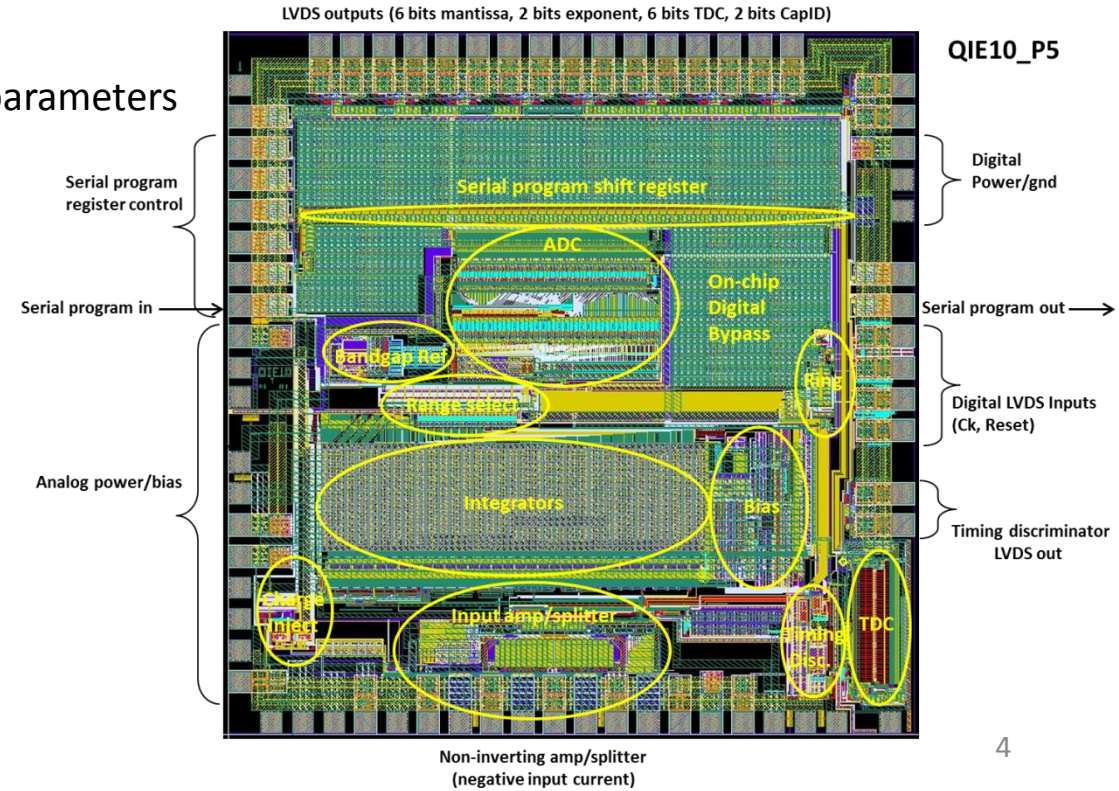
The current split ratios are determined by NPN emitter area ratios (using multiples of a unit transistor).

Split ratios remain constant over a big dynamic range, even in the presence of mismatch (not true for MOS)!

Therefore, all QIE chips are realized using a BiCMOS process.

Overview of QIE10

- The newest design (**QIE10**) features:
  - Dead-timeless operation @ 40 MHz, using 4-phase operation (same as all previous QIEs)
  - High dynamic range: 3 fC – 330 pC (~17 bits). 6-bit mantissa, 4 Ranges → 256 codes (10X the range of QIE8)
  - Logarithmic response - ~1% measurement across dynamic range
  - Controlled impedance input over full dynamic range (5 meter input cable from PMT)
  - 6 bit TDC (0.5 ns) with programmable threshold (first QIE with a TDC)
  - Serial download of programmable parameters (new feature)
  - True LVDS outputs
  - On-chip test charge injection
  - Low power: 320 mW
    - +5V @ 40 mA analog
    - +3.3V @ 35 mA digital
  - 350 nm AMS SiGe process (first QIE to use this process)



Overview of QIE11

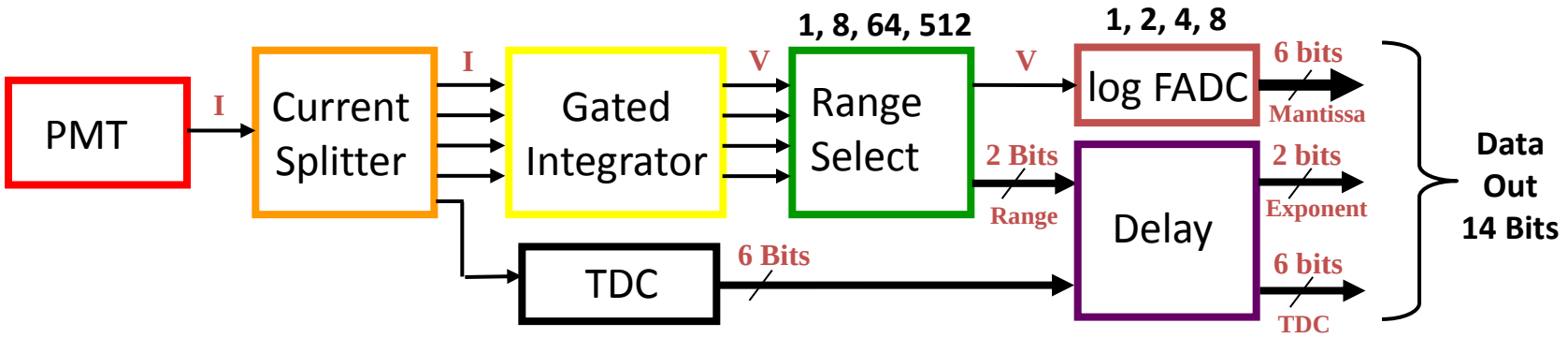
- Similar to QIE10 with the following differences:
  - Intended for SiPM readout
  - Programmable input current shunt to achieve scaling factors of:

    x1, x1.5, x2, x3, x4, x6, x8, x12 (in order to accommodate higher than anticipated SiPM gain)
  - Lowest possible input impedance (not constant, impedance naturally goes down as signal magnitude goes up)

- How the QIE10 works:
  - ✶ Receives charge (current) from PMT Anode
  - ✶ "Splits" current into four weighted ***Ranges***
  - ✶ Gates and integrates current fractions onto separate capacitors
  - ✶ Based on the signal magnitude, 1 of the 4 Ranges is selected to be digitized
    - Ranges are logarithmically weighted (X8)
  - ✶ Digitizes the analog voltage from the selected Range
    - 6-bit FADC with *logarithmic* response (bin width 1, 2, 4, 8) → *"Mantissa"*
  - ✶ Outputs 2-bit code for the Range digitized (0 - 3) → *"Exponent"*

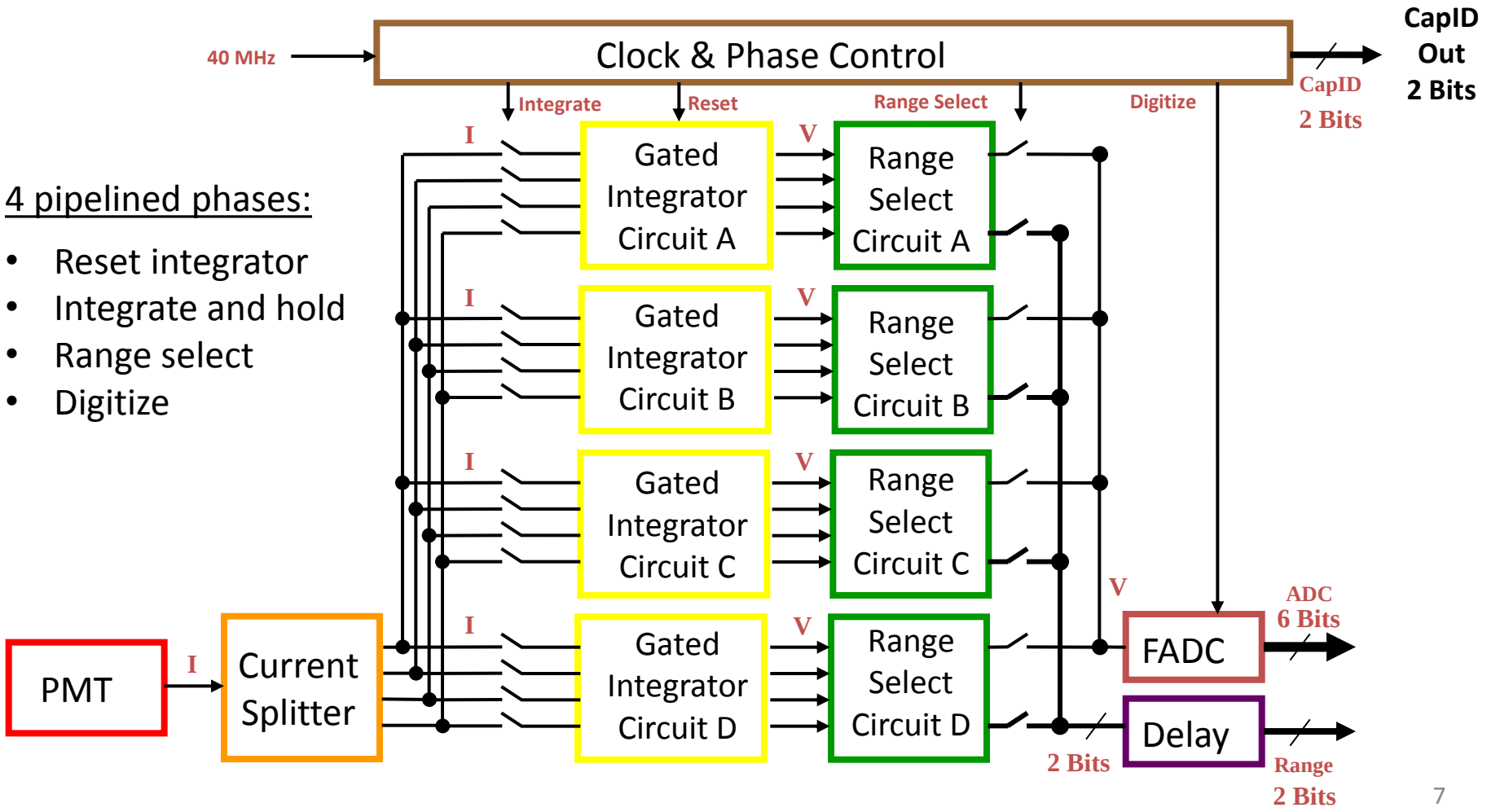
⇨ ***Produces floating-point output codes***

⇨ ***Response is approximately logarithmic…***



In reality, 4 sets of integrators (4 phases A-D) are used to achieve dead-timeless operation:

- Operations are pipelined at 40 MHz using 4-phase circuits ⇨ ***Produces a code representing the current integrated in each and every 25 ns period and never stops***
- Data includes 2-bit ***CapID*** to indicate phase



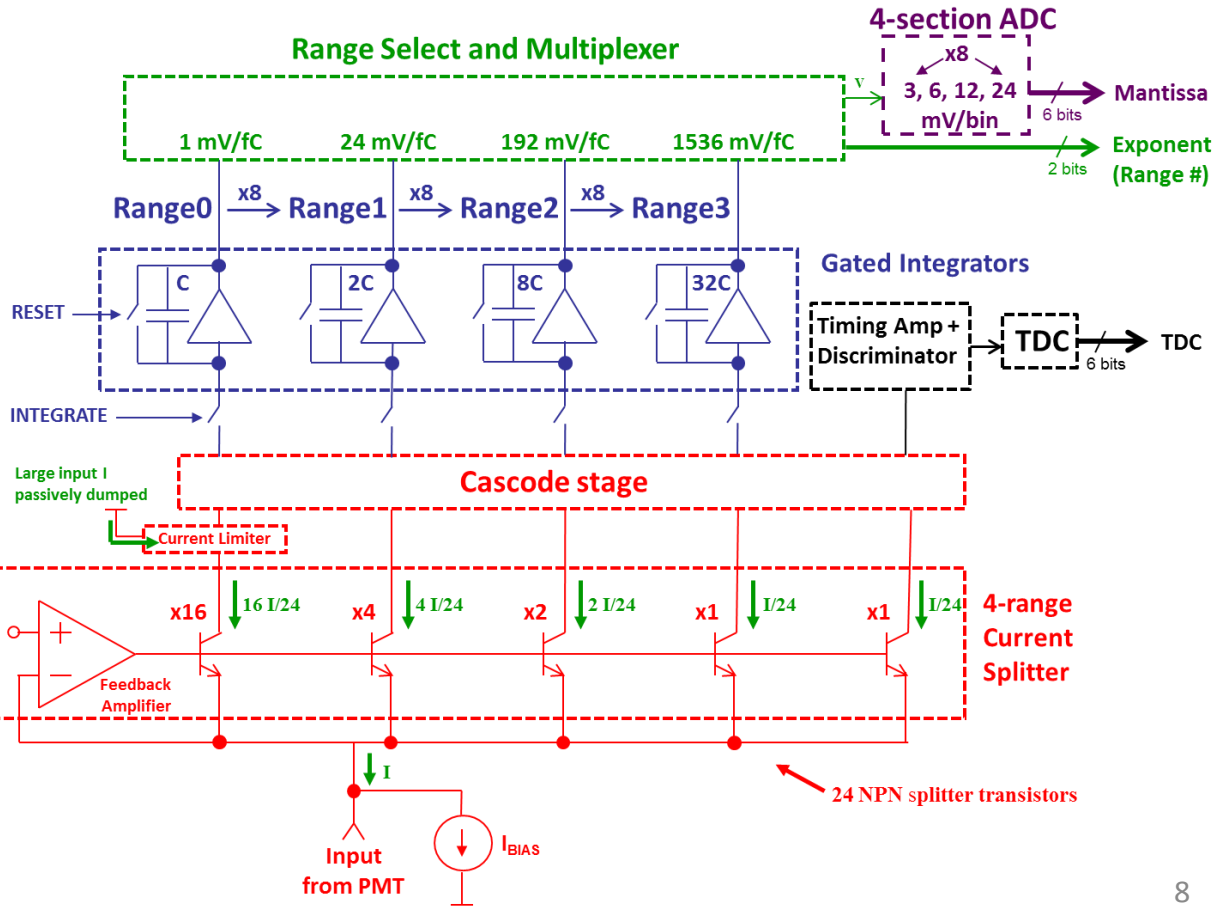
4 pipelined phases:

- Reset integrator
- Integrate and hold
- Range select
- Digitize

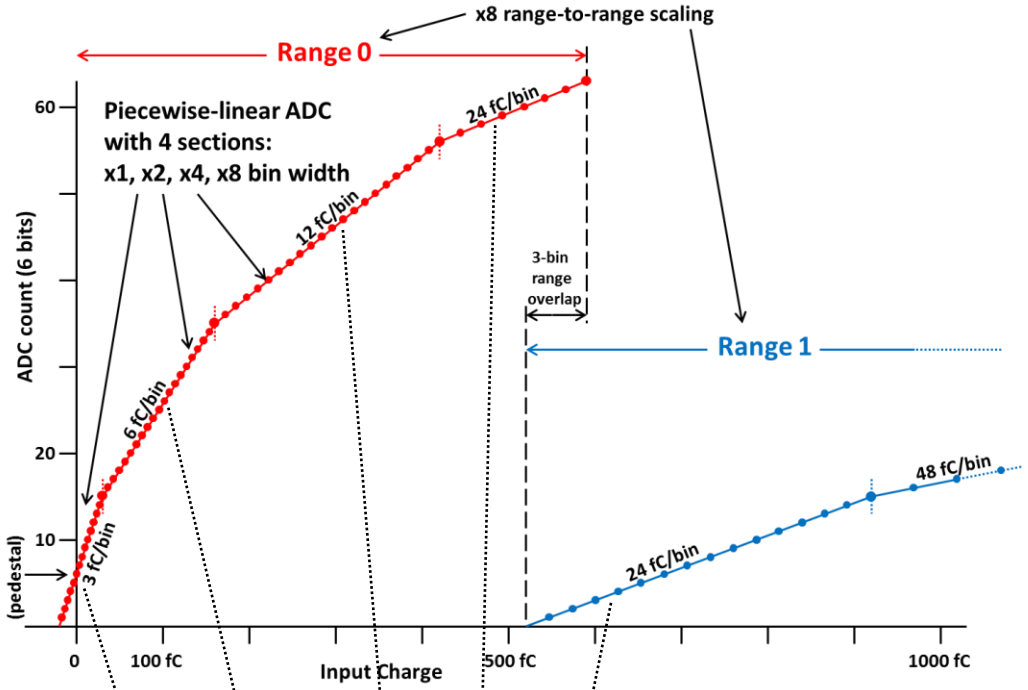
- **Splitter/integrator implementation:**
  - 24 identical NPN transistors, arranged in groups: x16, x4, x2, x1, x1
  - Integrator capacitor ratios: 1, 2, 8, 32
  - Results in 4 integration ranges, each scaled by X8
  - Selected integrator feeds a 4-section ADC with binary weighted bin widths
  - Results in effectively 16 ranges, scaled by x2

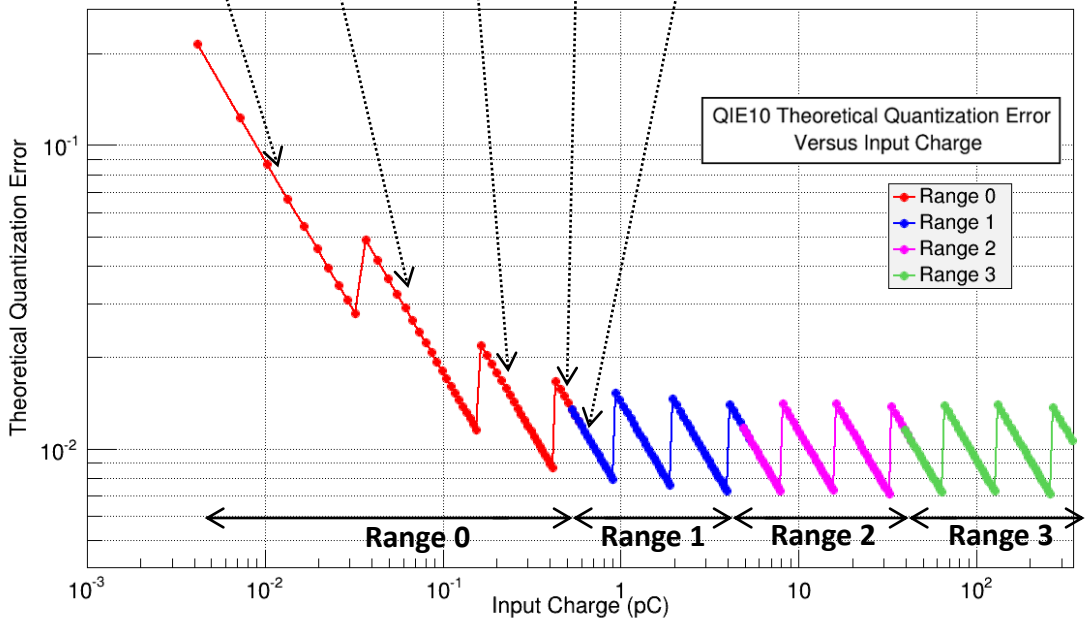
Simplified diagram:

- **Only 1 of 4 integration phases shown**
- **Shown as single-ended implementation, actually done in pseudo-differential form (shown later)**



The combination of x8 range scaling and a 4-section piecewise-linear ADC give "16-range" floating-point response:

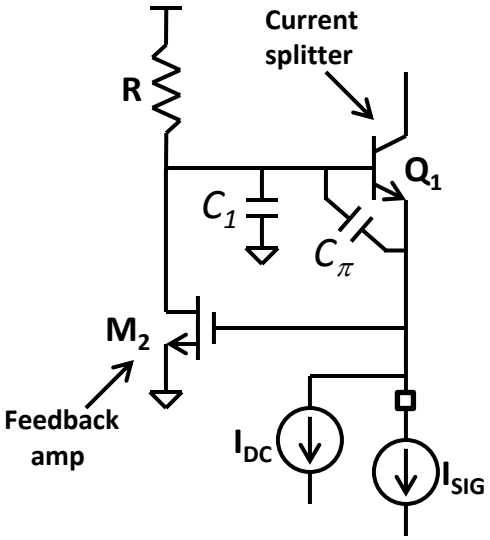




Controlled impedance input amplifier/splitter design challenges

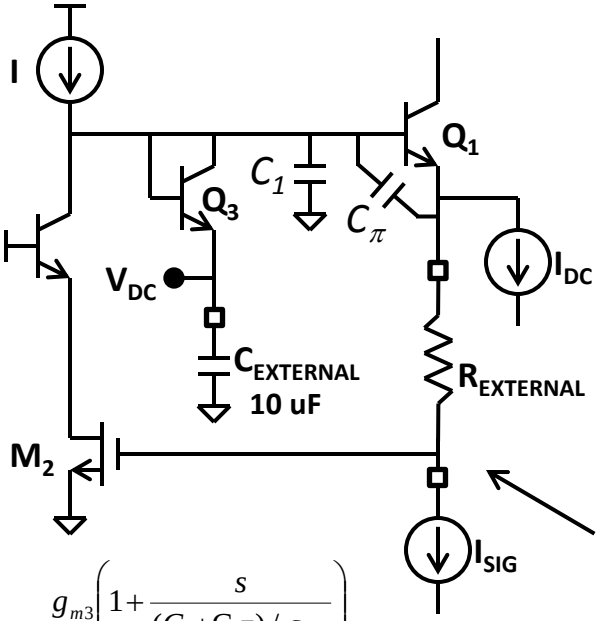
- Constant split ratio over wide dynamic range: NPN splitter required (not NMOS)
- Small DC input bias current (< 20 uA)
- Constant impedance input for 0 – 60 mA input current: *requires novel feedback amp approach*

Basic approach:



Stabilize the open-loop gain: replace R with I source and Q_3

Both g_{m1} and g_{m3} go up with I_{SIG}: R_{IN} remains constant!



$$R_{in}(s) = \frac{g_{m3}\left(1+\frac{s}{(C_1+C\pi)/g_{m3}}\right)}{g_{m1}g_{m2}\left(1+\frac{s}{C\pi/g_{m1}}\right)}$$

Small signal analysis

$$R_{in}(s) = \frac{1+\frac{s}{R(C_1+C\pi)}}{g_{m1}g_{m2}R\left(1+\frac{s}{C\pi/g_{m1}}\right)}$$

But I_{SIG} >> I_{DC} so NOT small signal!

g_{m1} goes up with I_{SIG}, so open-loop gain and R_{IN} changes with I_{SIG}!

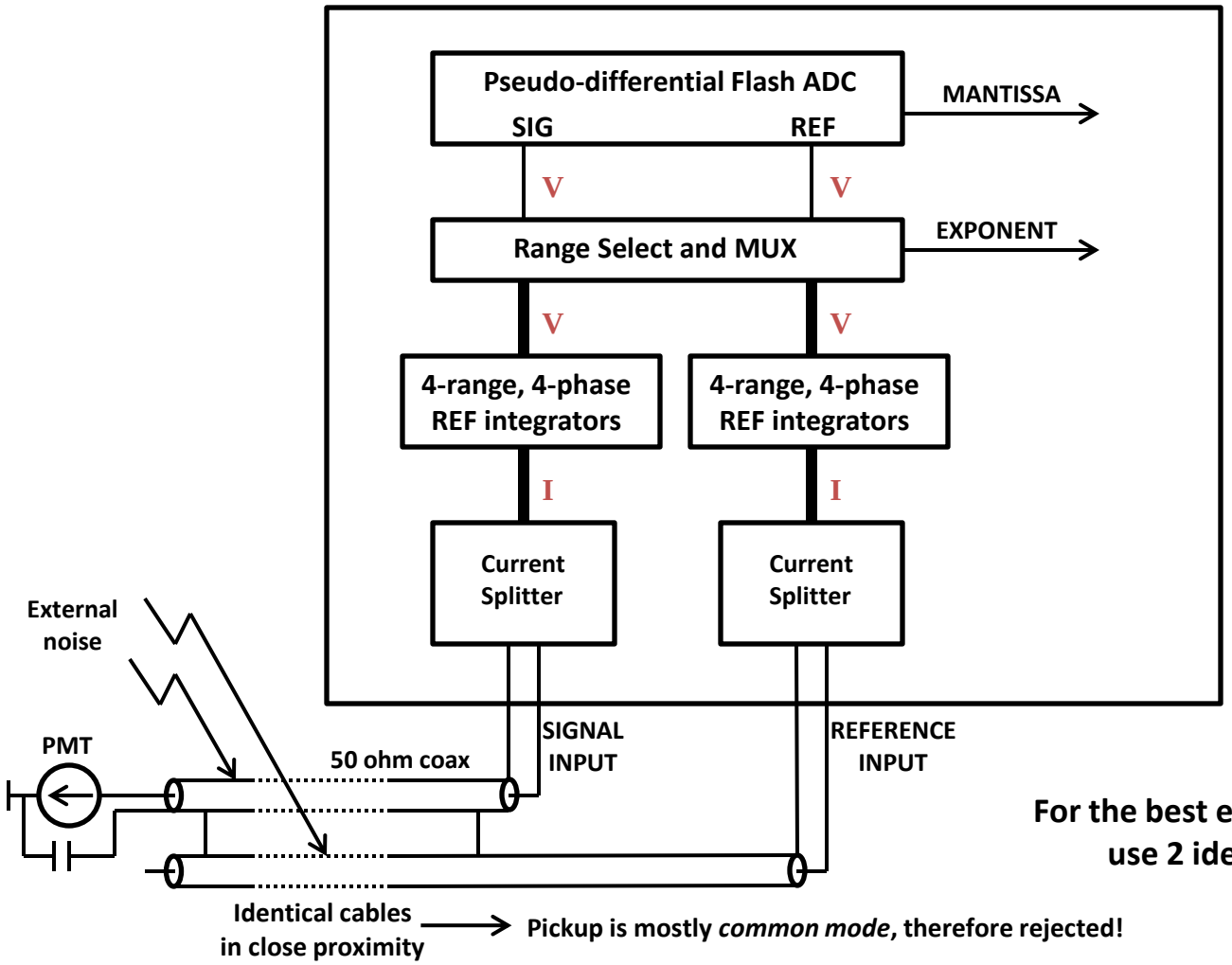
Arrange the value of C1 so the pole cancels the zero: resistive input to very high frequency!

For the biggest signals (>> 1mA), M_2 is debiased, and Q_1 functions as an open-loop common base amp, with input resistance set by $R_{EXTERNAL}$.

Tune V_{DC} and $R_{EXTERNAL}$ for R_{IN} = 20 ohms.

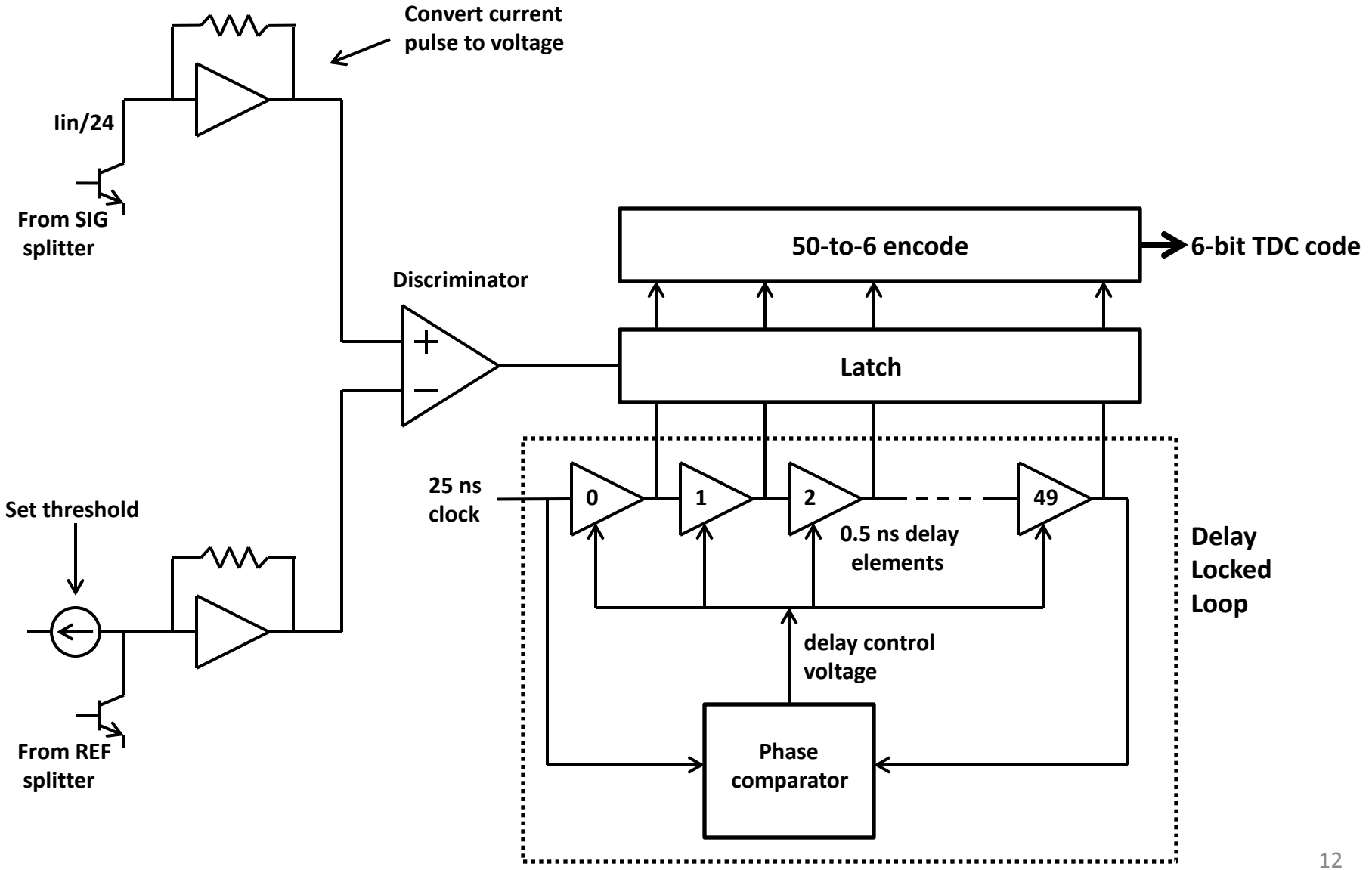
A crucial QIE strategy: **Implement all analog circuits in pseudo-differential form: 2 "identical" inputs -- signal source connects to the *SIG* input, and the *REF* input floats**

RESULT: *excellent stability and common-mode rejection*
(relatively immune to shifts in bias levels, supply voltage, clock frequency, temperature, etc.)

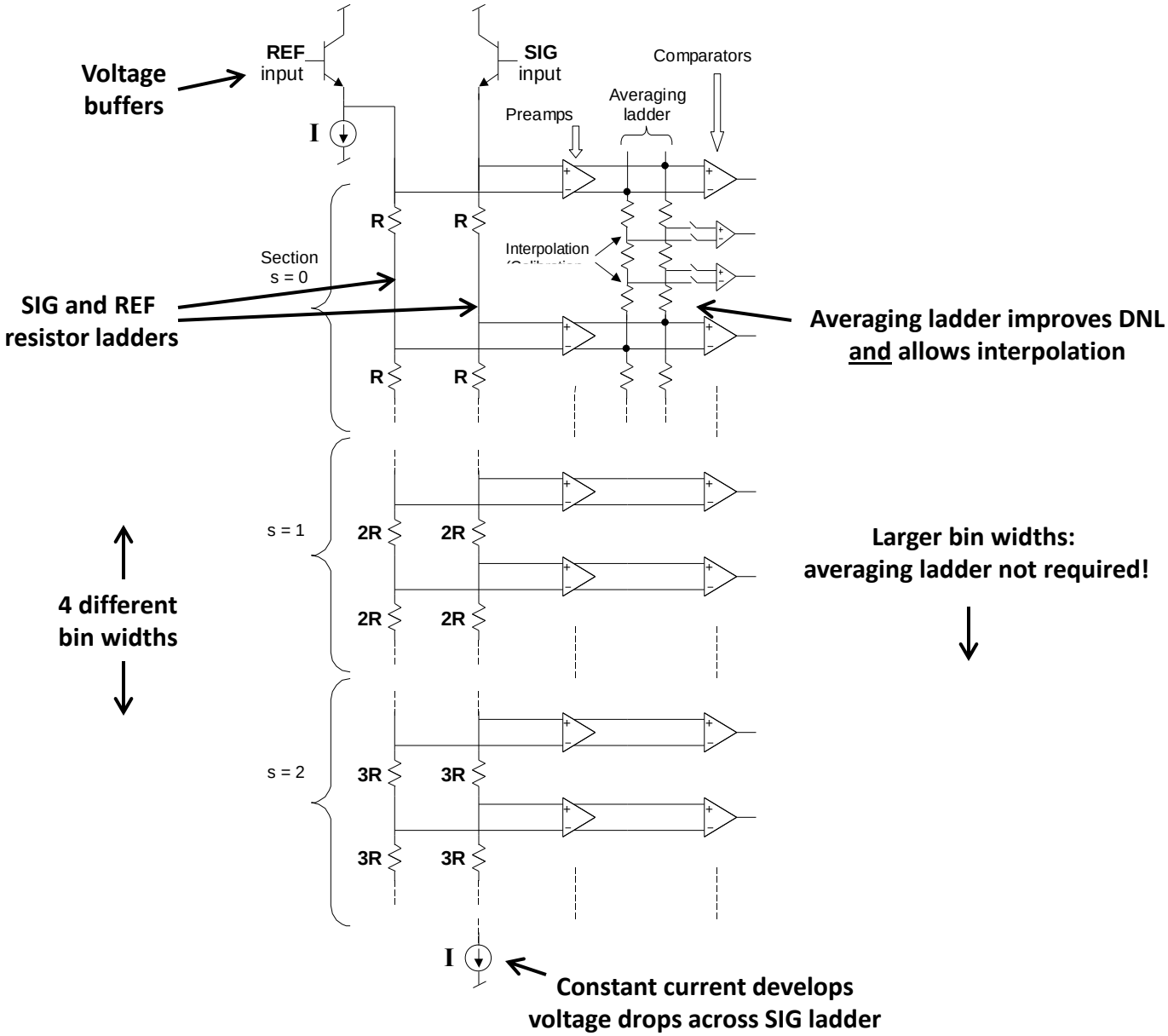


For the best external pickup rejection, use 2 identical input cables!

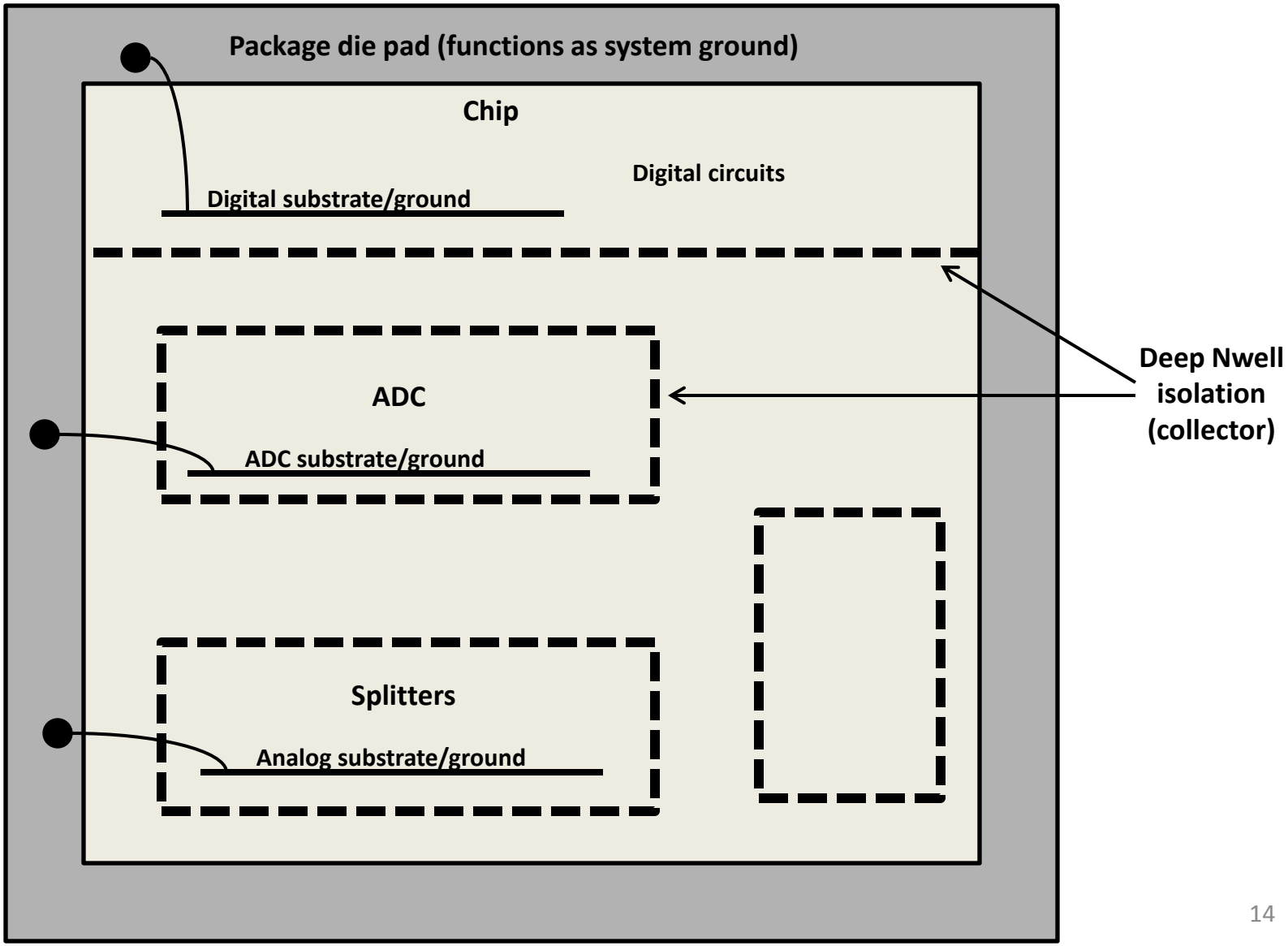
Pseudo-differential TDC implementation



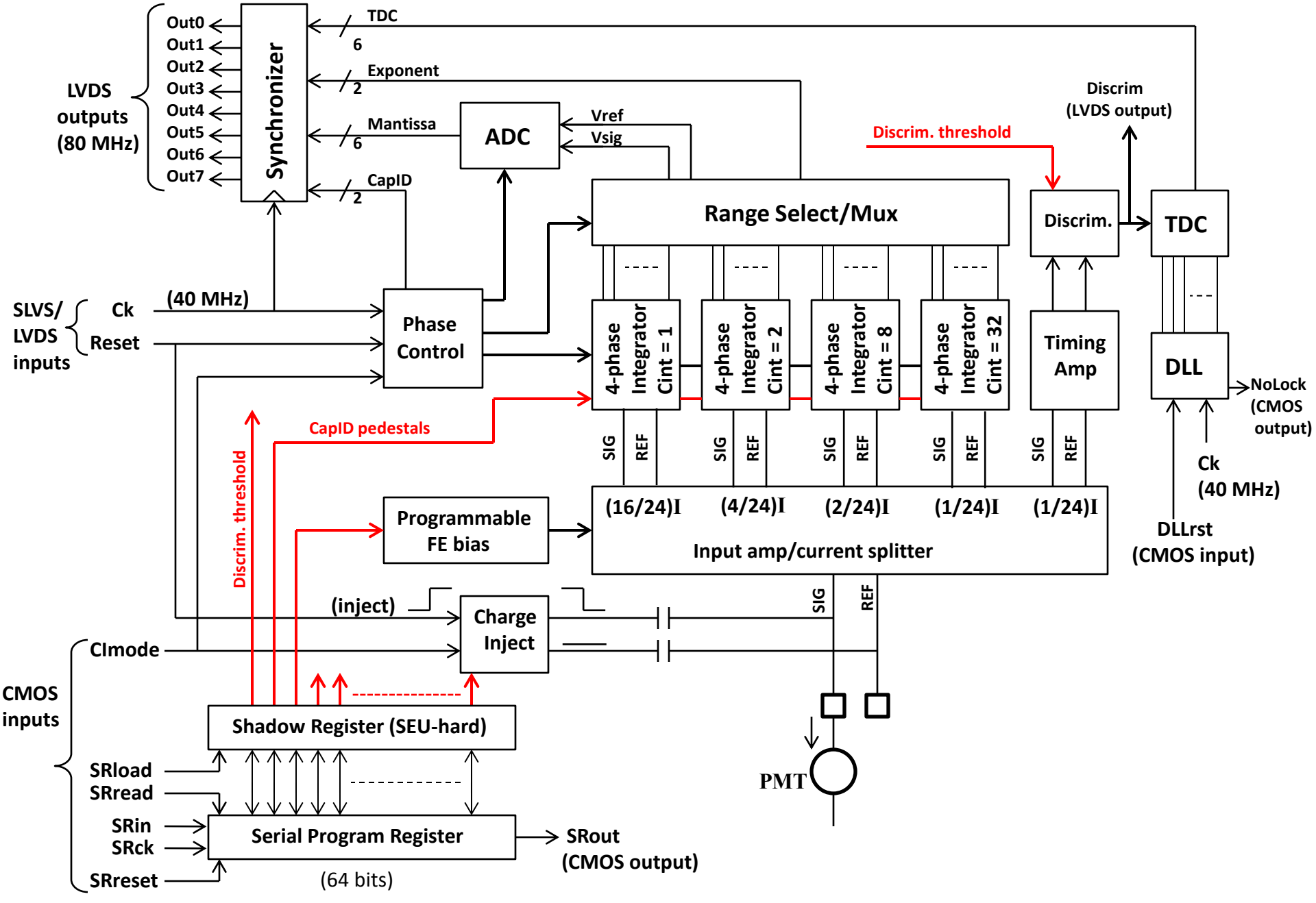
Pseudo-differential Flash ADC implementation



Another crucial QIE strategy: **Create isolated substrate areas on the same chip. Reference them all to the die pad ("system ground"). This greatly reduces digital-to-analog coupling!**

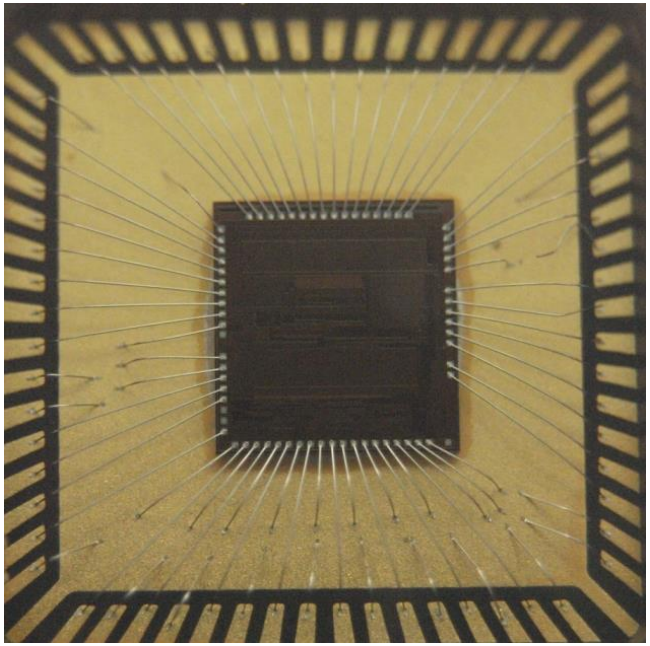


Put it all together: QIE10 full chip block diagram

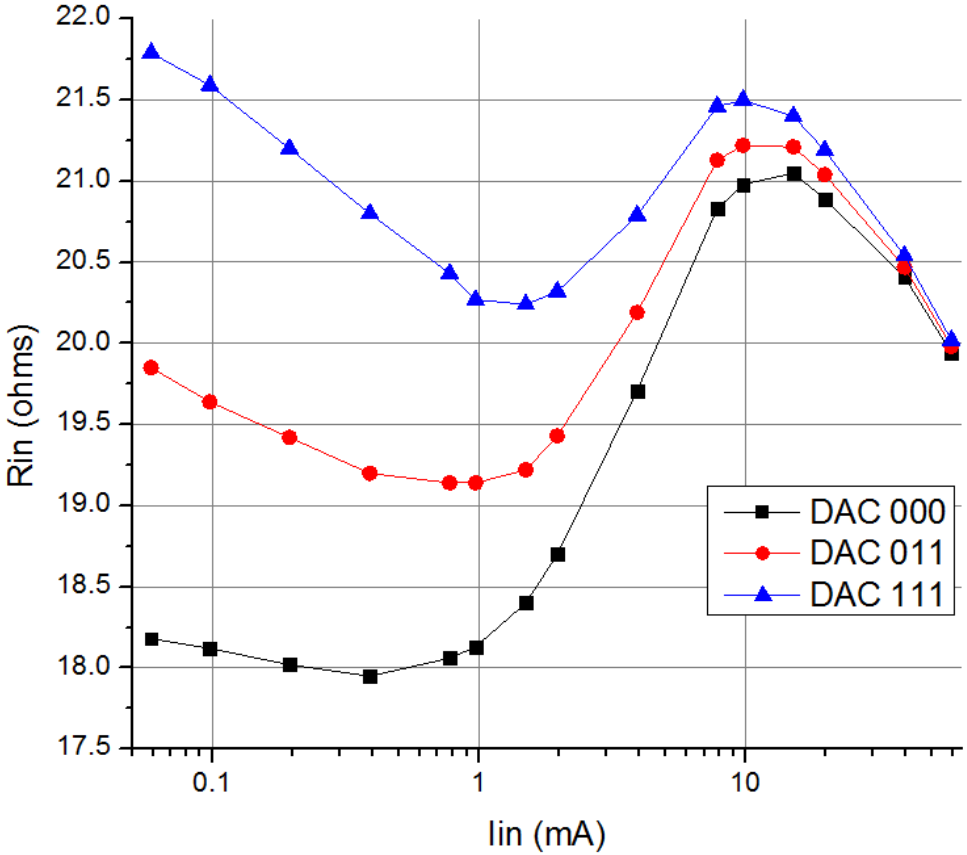


QIE10 Test Results

- **LSB = 3 fC (as expected)**
- **Input impedance stable over complete dynamic range**
- **Noise with 5 meter RG58 input cables: 1.8 fC (input referred)**
- **Noise with short (0.2 meter) RC58 input cables: 0.6 fC**
- **No change in pedestals or noise after 50 KRad TID (Cs-137 source)**
- **No SEUs in shadow register holding programmed values after 6E12 p/cm2 (230 MeV proton beam)**



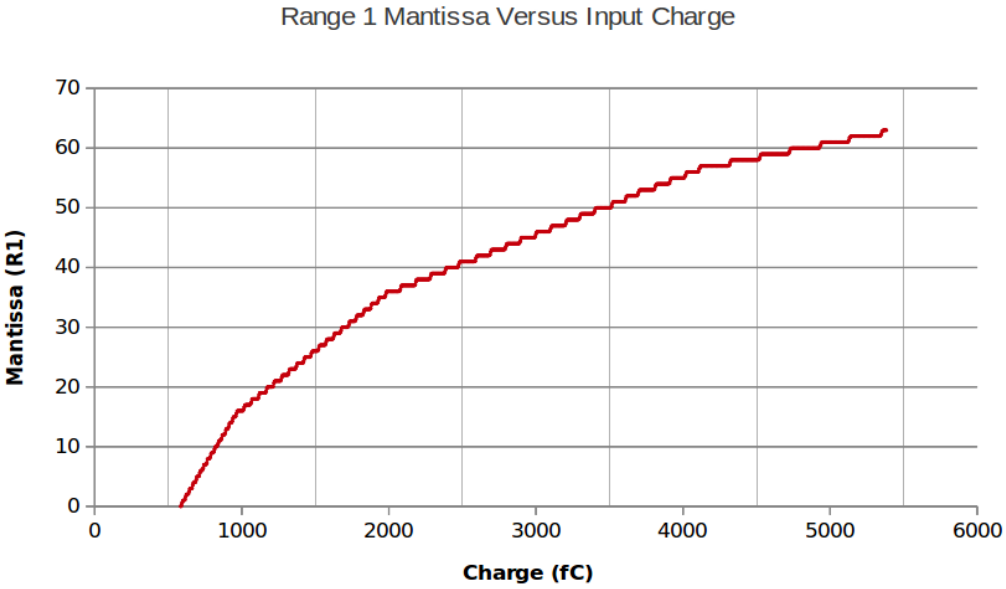
Measured QIE10 input resistance over full dynamic range



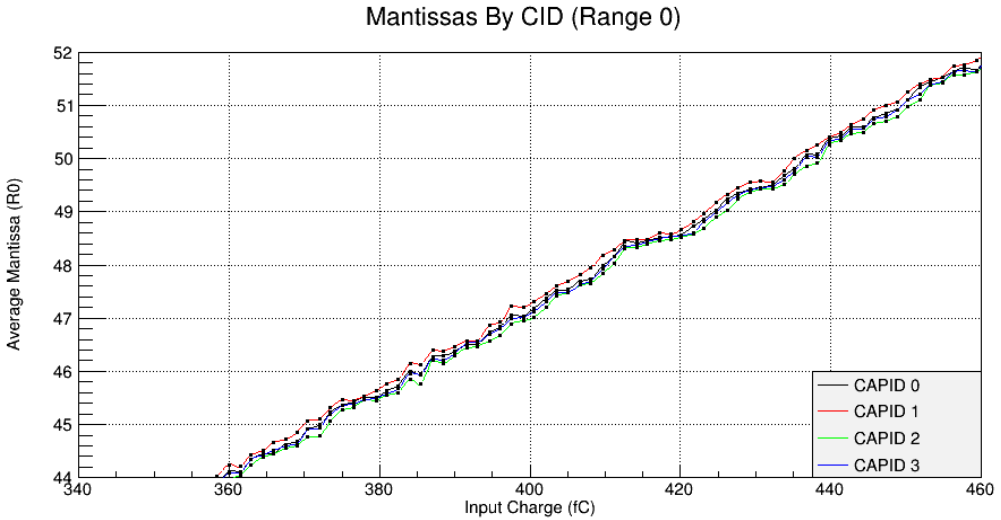
(DAC provided for tweaking of input resistance at low end)

Study ADC response on a single range:

⇨ ***Response as expected – See all 4 ADC sections***



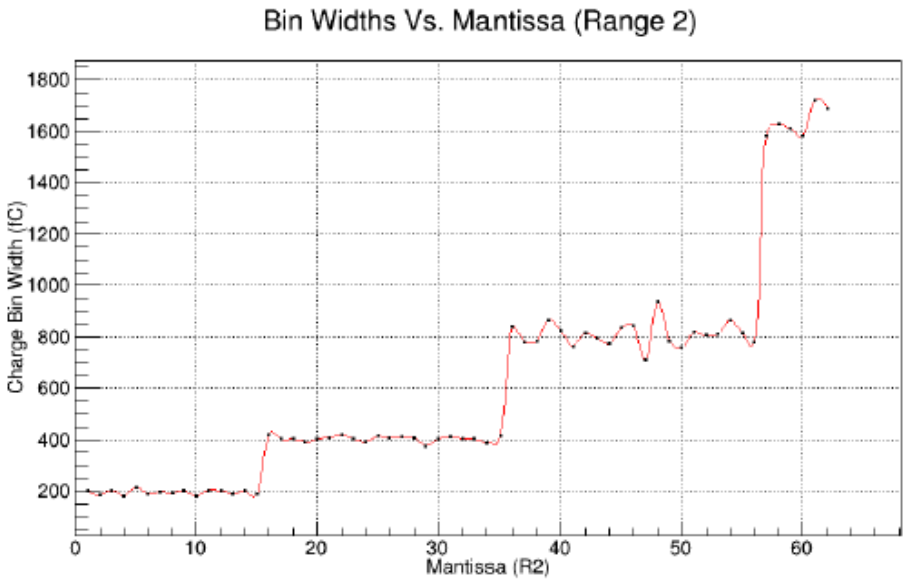
Look at uniformity across all 4 capIDs (phases) (one ADC section shown):



⇨ ***Response as expected***

⇨ ***Note: Uses capID pedestal adjust feature to make pedestals uniform***

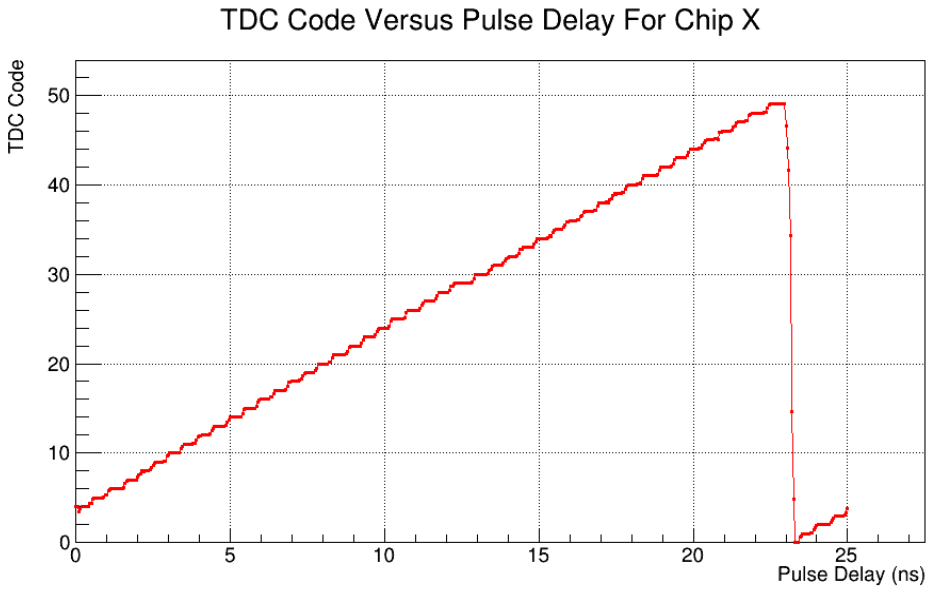
Study of bin widths in the 4-section ADC:

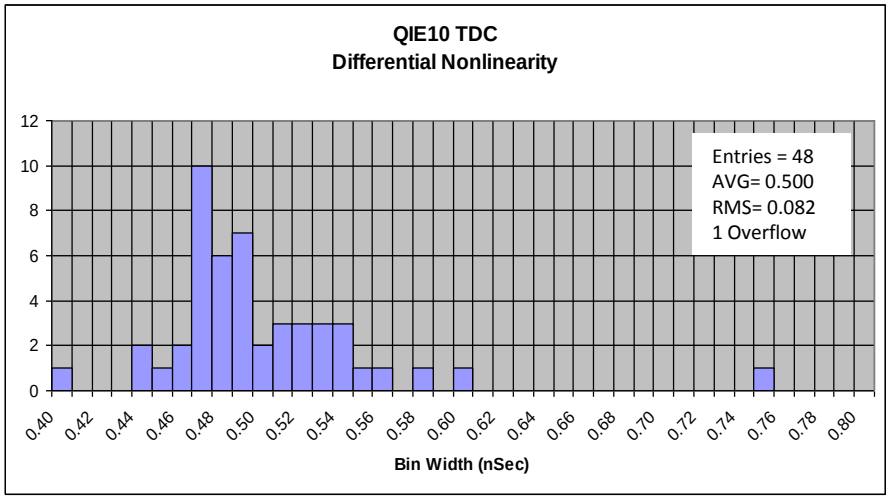


⇨ ***See nice uniform bin widths***

⇨ ***Bin width variation minimized in bottom 2 sections by design***
(small bin size requires less variation than large bin to achieve the same DNL)

- Timing Studies - TDC Response
  - Apply external input pulse (well above TDC threshold).
  - Step pulse delay by 50 ps, average 100 data points per setting





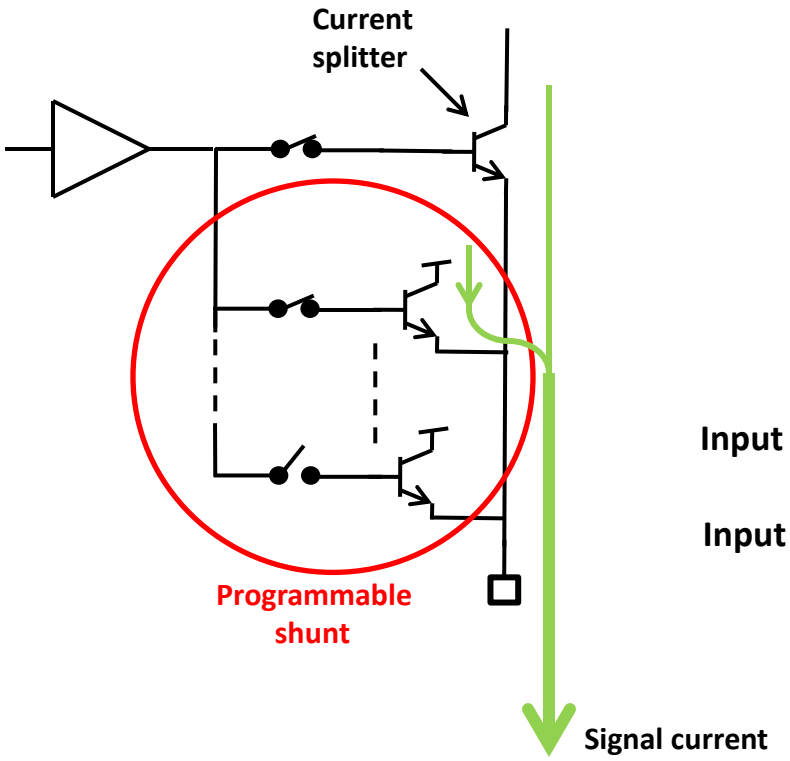
Data from Fermilab

⇨ ***See nice linear response***

⇨ ***Bin width uniformity is good: average width = 0.50 ns, DNL < 0.1 ns***

QIE11 (SiPM readout chip)

- Non-inverting input (same as QIE10)
- Current shunt provides programmable gain to accommodate big SiPM signals
- Low input impedance for big signals (remove constant impedance circuit)
- Full-chip prototype works well (x5 shunt) with only a couple of small bugs



Input resistance ~15 ohms for small signal, no shunt

Input resistance ~1 ohm for largest signal, big shunt

QIE: a success story over 25 years!

Future QIE work this year:

- **Modification of QIE11 for ATLAS: add another bit of resolution (7-bit mantissa)**
- **Quad QIE (4 per package)??**