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SI LAB Silizium Labor Bonn

Fully Depleted MAPS in Standard CMOS Technologies

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Front End Electronics 2014 - 21.05.2014

High Luminosity LHC Environment - Requirements

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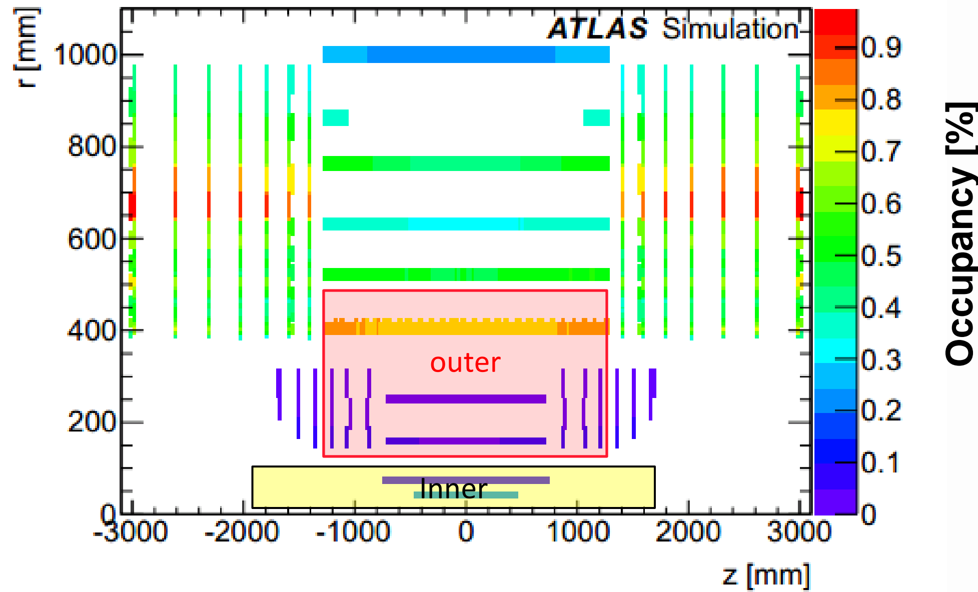

Detector:	Silicon area [m^2]	Channels [10^6]
Pixel barrel	5.1	445
Pixel end-cap	3.1	193
Pixel total	**8.2**	**638**
Strip barrel	122	47
Strip end-cap	71	27
Strip total	**193**	**74**

ATLAS Phase II Letter of Intent

Inner layer

1. **Low power**
2. **Low material**
3. Occupancy
4. Resolution

hybrid pixels (65nm? + sensor?)

Outer layer

1. **Low cost**
2. **Low power**
3. Low material
4. Resolution

low cost hybrid pixels or monolithic?

High Luminosity LHC Environment - Requirements

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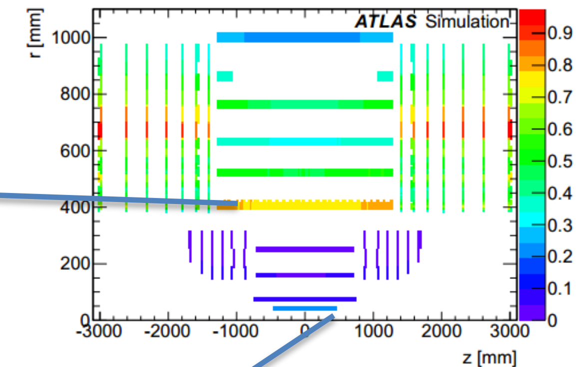

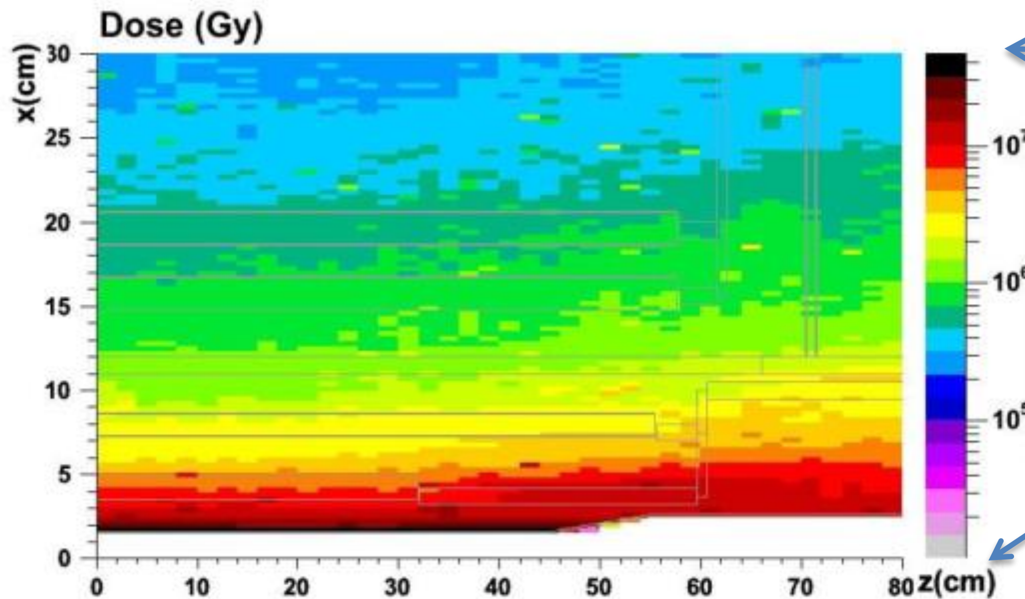

- **Radiation levels:**
  - at 5 cm : ~1500 Mrad ($2 \bullet 10^{16}$ n_{eq}/cm^2)
  - at 25cm : ~100 Mrad (10^{15} n_{eq}/cm^2)

** estimates for 10years of operations*

What are possible solutions?

Hybrid Pixel Detectors

Monolithic Pixels

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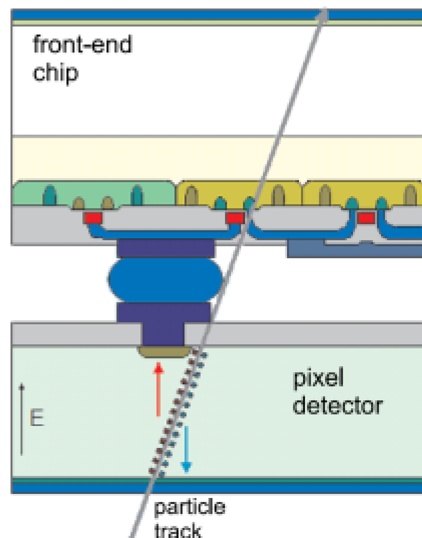

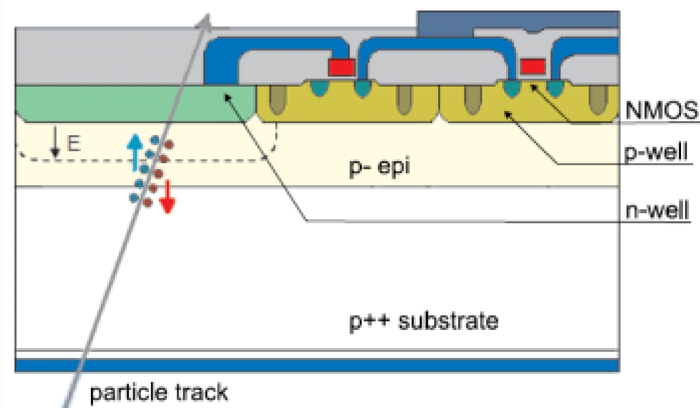

	Hybrid	Monolithic
charge collection time	**fast (drift)**	**slow (diffusion)**
cost	**high**	**low**
material	**high**	**low**
pixel size	**medium**	**small**
radiation resistance	**high**	**low/medium**
signal	**high**	**low**

Trapping in irradiated silicon

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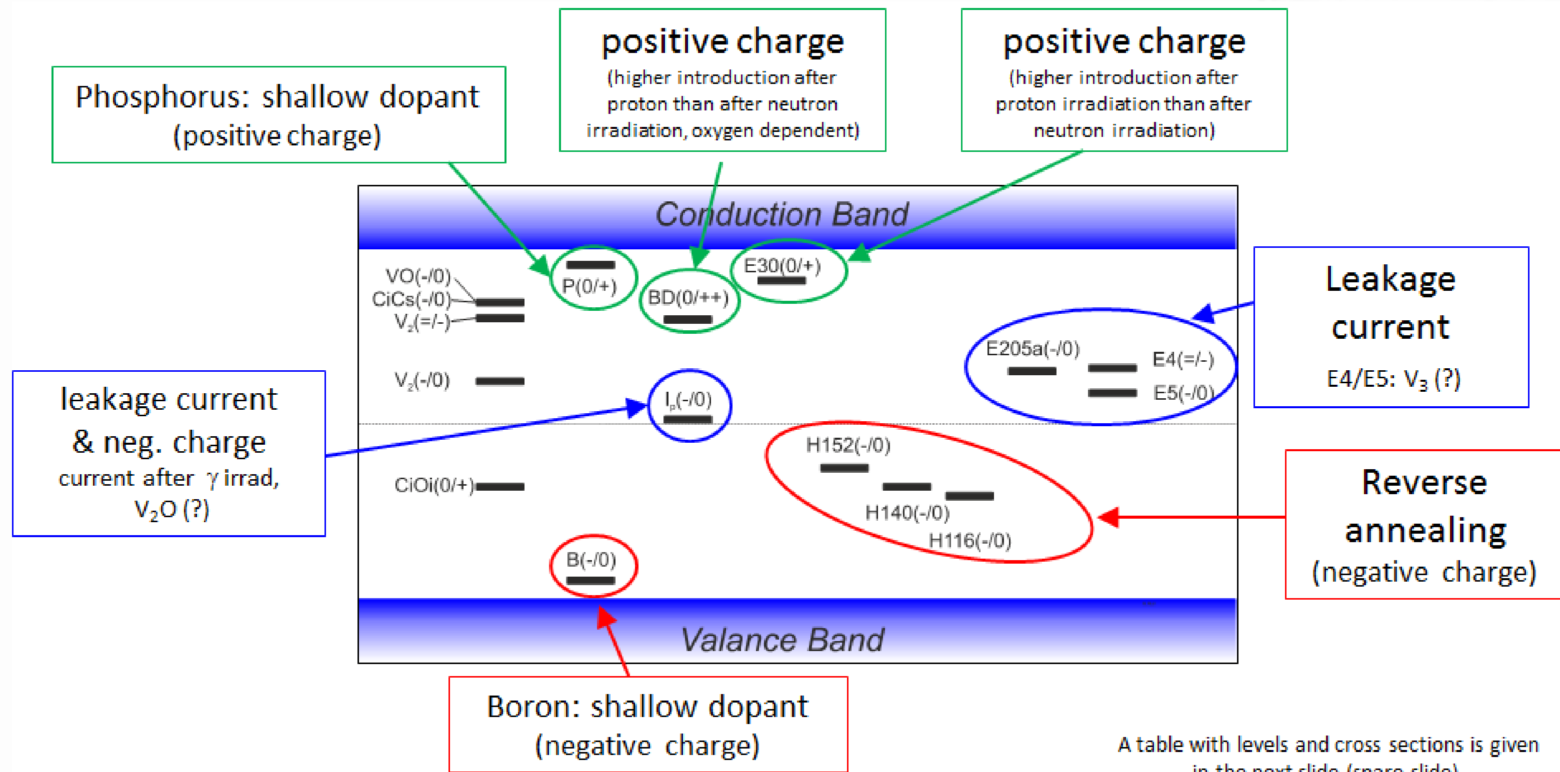
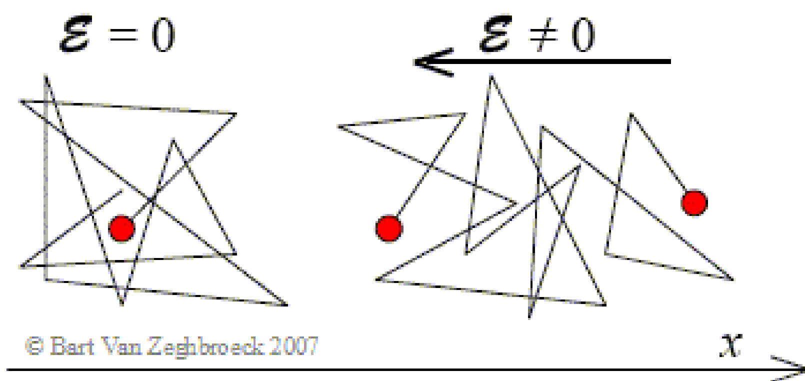


RD50

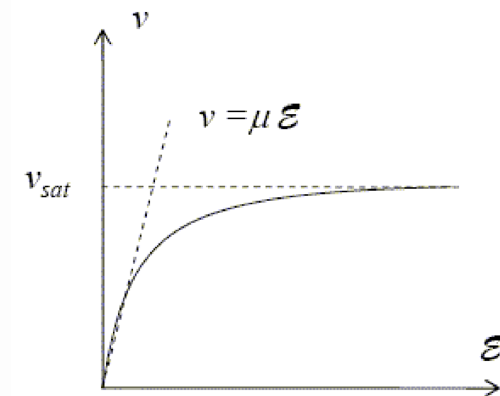
Need to be as fast as possible!

Electrical field

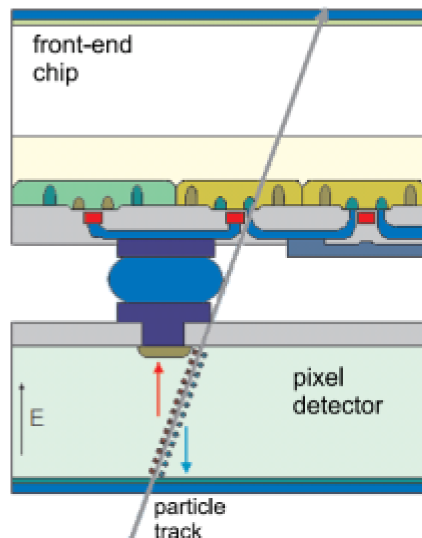
Motion of carriers



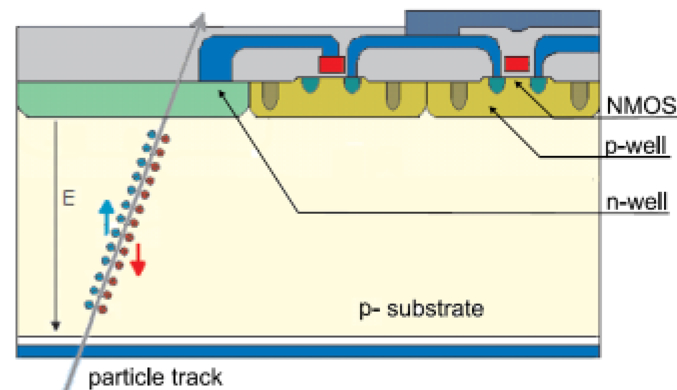
Velocity-field relation



Hybrid Pixel Detectors



Depleted Monolithic Pixels



	Hybrid	Depleted Monolithic
charge collection time	**fast**	**~~mainly diffusion~~ fast**
cost	**high**	**low**
material	**high**	**low**
pixel size	**medium**	**small**
radiation resistance	**high**	**~~low/medium~~ high**
signal	**high**	**~~low~~ high**

Charge Collection in Depletion Layer

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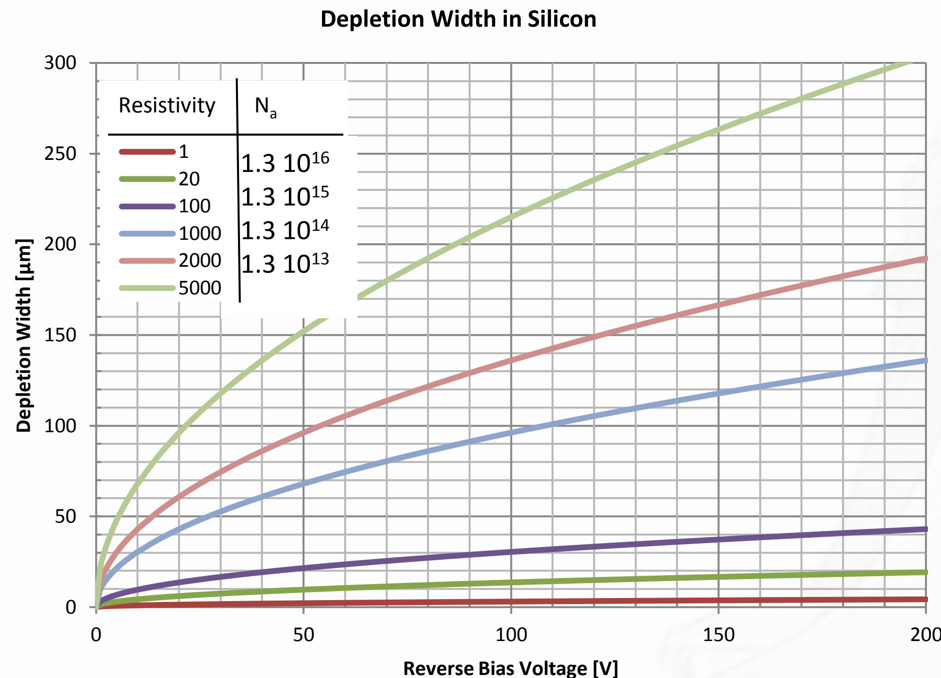
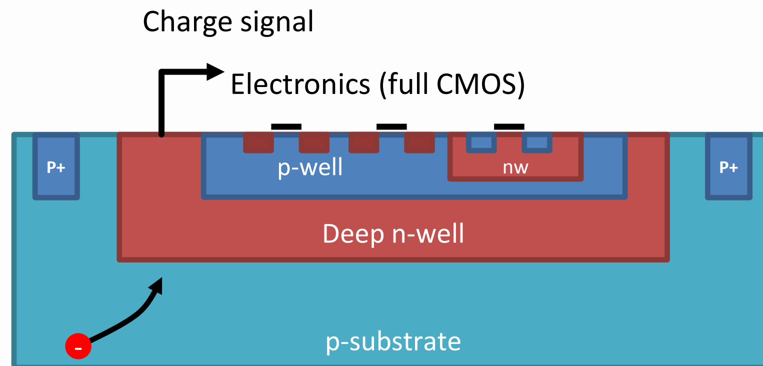
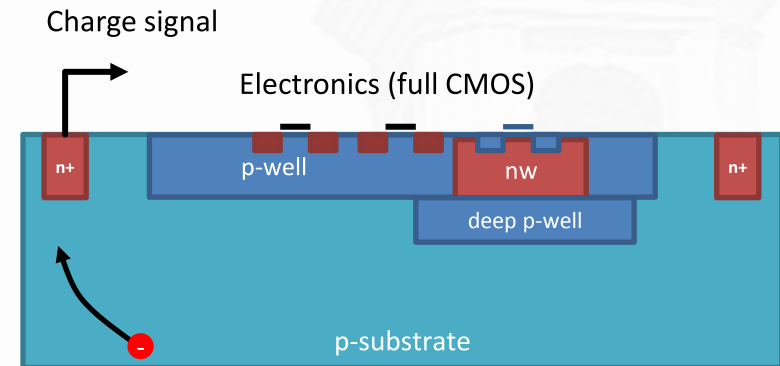
Depletion width d $\propto \sqrt{U_{bias} \cdot r_{substrate}}$

- $Q_{MIP} \propto d$
- $C_{parallel\ plate} \propto \frac{1}{d}$
- High voltage on the r/o node → HV CMOS process
- High resistive substrate material → CMOS on high resistive substrate (“HR CMOS”)
- Something in-between



Bulk process options (simple options, n-on-p)





Electronics **outside** charge collection well

- Very **small sensor capacitance** → low power
- Potentially less rad. hard (longer drift lengths)
- Full CMOS with additional deep-p implant

Electronics **inside** charge collection well

- Collection node with **large fill factor** → rad. hard
- Large sensor capacitance (DNW/PW junction!) → x-talk, noise & speed (power) penalties
- Full CMOS with isolation between NW and DNW

Enabling technologies

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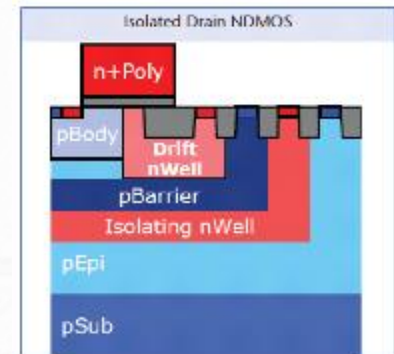
“High” Resistive Wafers

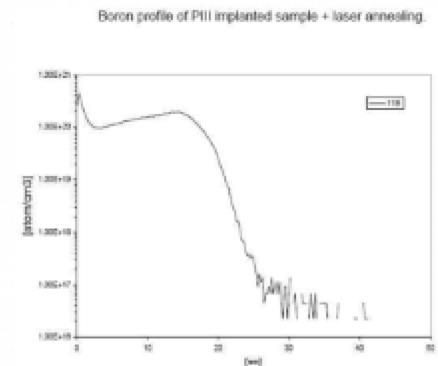
8” hi/mid resistivity silicon wafers that will be qualified by the foundry.
What is the influence of CMOS processing? (thermal donors …)



from: www.xfab.com

Sensor/Implants (<3nm gate)

Radiation hard process with as many wells as possible.
High voltage tolerant. Foundry accepts some process/DRC changes!



from: ion-beam-services.com

Low Temperature Backside Process

To achieve backside contact after CMOS processing.
Laser activation?

Simple device cross-section

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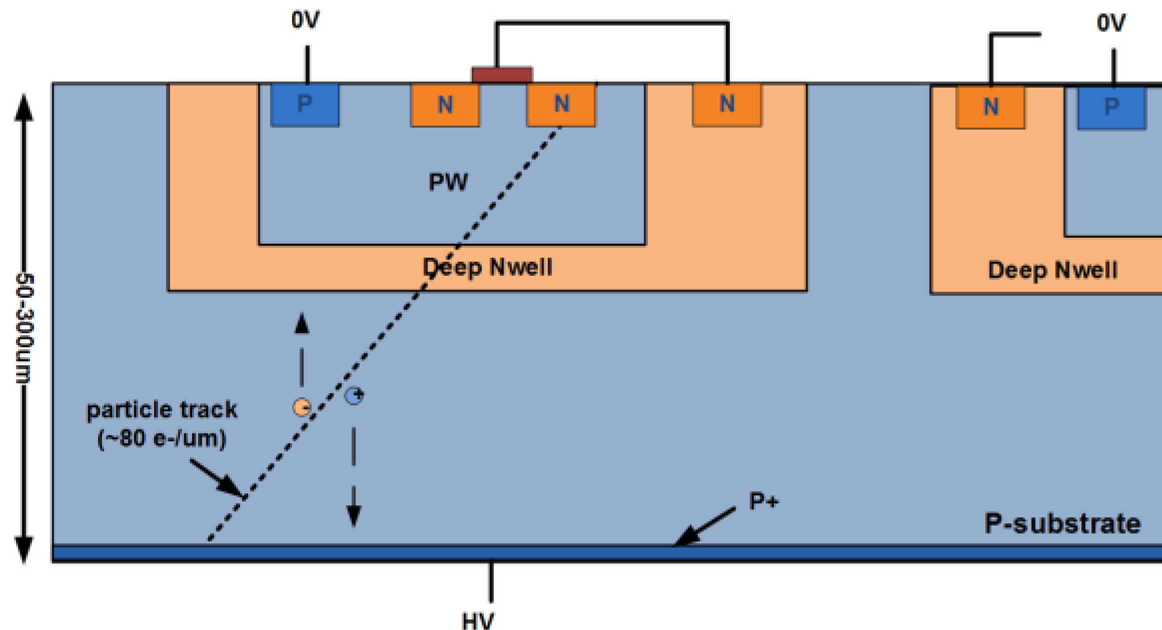


high signal (full depletion possible)

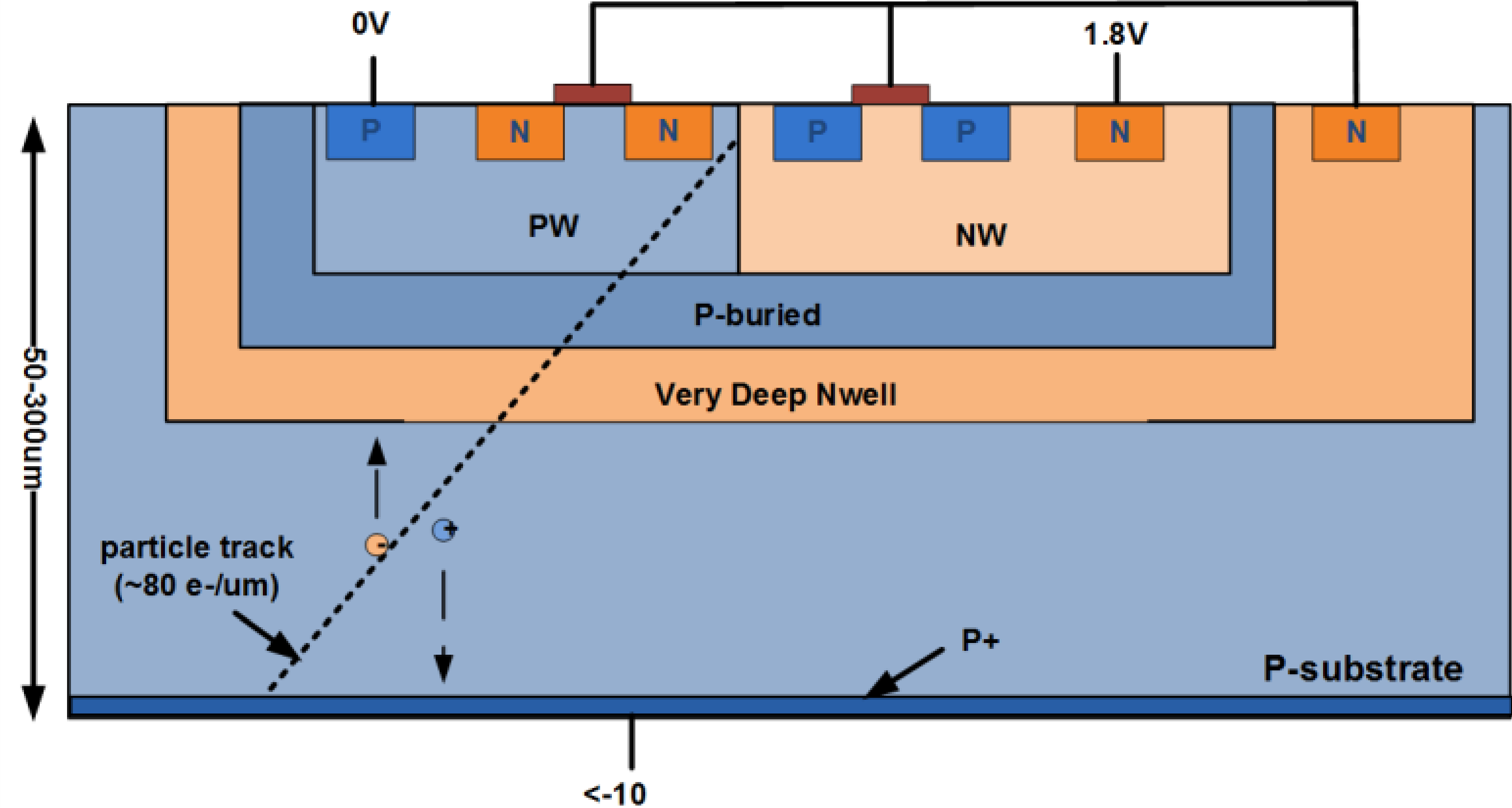
fast (collection by drift)

small pixels

only NMOS in active area

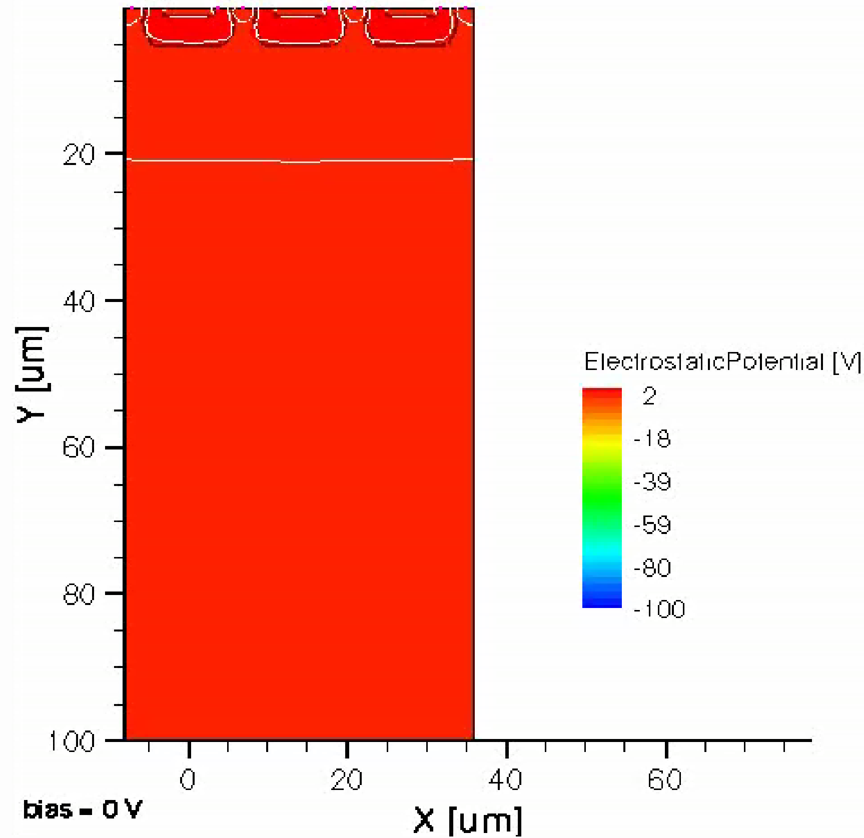
input capacitnce dominated by deep-nwell to pwell capacitance

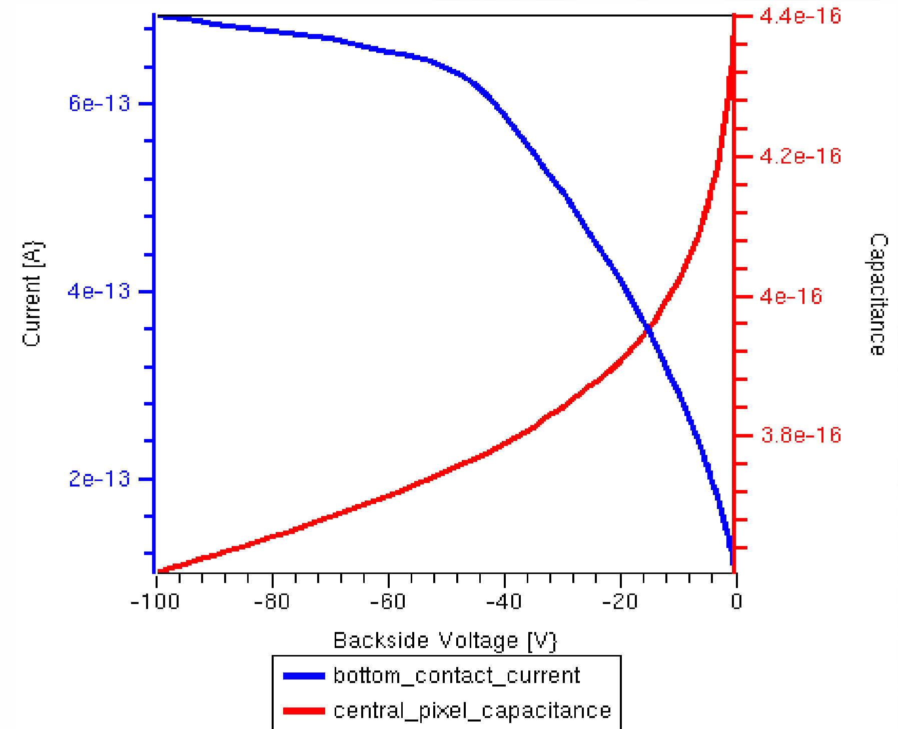
Something better



How to verify this idea?

Electrostatic Potential (HV)





Following TCAD based of foundry based 130nm process

Depletion Evolution with Voltage

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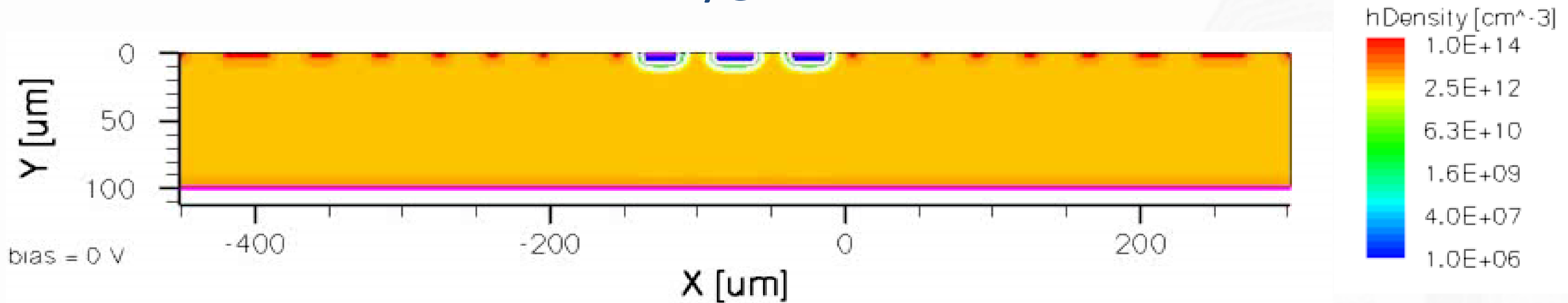
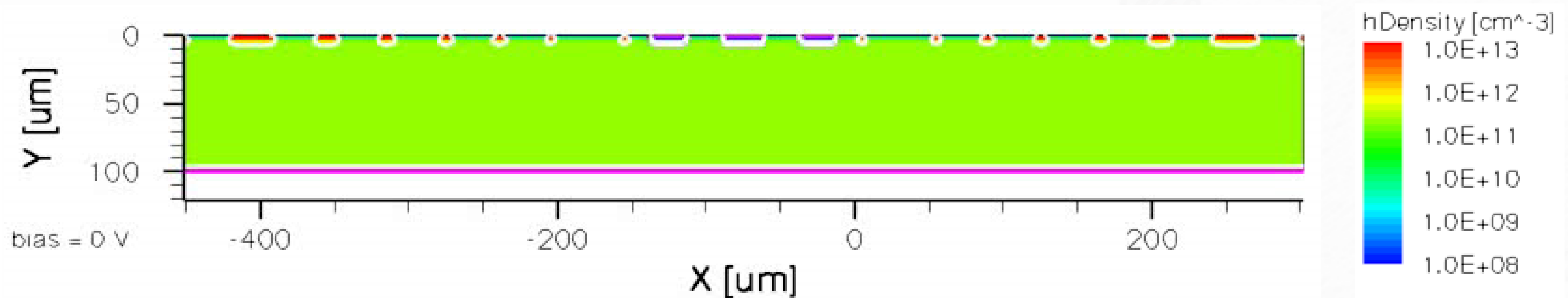
Hole Density @ no radiation



Hole Density @ Oxide Charge 1e+12 cm^{-2} + Fluence 1e+15 N_{eq}/cm^2



Charge Collection

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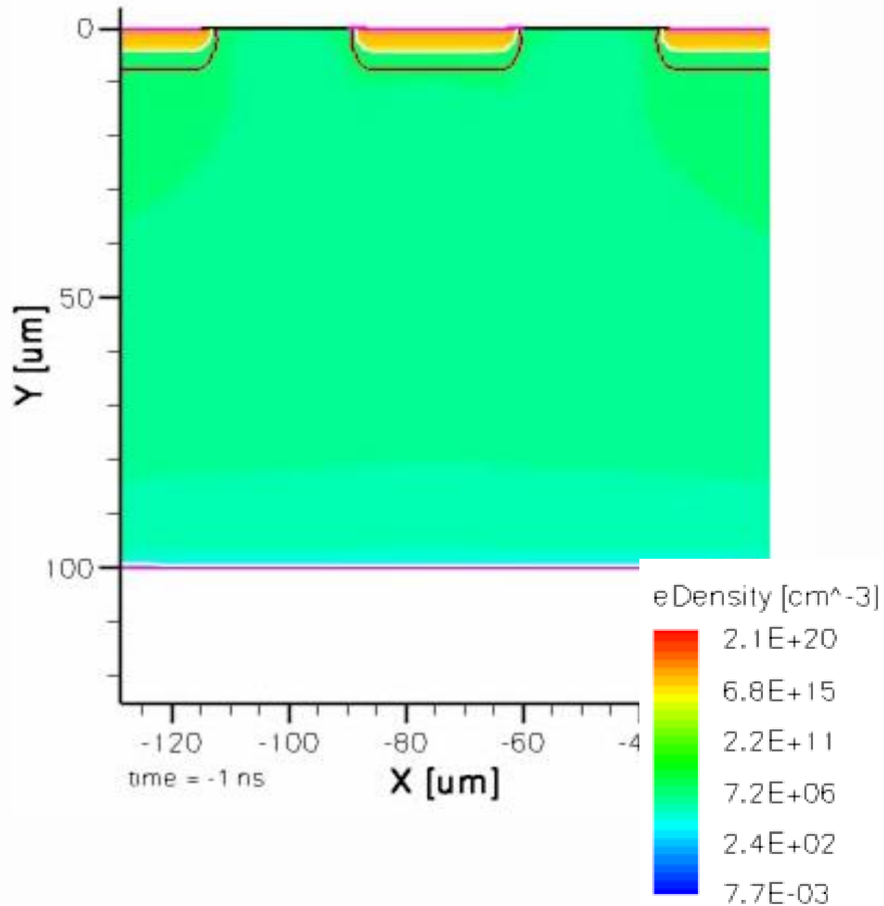
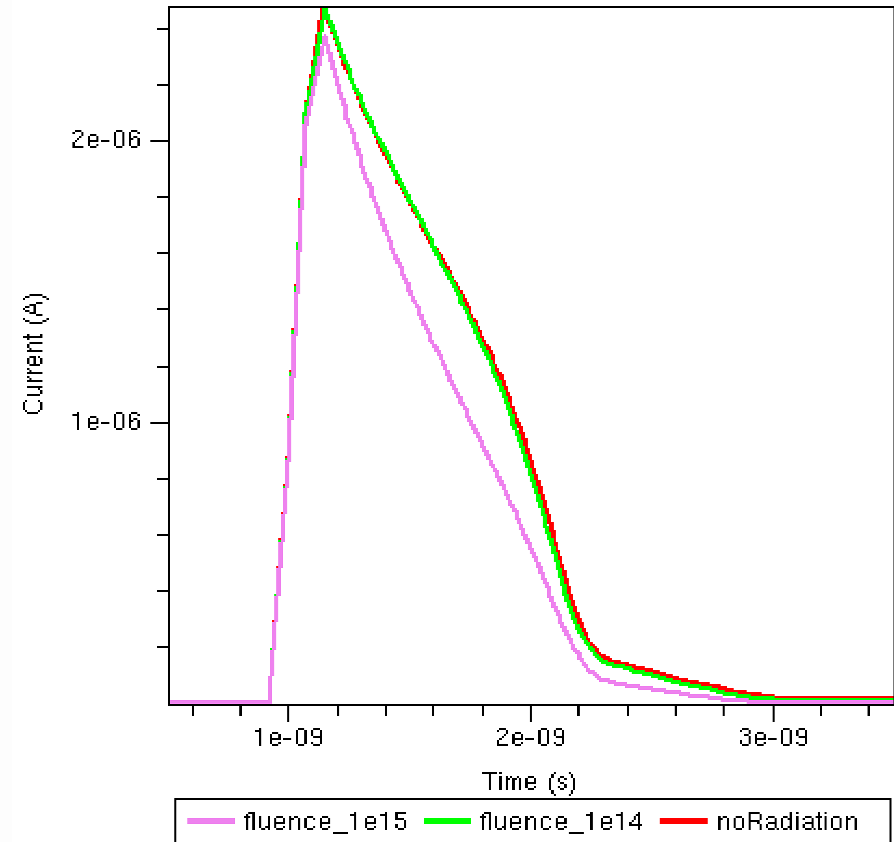
Electron Density @ 200V (no radiation)



Current on collecting electrode @200V



Charge Collection Efficiency

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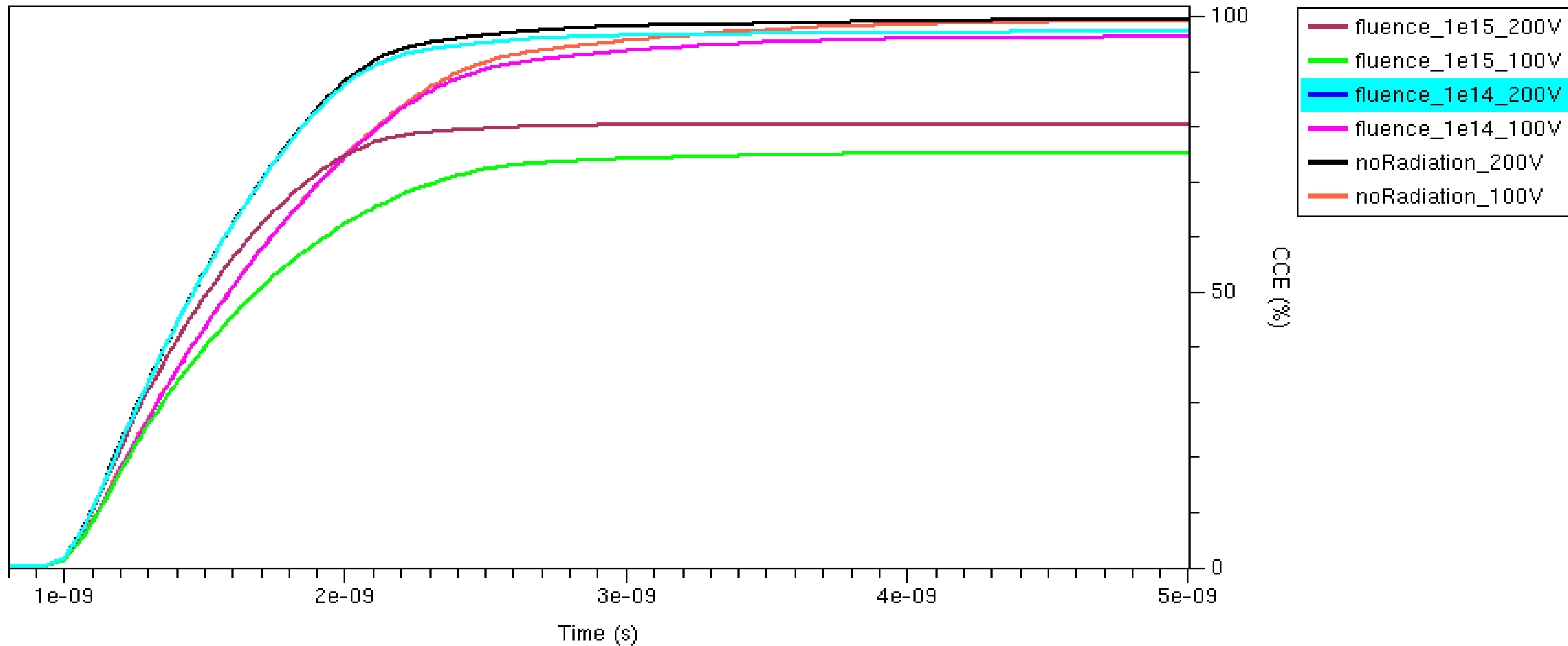
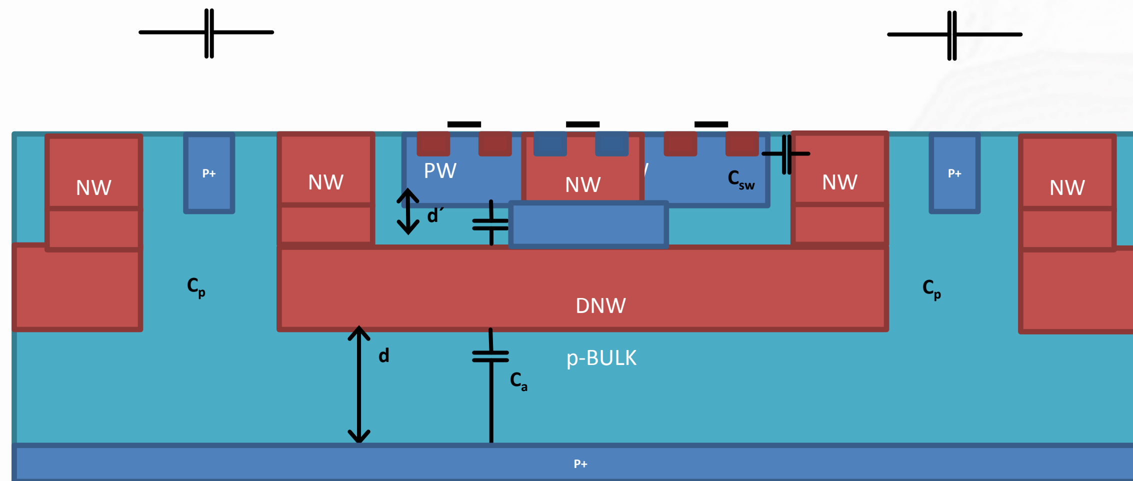


Fluence (N_{eq}/cm^2)	Back Voltage [V]	CCE [%]
0	100/200	100
1e14	100	96
1e14	200	97
1e15	100	75
1e15	200	80

Mind input capacitance



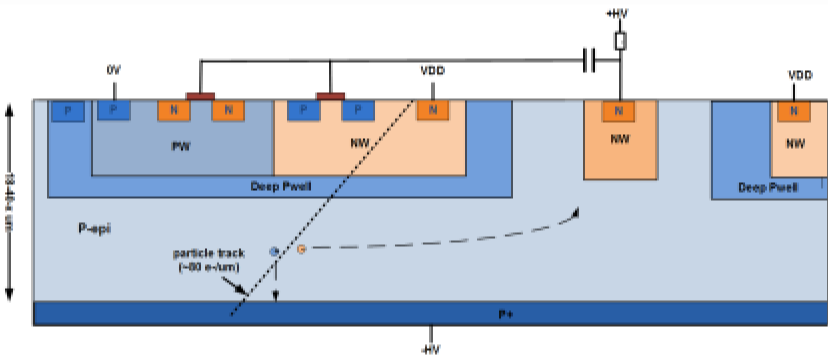
If deep n-well is used for charge collection

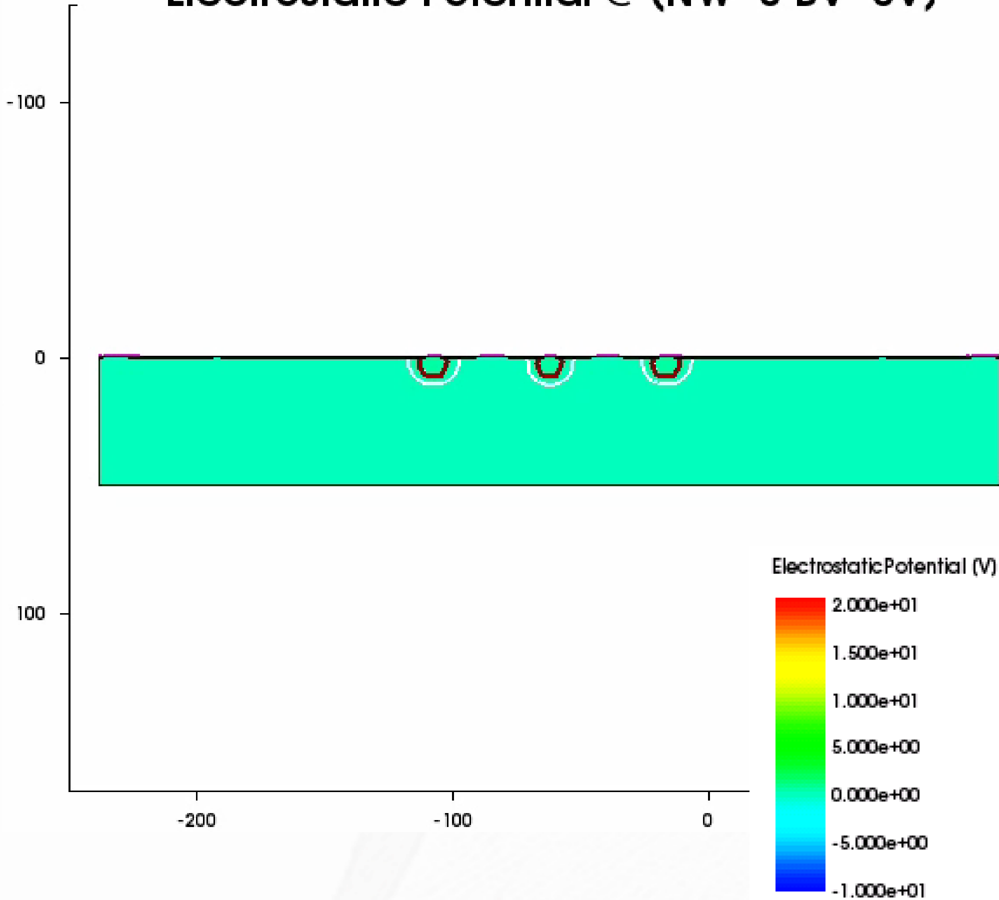
DNW no longer available for analog-digital isolation

Pixel size DNW has a large capacitance to p-implant: O(100fF)

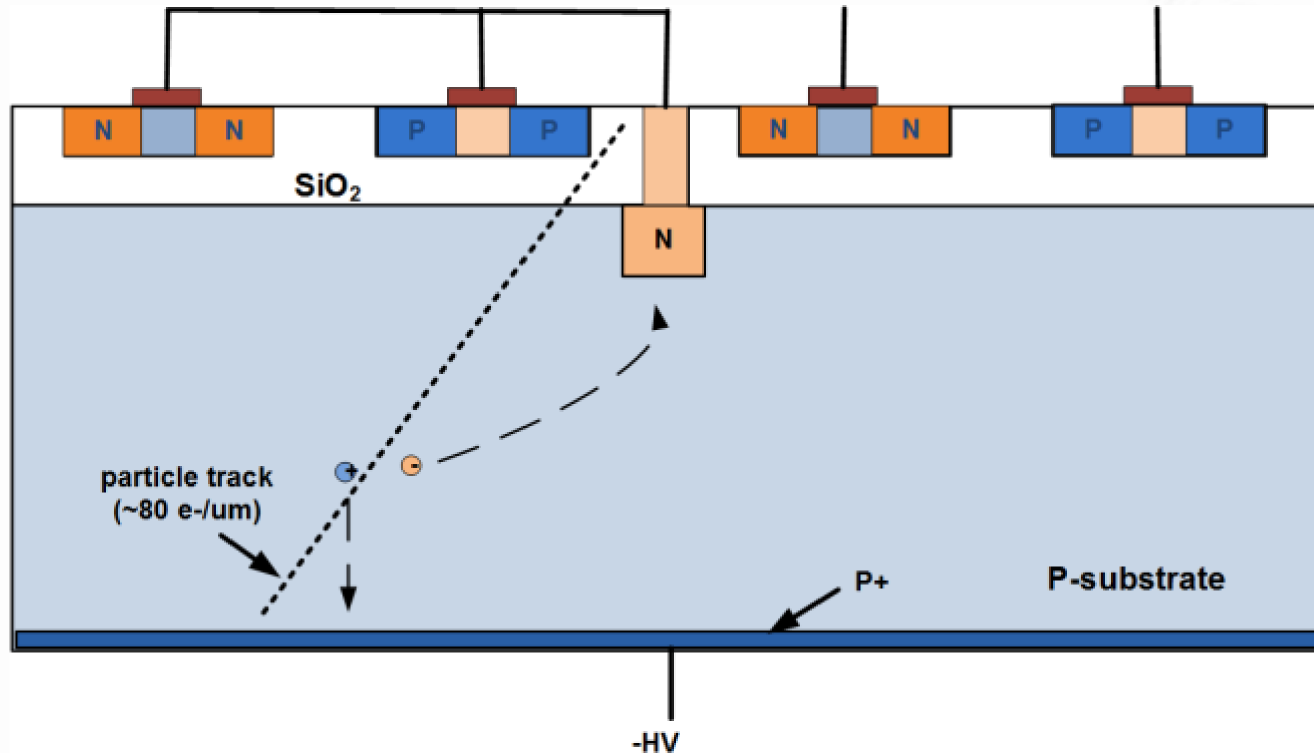
➔ <u>0.5mV ripple on p-well potential (GND) will already inject 300e$^-$ to the input!</u>

Logic next to collection node simulation





SOI process



Other …

Implementation

Active Pixel Sensors on HV-CMOS process

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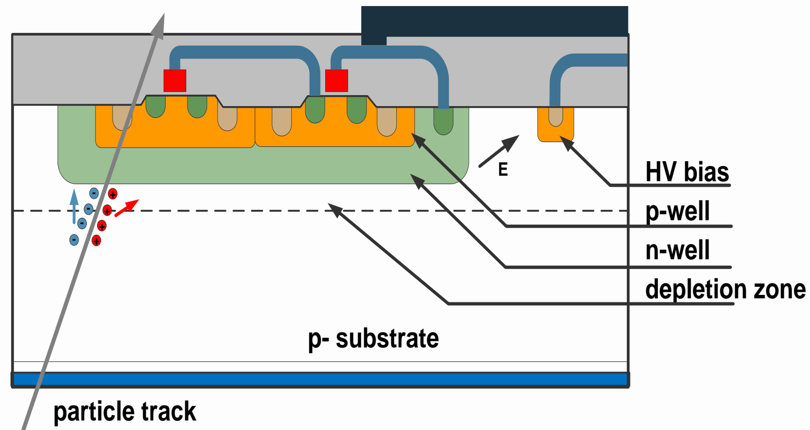
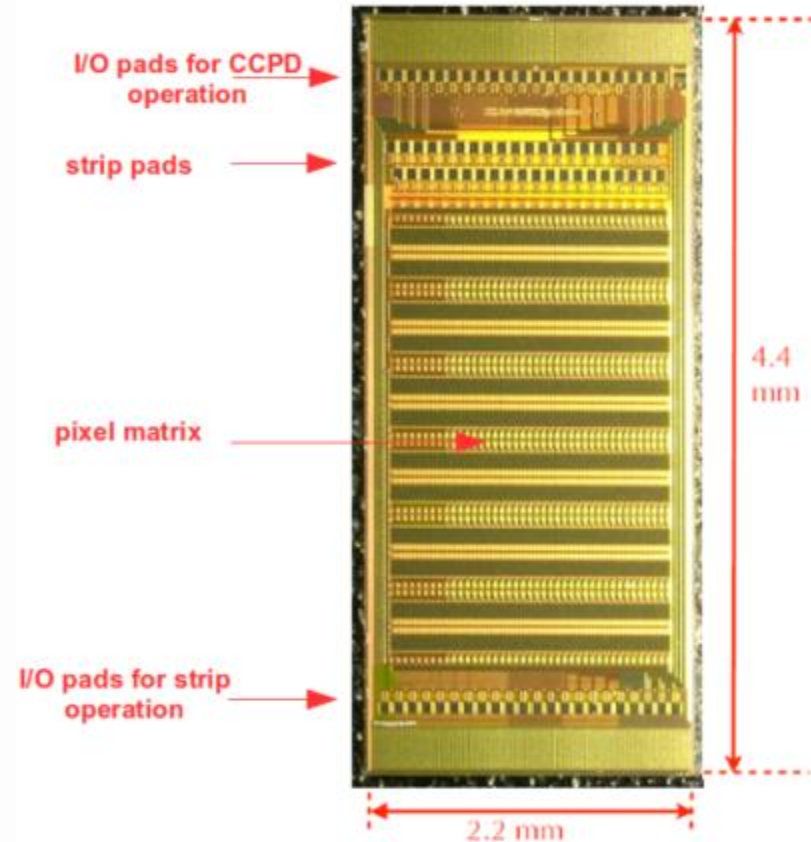




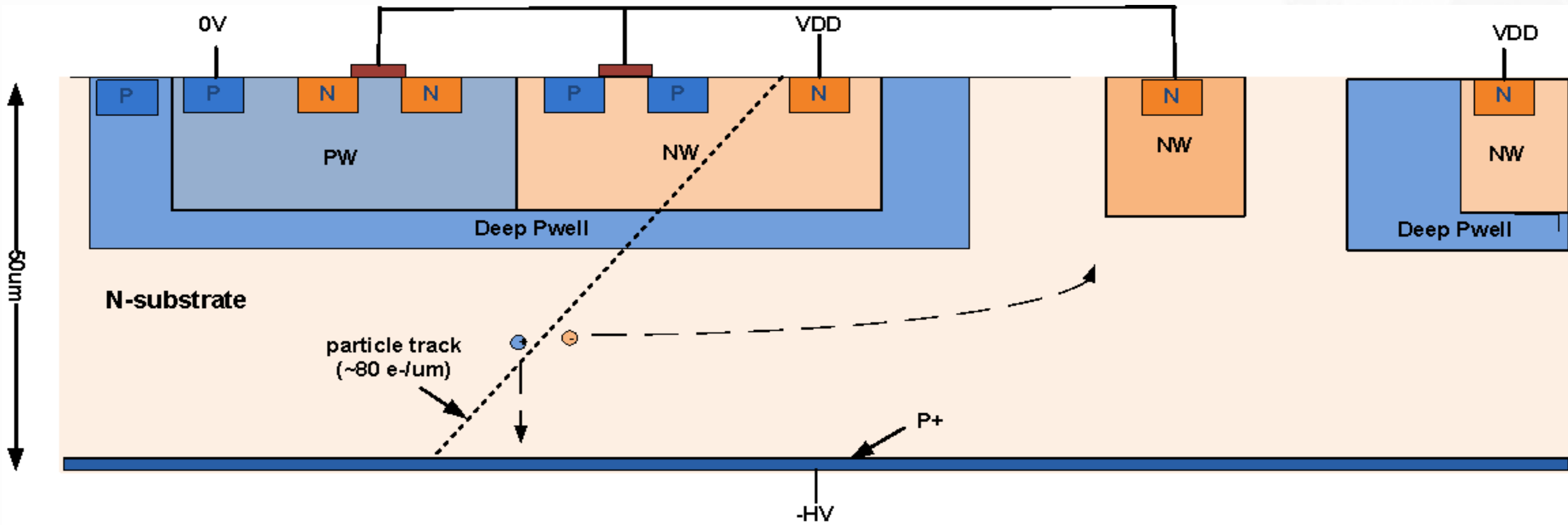
I. Peric (AMS,,GF)

In summary

- depletion (small)
- low leakage
- possible high resolution
- limited use of PMOS

Details in next talk!

ESPROS Photonic CMOS™



There is more to this in this technology ☺

EPCB01 - overview

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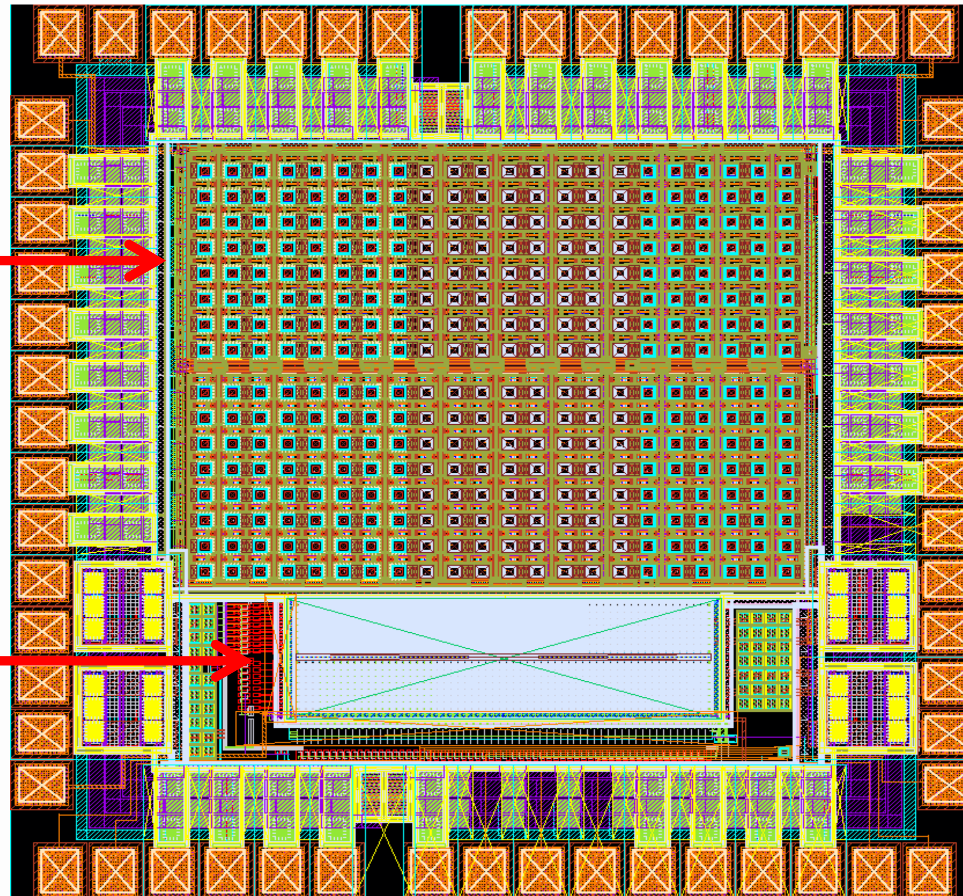
DMAPS pixels

Deep N-well pixels



Chip size: 1.4 × 1.4 mm²

Design&Testing:

Y. Fu,

M. Havranek,

T. Hemperek,

T. Kisisita,

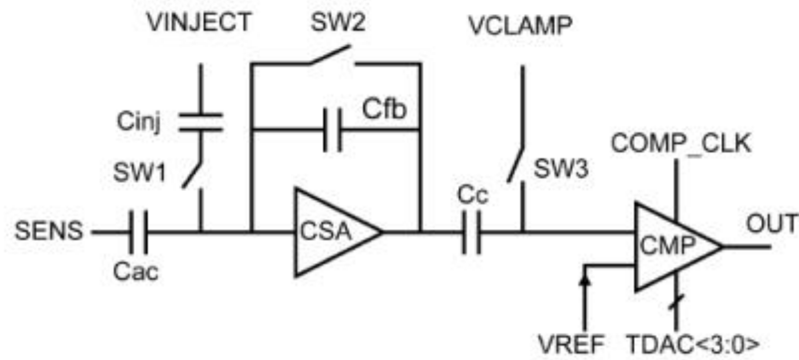
H. Kruger,

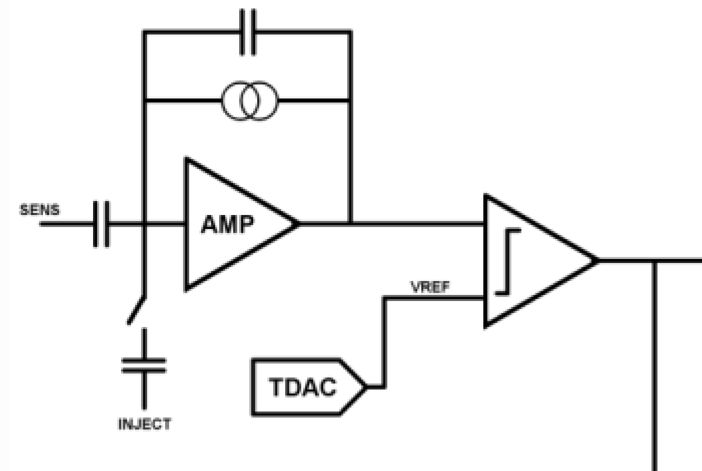
T. Oberman

L. Germic

First **50um**, **back side processed**, **full CMOS**, “**fully depleted**”
(>2kOhm-cm substrate).

EPCB01 – Front end designs





EPCB01 – Sensor bias

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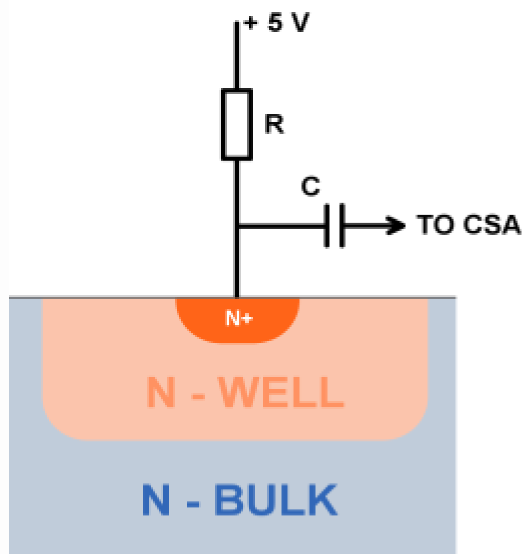

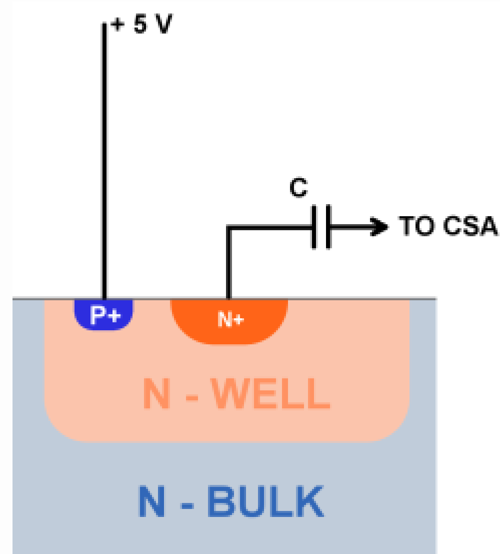

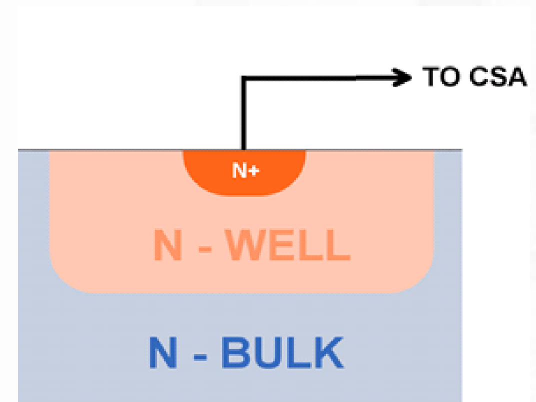

EPCB01 - noise

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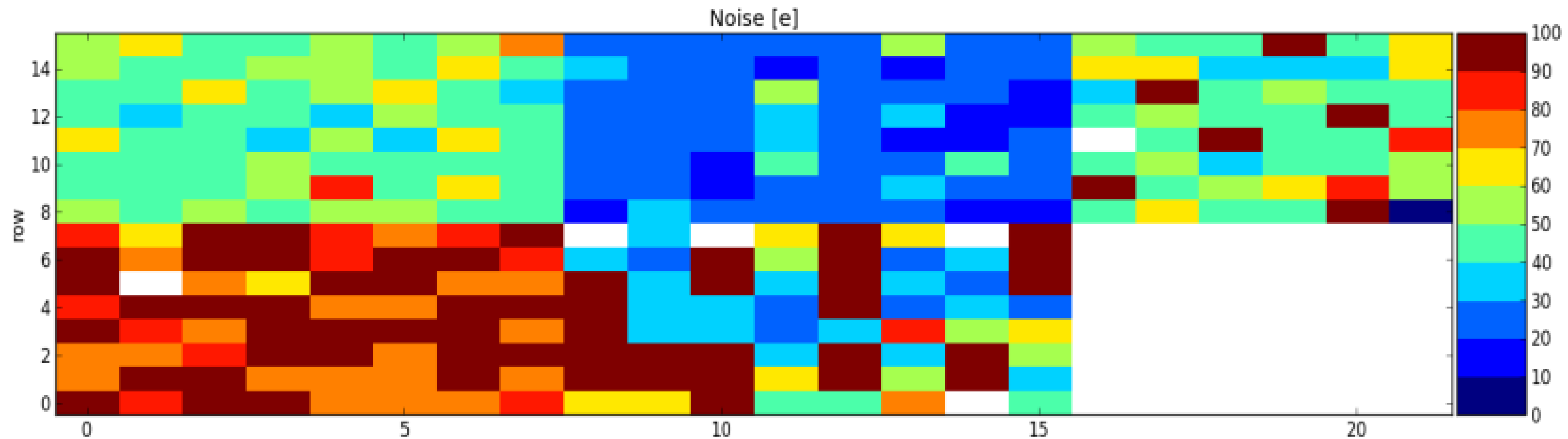

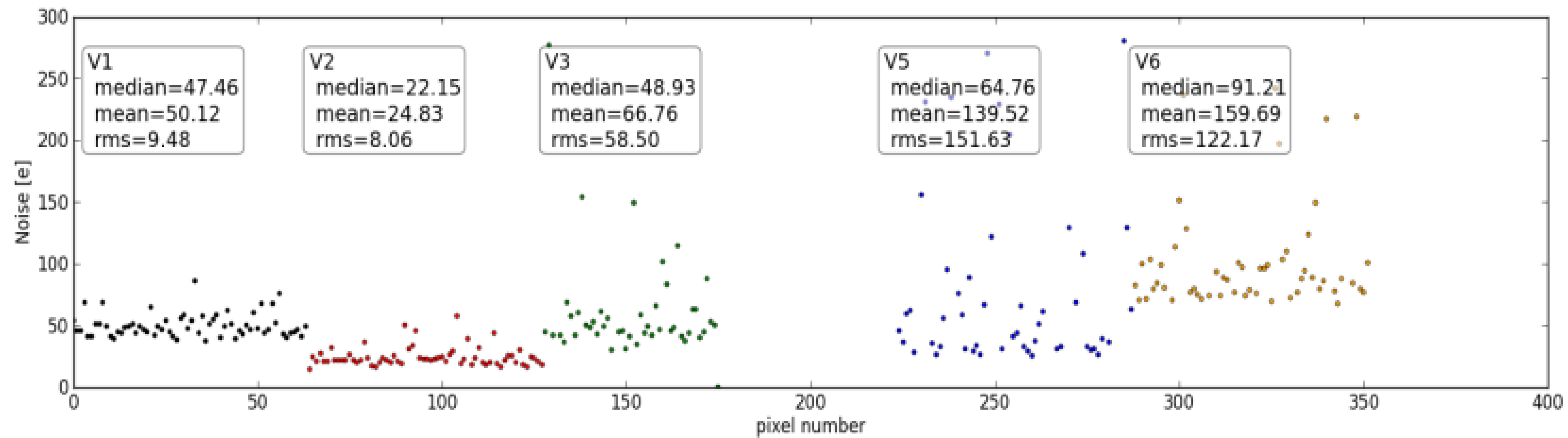

EPCB01 Fe55/Laser

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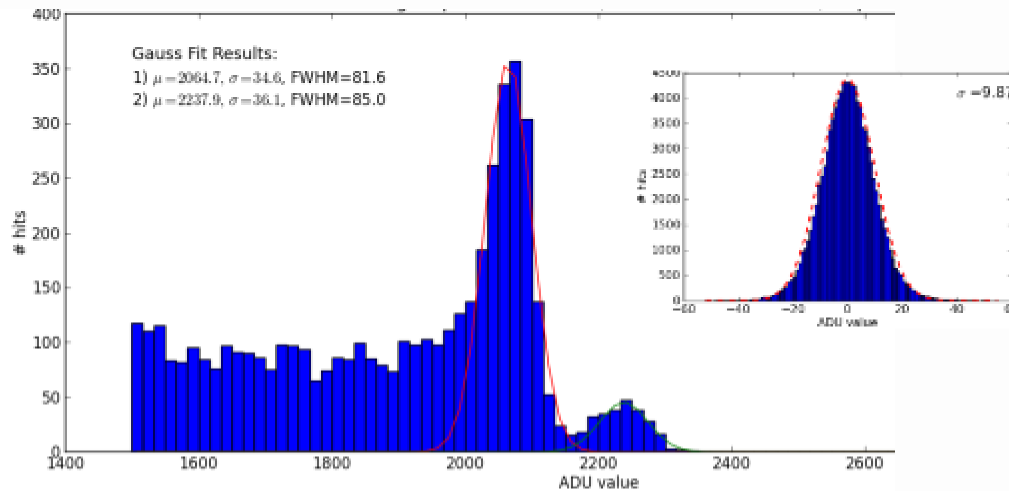
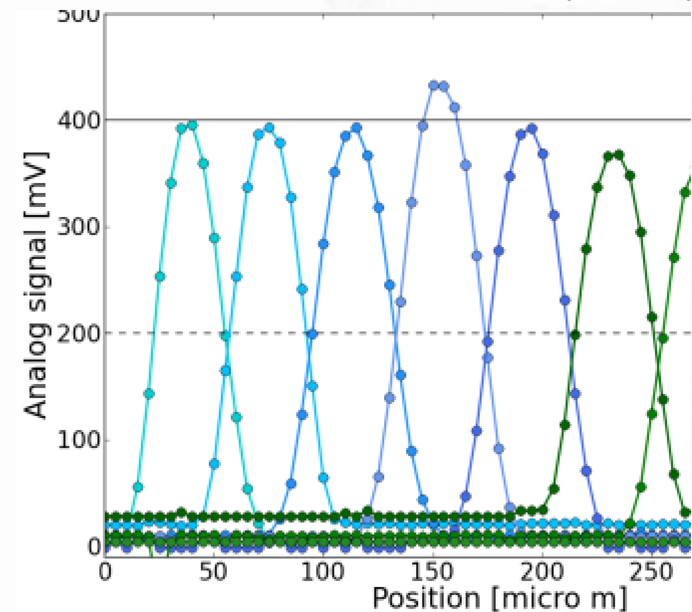
Fe55 and baseline spectrum (single pixel 40x40um)

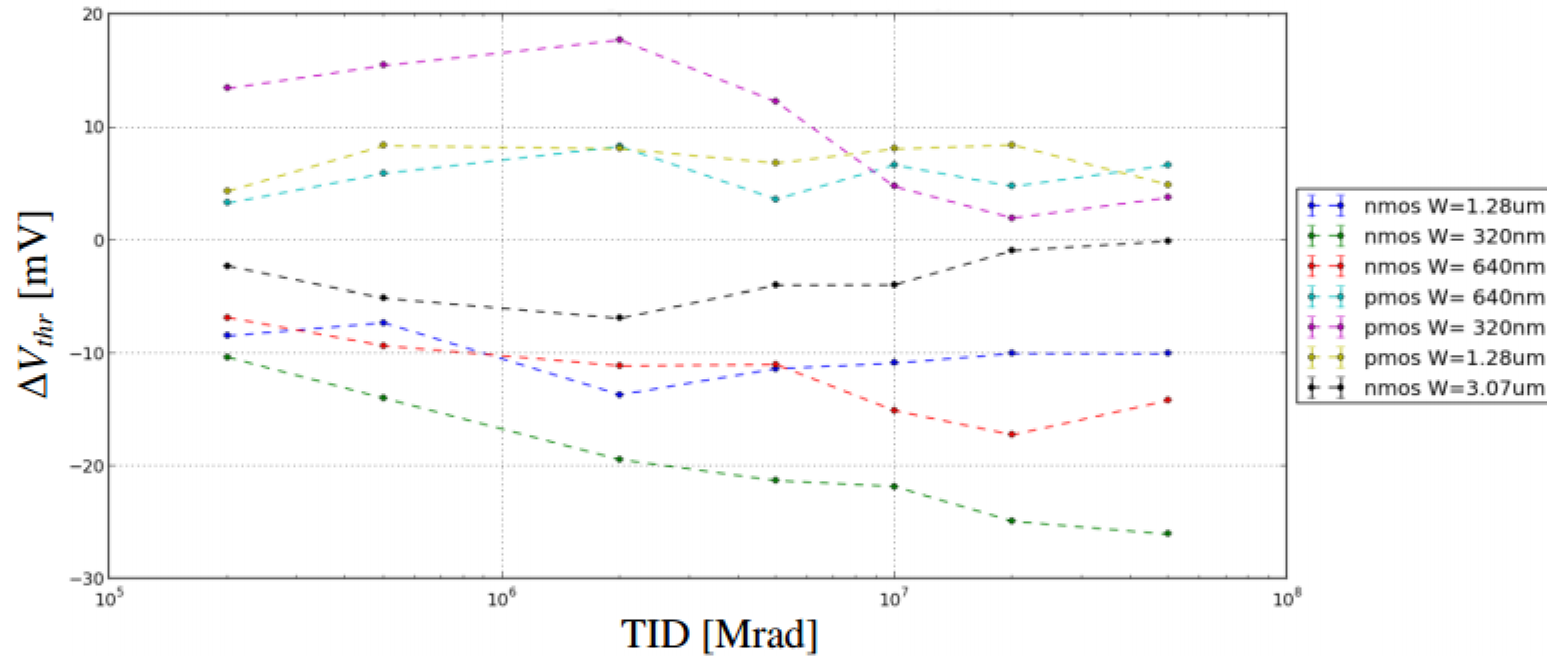


Gain: ~ 100 µV/e (200 mV ~ 2 ke)
Power: ~5uW
Peaking time: <25ns
Sahping time: ~200ns-2us (for continous reset)

Backside laser scans (@~12V)



EPCB01 - Radiation



Pegasus prototype

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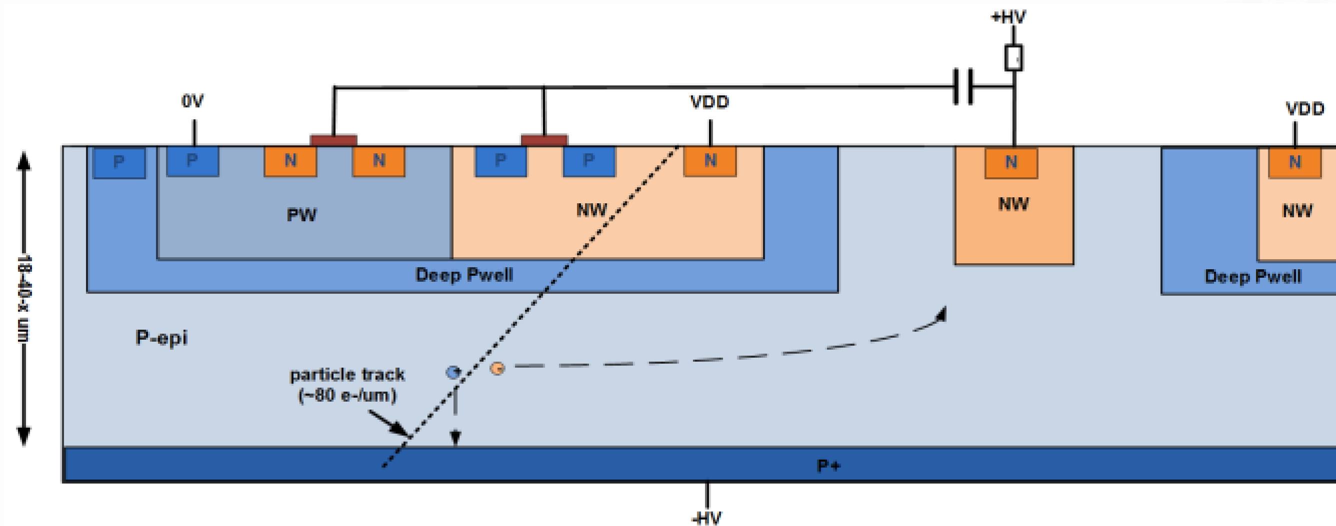
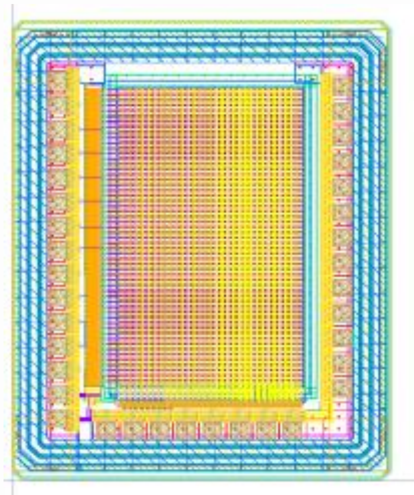




Parameters:

180nm CMOS (TowerJazz)

Different wafer materials

18µm HR epi

40µm HR epi

HR bulk

50 x 50 µm^2 and 25 x 25µm^2 pixels

Design:

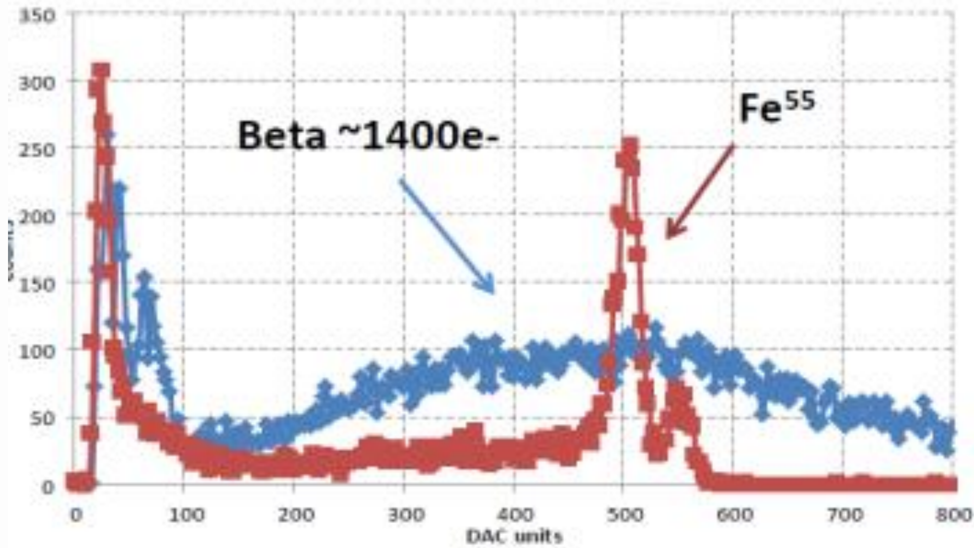
M. Kachel (IPHC),

W. Dulinski (IPHC),

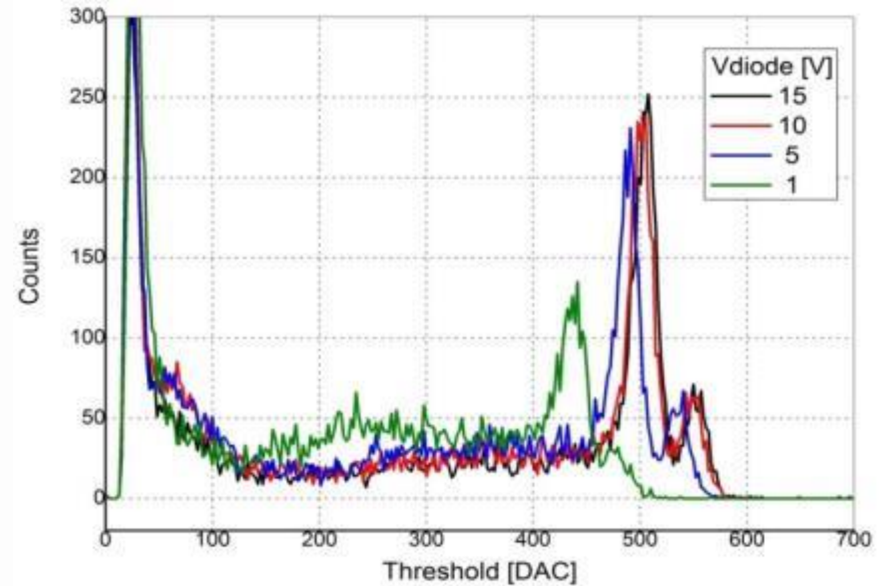
T Hemperek

Pegasus - measurements

Sr^{90} and Fe^{55} Spectra for 18µm epi



Fe^{55} Spectra for 18µm epi



M. Kachel (IPHC)

> 20V bias possible

FD-SOI

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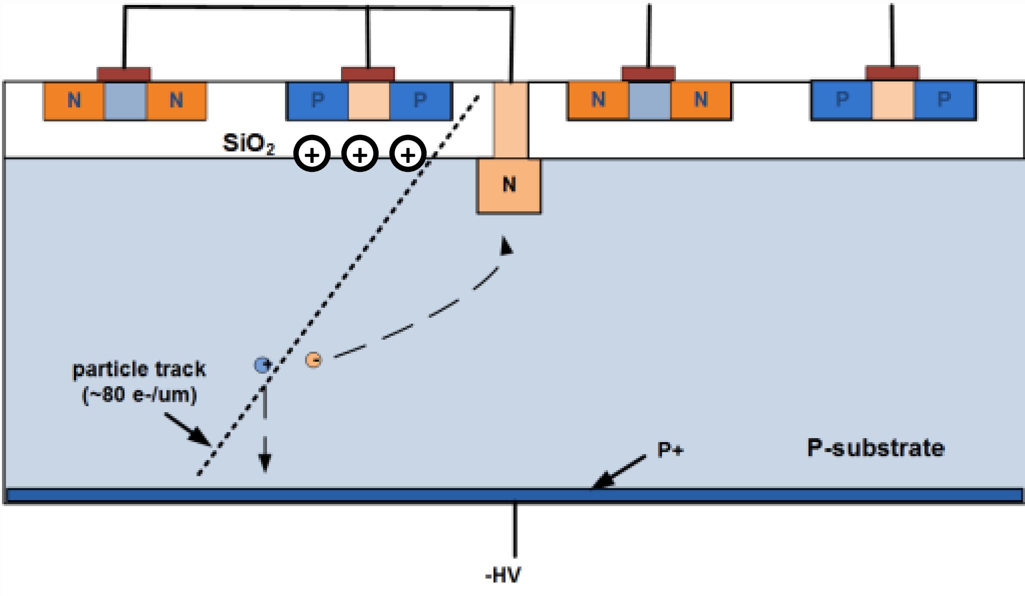

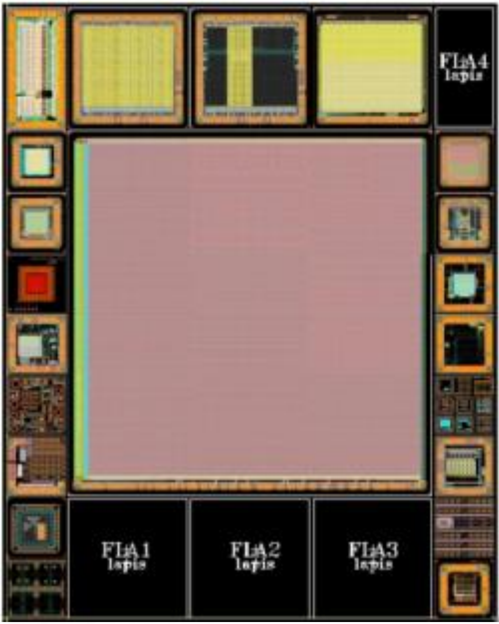

HV-SOI

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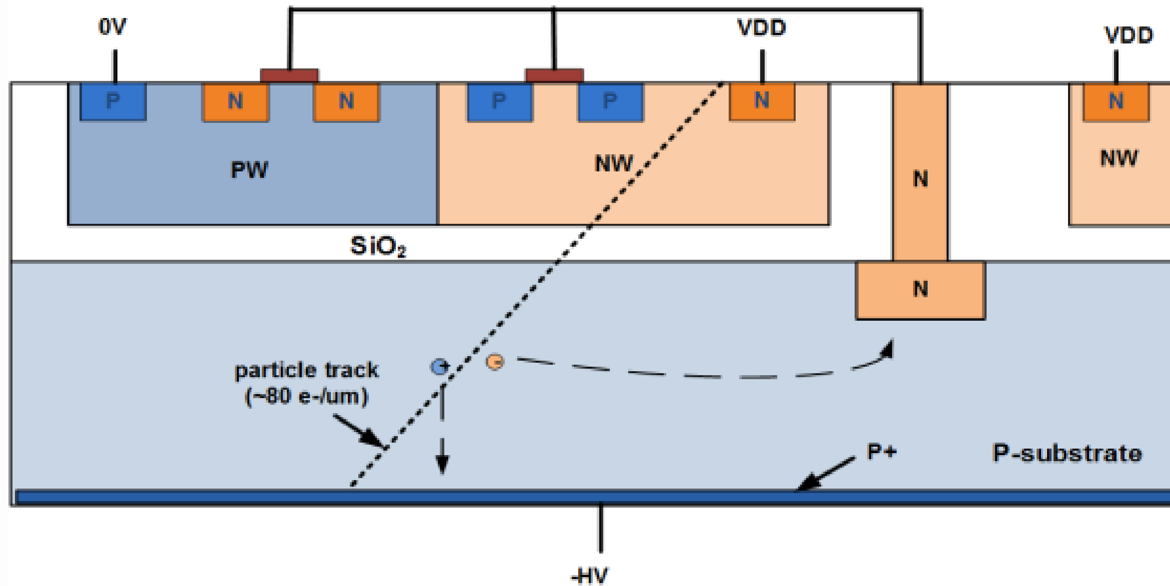
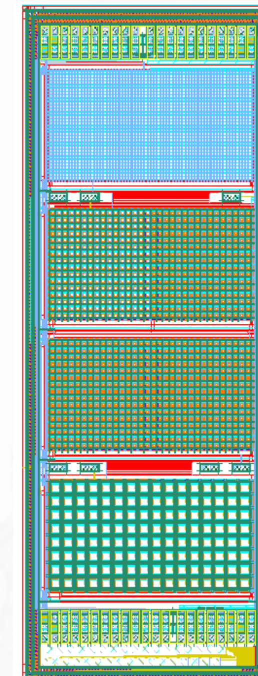


XTB01 prototype



Design&Testing:

T. Hemperek,

T. Kisisita,

H. Krueger

Parameters:

180nm CMOS

100 Ohm bulk

100x100um 50 x 50 μm^2 and 25 x 25μm^2 pixels

Roooling shutter

No back process at this point (side bias)

XTB01 – first measurements

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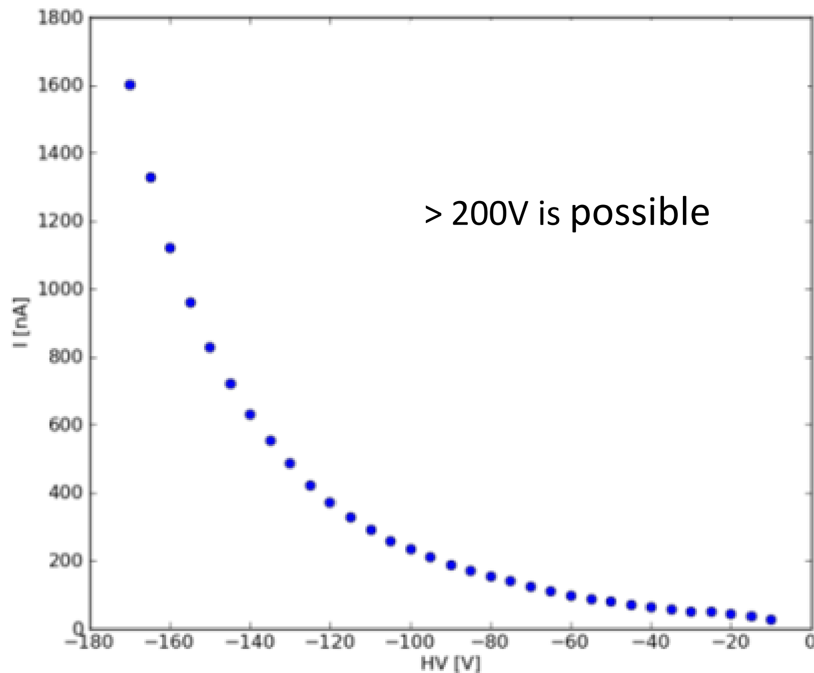

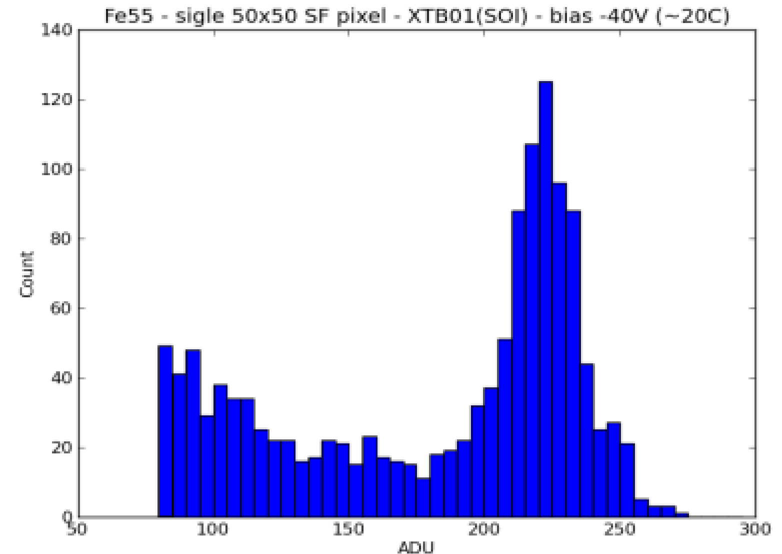

- Sensor leakage problems observed
- Process has been changed (to mitigate leakage)
- Transistor Radiation studies ongoing

Possible scenarios for Active Sensors

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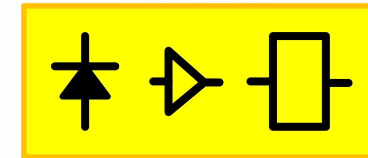
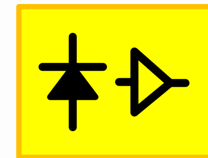
- Depleted Monolithic Active Pixel Sensor
  - HR- material (charge collection by drift) ➔ **Fully depleted** MAPS (**DMAPS**)

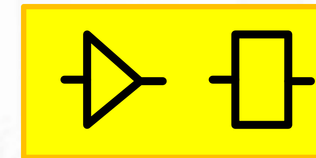


Diode + Amp + Digital

- Hybrid Pixels with "smart" diodes:
  - HR- or **HV-CMOS** as a sensor (8")
  - Standard FE chip
  - CCPD (HVCMOS) on FE-I4

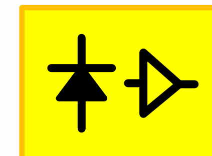


Diode + preamp



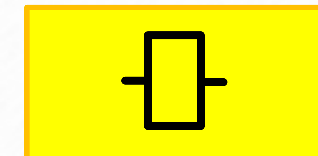
FE chip

- CMOS Active Sensor + Digital R/O chip
  - HR- or HV-CMOS sensor + CSA (+Discriminator)
  - Dedicated **"digital only" FE chip**



Diode + full analog processing

Wafer to wafer bonding



Digital only FE chip

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Thank you

Conclusion

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- Particle detection in high radiation environments based on commercial CMOS technologies looks promising
- Progress in technology and openness of industry for niche applications allows new concept to be realized
- Possible implementations were presented and results from first prototypes
- More designs are being submitted in various technologies
- Radiation qualification is ongoing
- Lot of work and many open questions