PMm²
Smart chip for large area distributed photomultipliers

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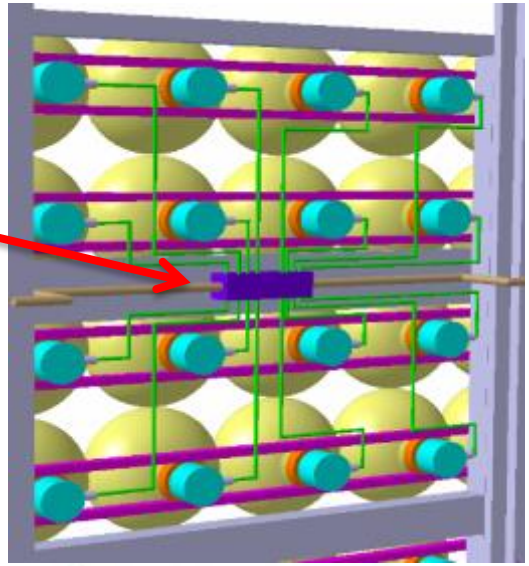
Organization for Micro-Electronics desiGn and Applications

PMm^2 project and PARISROC chip

- **Goal of PMm2 project** :
  - Replace large PMTs by arrays of smaller ones with common high voltage and a central ASIC
  - This central ASIC must provided :
    - 16 independent channels
    - Auto-trigger at 1/3 p.e.
    - Charge and time measurement (10-12 bits)
  - The electronics must be water-tight and Data driven : « One (cheap) wire out »
- **Next generation of readout for large systems**
  - « Smart communicant sensors »
  - On-detector signal processing
  - Cost minimization



PARISROC stands for Photomultiplier ARray Integrated in SiGe Read-Out Chip

PARISROC overview

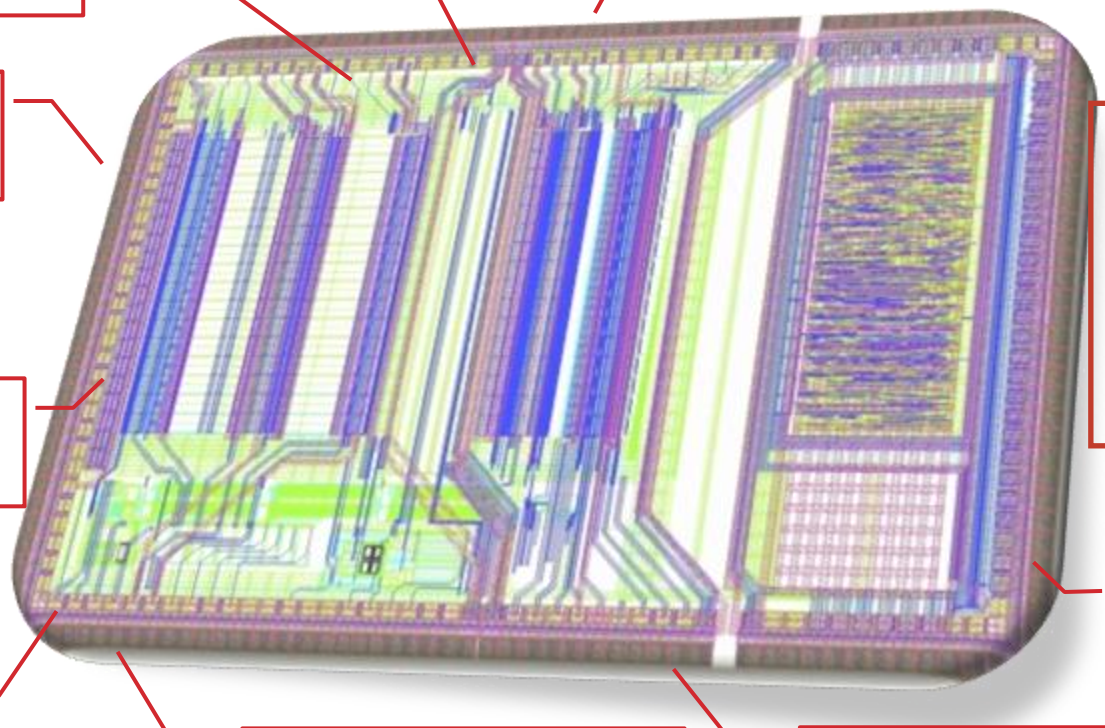
Dual-gain Preamplifiers

Time measurement: tagging < 1 ns

16 Channels (negative input signal)

10 bit ADC internal conversion

CQFP160
5 mm X 3.4 mm



A very complex SoC designed for multiple purposes and experiments

Large input range

278 slow control parameters

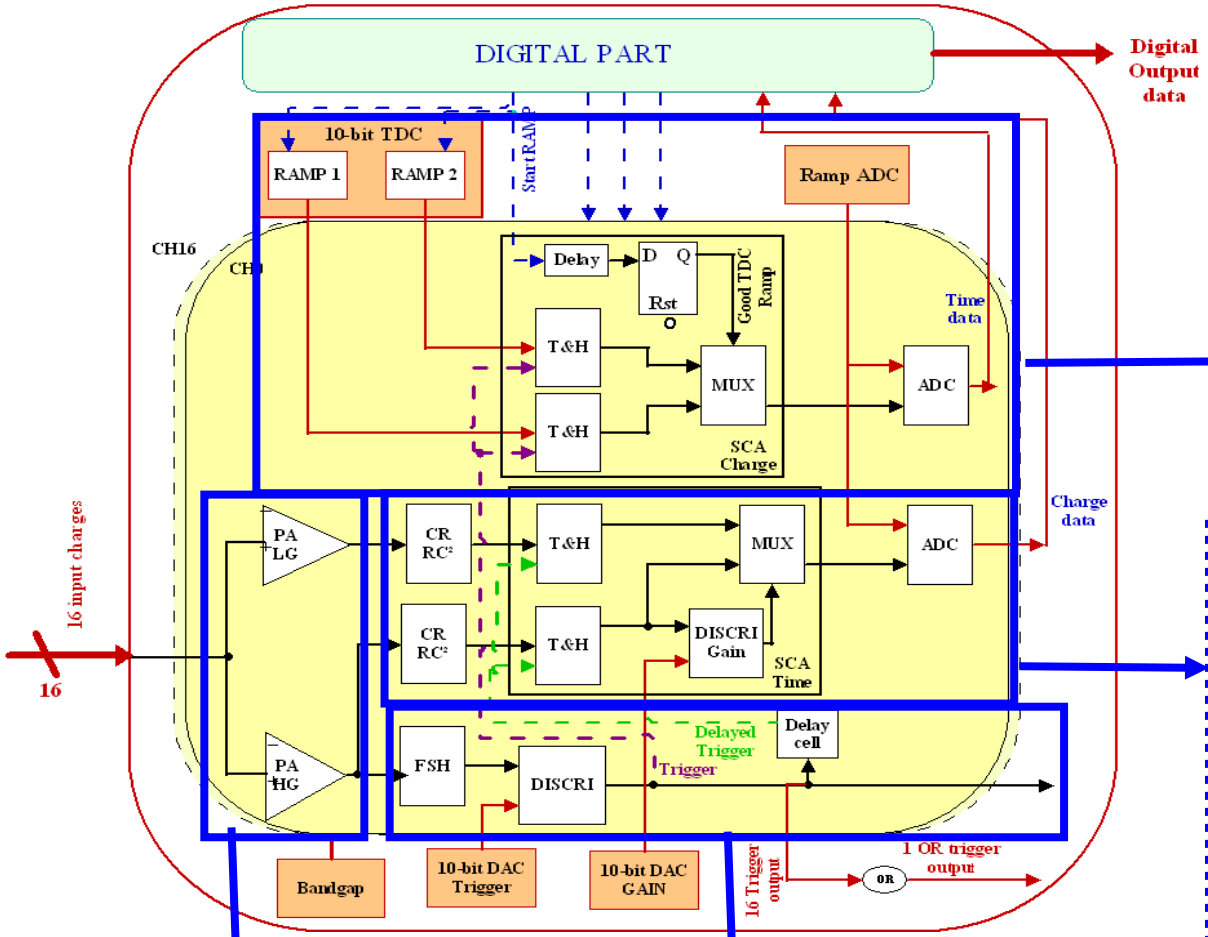
Auto-trigger design

Charge measurement: 50 fC ~ 100 pC

15 mW / channel

Technology: 350 nm AMS SiGe process

PARISROC: System On Chip



Time measurements

by 2 systems :

1. Coarse time by 24-bit gray counter (Digital part)
   - working at 10 MHz
   - with 1.67 s of dynamic
   - 100 ns steps
2. Fine time by analog TAC
   - 100 ns dynamic range
   - 1 ns steps

Charge measurements

✓ Two gain channels to cover the large input dynamic range
✓ Shaper with variable shaping time (form 25 ns to 100 ns) and gain
✓ Dynamic range from 1/3 pe to 600 pe (~ from 50 fC to 100 pC)
✓SCA with depth 2
✓10-bit Wilkinson ADC
✓ Charge resolution: max 0.2 p.e. (32 fC)

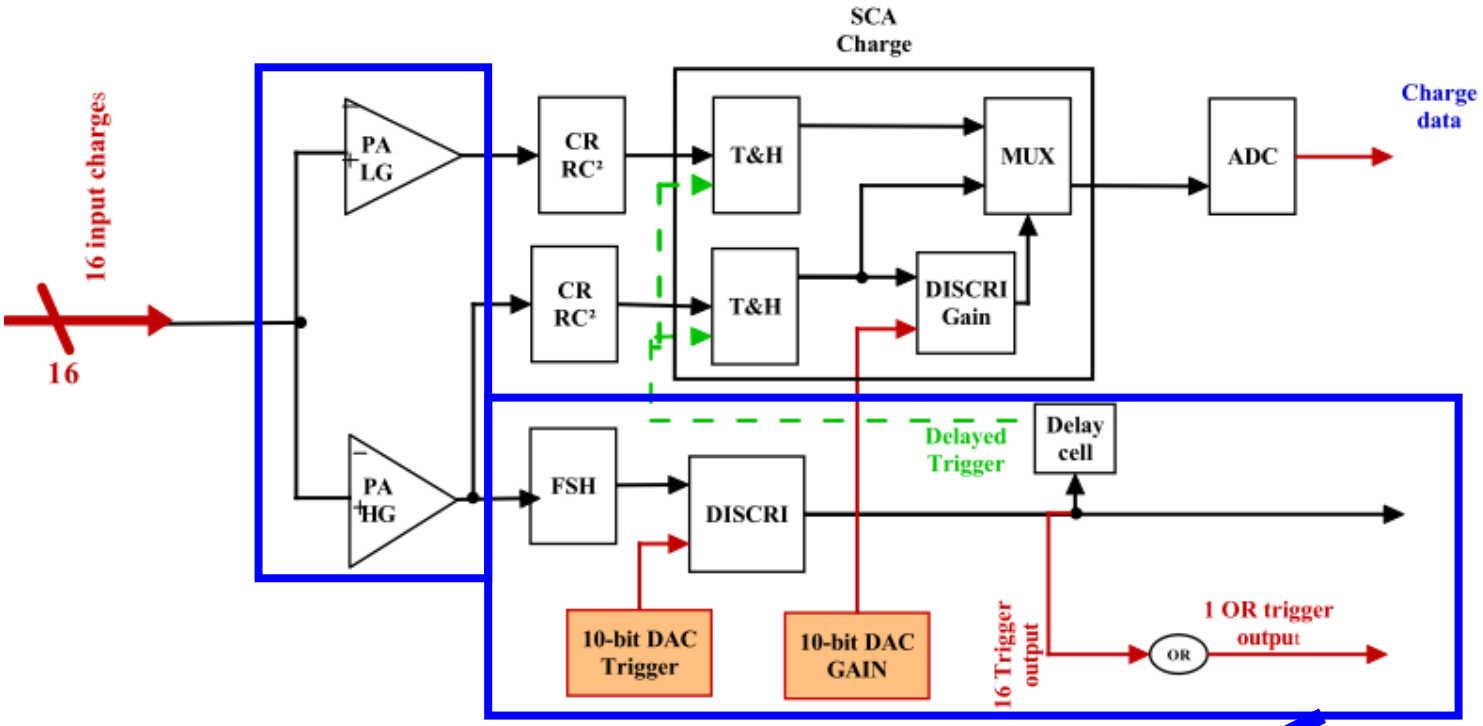
Input stage

2 input preamplifiers with adjustable gains (on 8 bits)

Auto-trigger

Fast shaper (15ns)
Low offset discriminator
Common 10 bit-DAC as threshold

Auto-trigger



Auto-trigger system :

Fast shaper (15ns) + Low offset discriminator

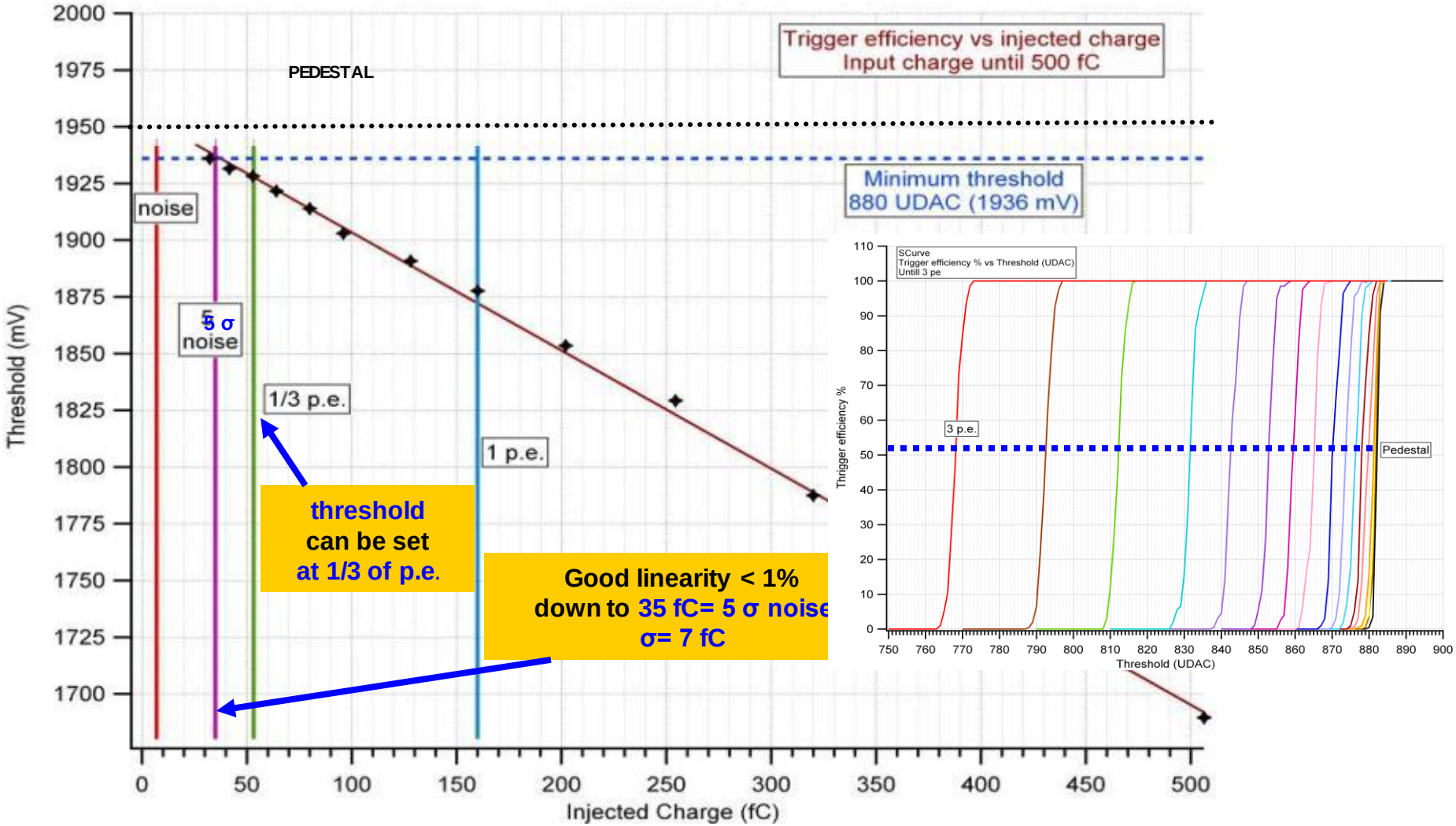
Common 10 bit-DAC as threshold

System auto-trig at 1/3 pe (50fC) and starts the charge and time measurement

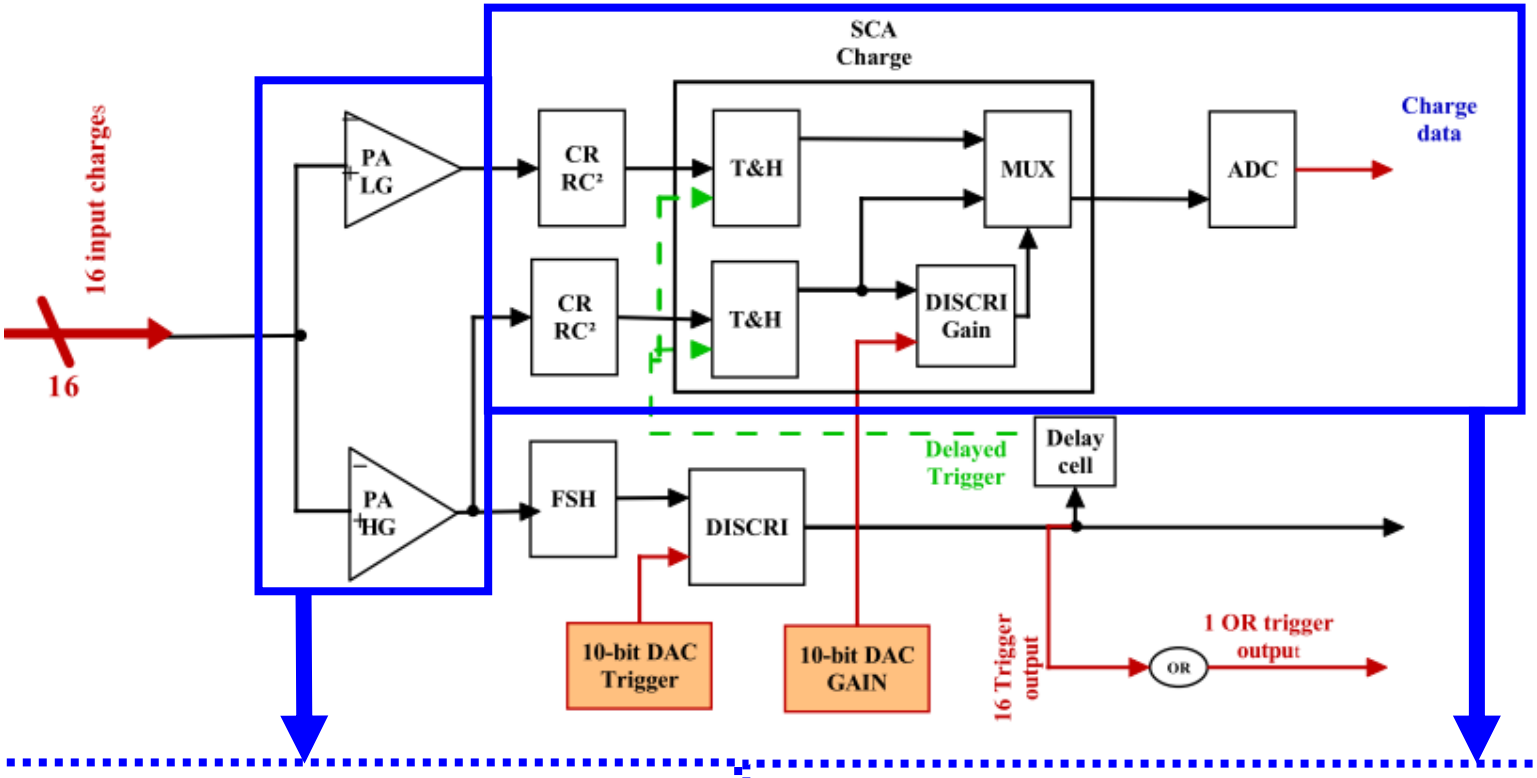
16 trigger outputs

1 OR of the 16 triggers output

Auto-trigger efficiency



Charge measurement



➢ Input stage:

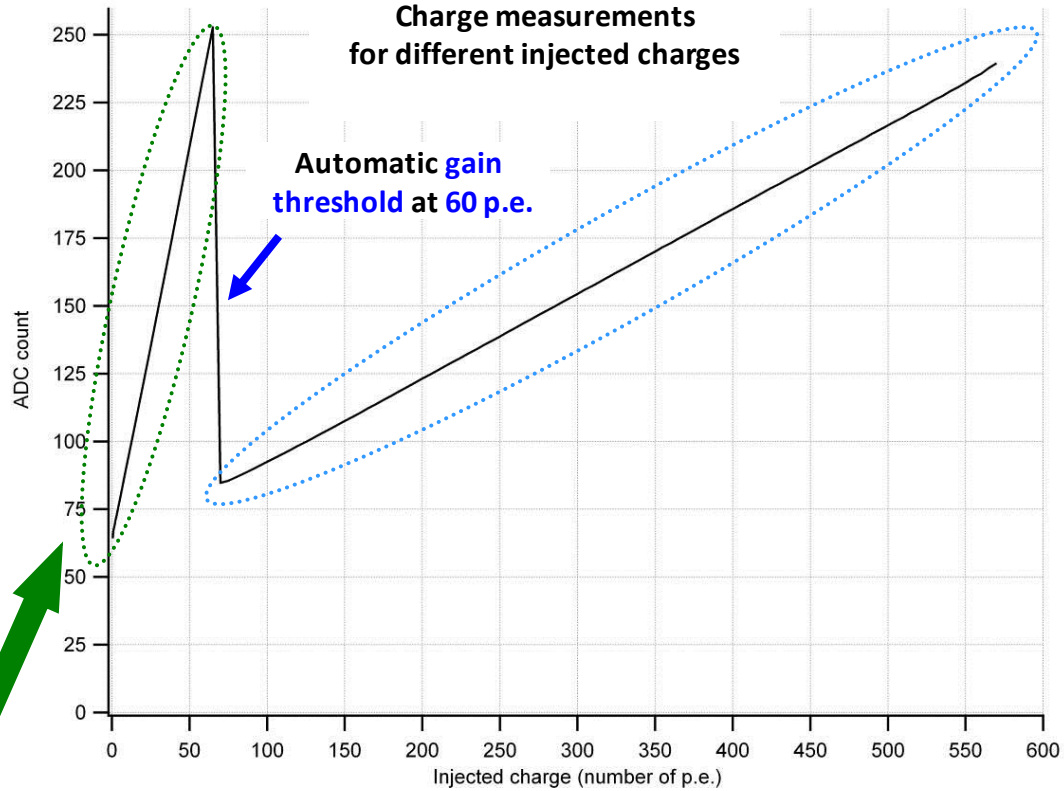
- Voltage input (external 50Ω termination)
- Two gain channels to cover the large input dynamic range (from 50fC to 100pC)
- Preamplifiers with adjustable gains (variation of a factor 4 on 8 bits)

➢ Charge measurement:

- Shaper with variable shaping time (from 25 ns to 100 ns)
- Track and Hold system (depth 2 : ping-pong to reduce dead time)
- 8, 9 or 10-bit Wilkinson ADC
- Charge resolution: max 0.2 p.e. (30 fC) with 10-bit ADC

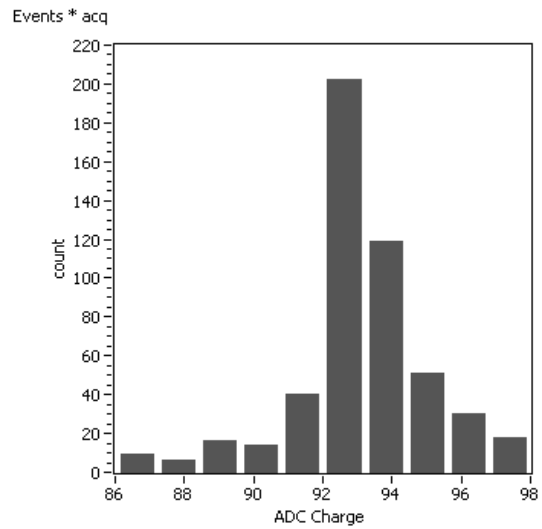
Auto-gain test (ADC measurements)

Whole chain test: input signal is amplified, auto-triggered, held in the SCA, converted and readout.



Low gain
Up to 570 p.e.

Residuals < 1 UADC → until 570 p.e.



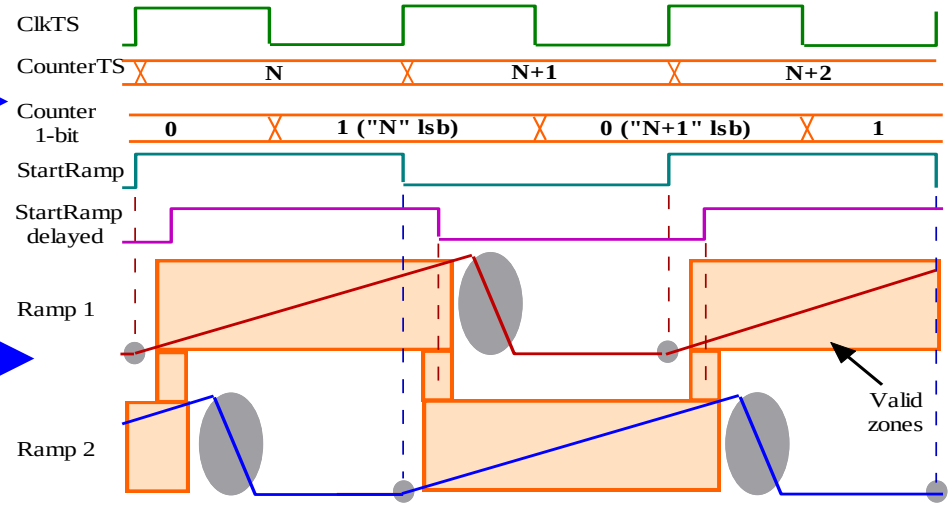
1 pe charge measurement by 10-bit ADC.
Average= 93.02 UADC,
sigma= 2.02 UADC,
range= 12UADC.
Pe/noise = 6

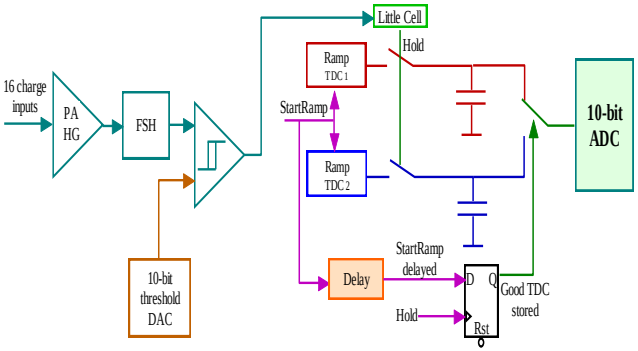
High gain
Up to 60 p.e.

Residuals < 1 UADC → until 60 p.e. (10pC)

Time measurement

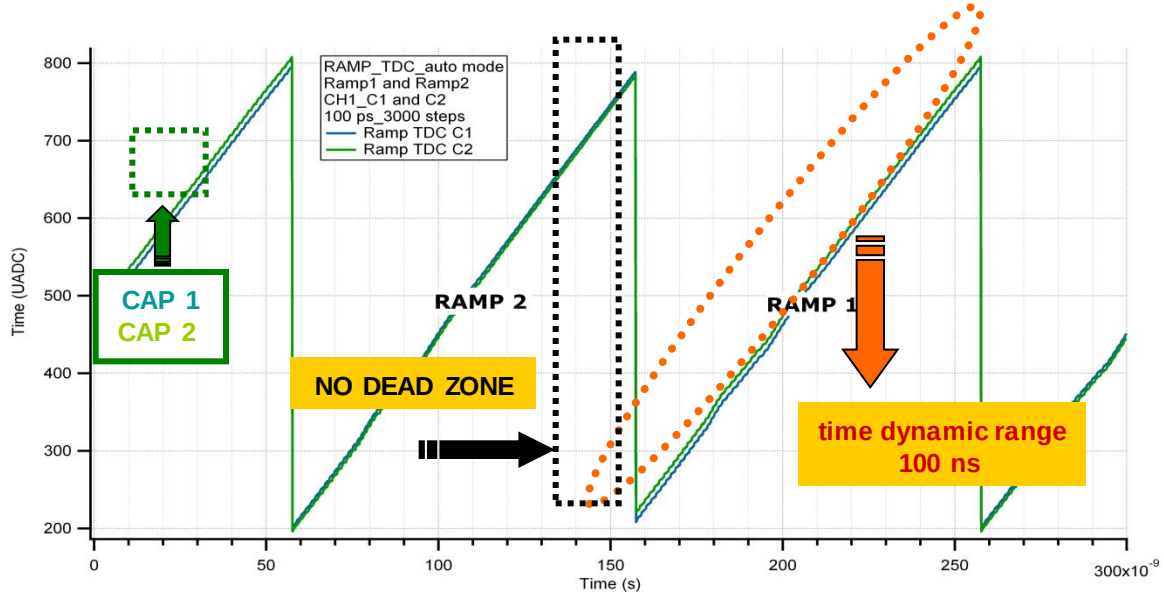
- **Coarse time** made with 2 overlapped counters :
  - 24-bit gray counter @ 10 MHz
  - 1-bit counter @ opposite edge
- 100 ns steps
- Overflow @ 1.67 seconds
- **Fine time** made with 2 overlapped TAC ramps
- 100 ns dynamic range
- 1 ns step
- Automatic selection of valid ramp





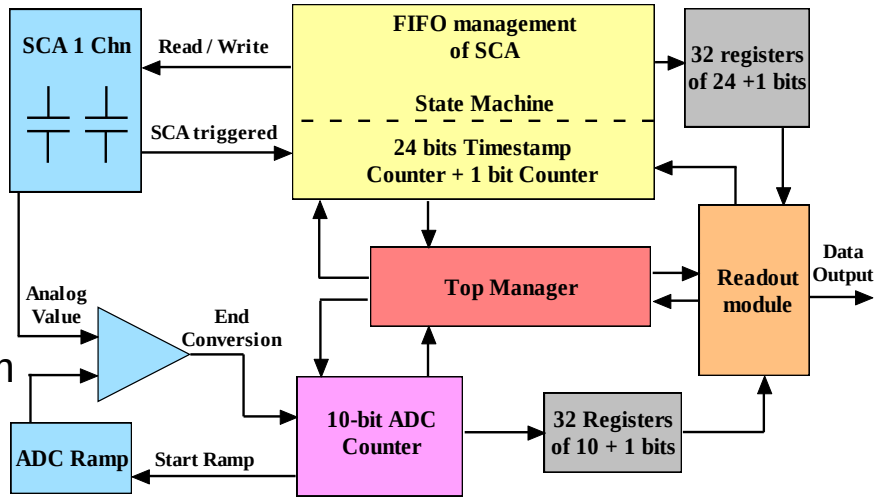
Time dynamic range	100 ns
"Blind zone"	0
linear zone	100 ns
Ramp 1 linear	± 1 ns
Ramp 2 linear	± 1 ns

Time overall measurements



Digital part

- 4 modules:
  - **Acquisition**: Analog memory (SCA) management
  - **Conversion**: Wilkinson ADC management and memory writing
  - **Read Out**: RAM read out to external system
  - **Top manager**: Global sequencer



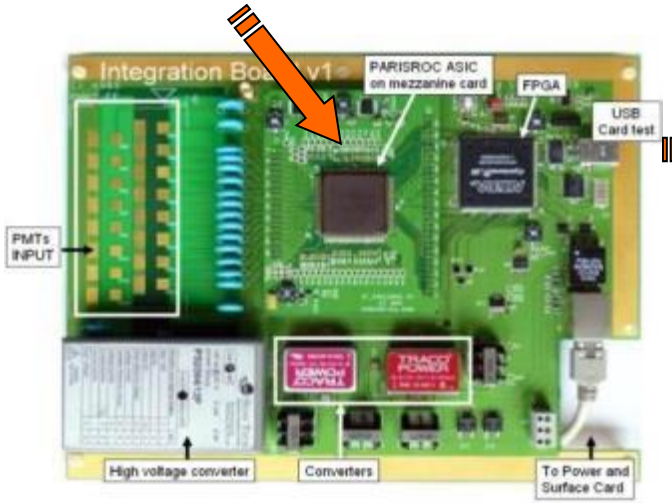
- **Selective readout: only hit channels are readout**
  - Readout clock : 40 MHz
  - Max Readout time (16 ch hit) : 25 µs
  - 51 bits of data / hit channel
  - Hit rate / ch : 5 KHz

Worst case	PARIROC 2
Conversion Time	26 µs
Readout Time	25 µs
Max total cycle duration	51 µs

Readout frame	PARIROC 2
Channel number	4
Coarse time counter	24
Extra Coarse time	1
Gain used	1
Charge converted	10
Fine time (TDC) used	1
Fine time (TDC) converted	10
Total	51 bits

PMm^2 demonstrator

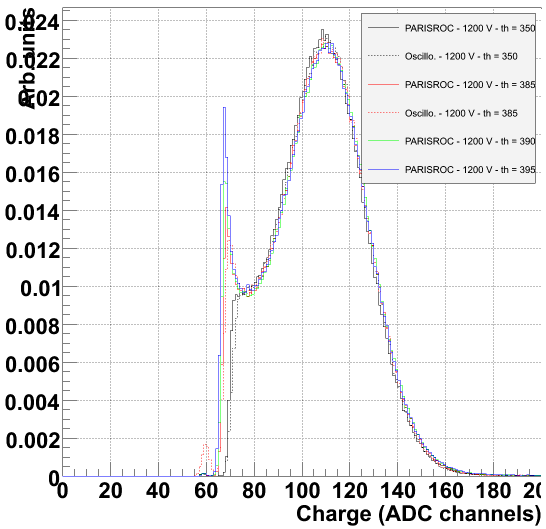
PARISROC2 chip



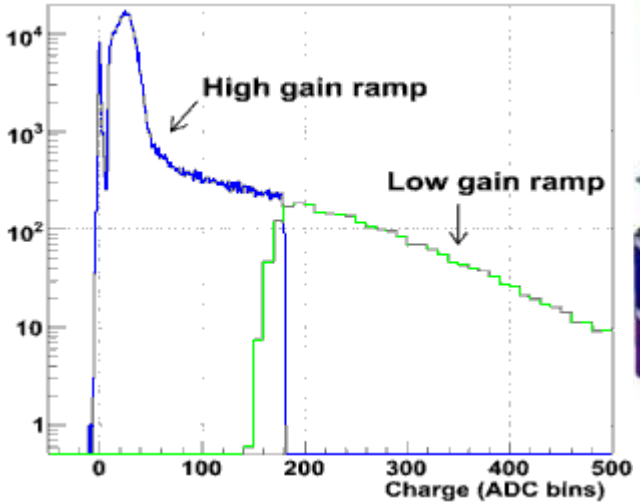
Watertight box

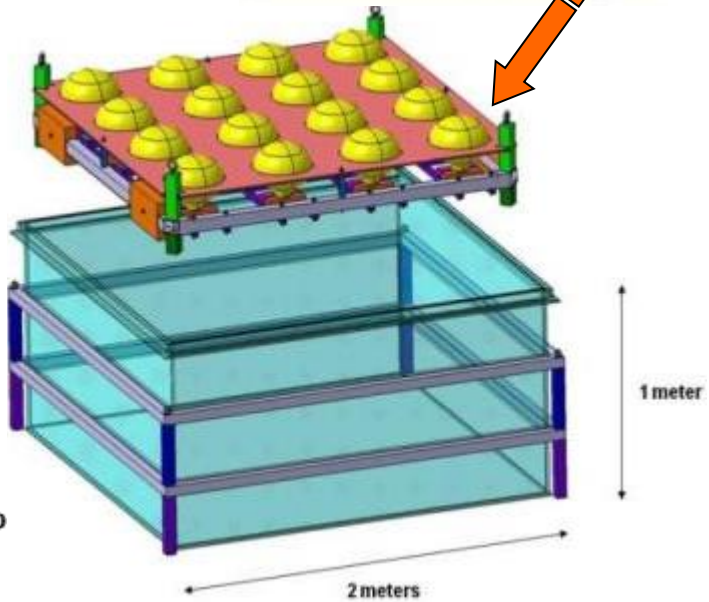
2m x 2m array

1-in (XP3102) single p.e. noise spectrum.

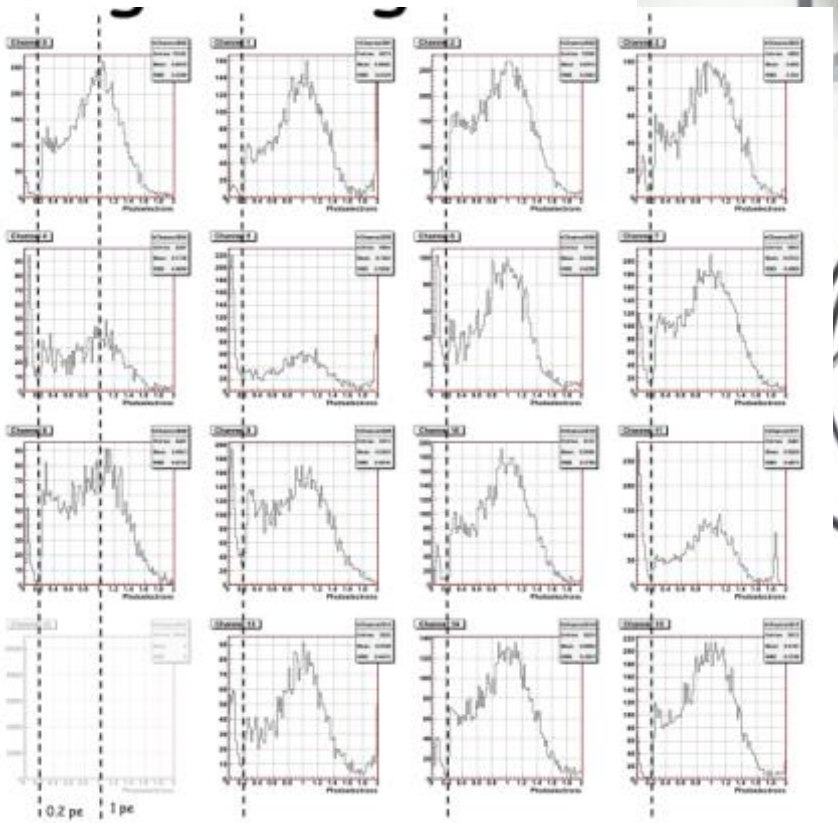


8-in (Hamamatsu R5912)
Single p.e. noise spectrum.





First full scale tests



PMm^2 demonstrator provided by IPNO+LAL/OMEGA+LAPP+ULB

LHAASO :*Large High Altitude Air Shower Observatory*

Omega

Combination of various detectors :

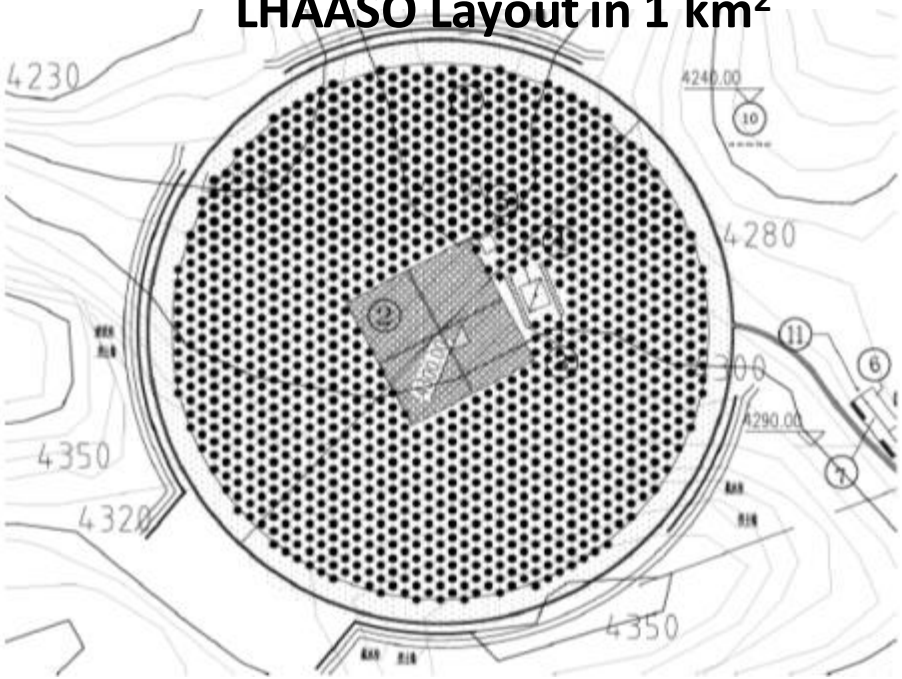
90km2 Water Cherenkov Detector array (WCDA).

24 **W**ide **F**ield of view **C**herenkov/**F**luorescence **T**elescope **A**rray (WFCTA).

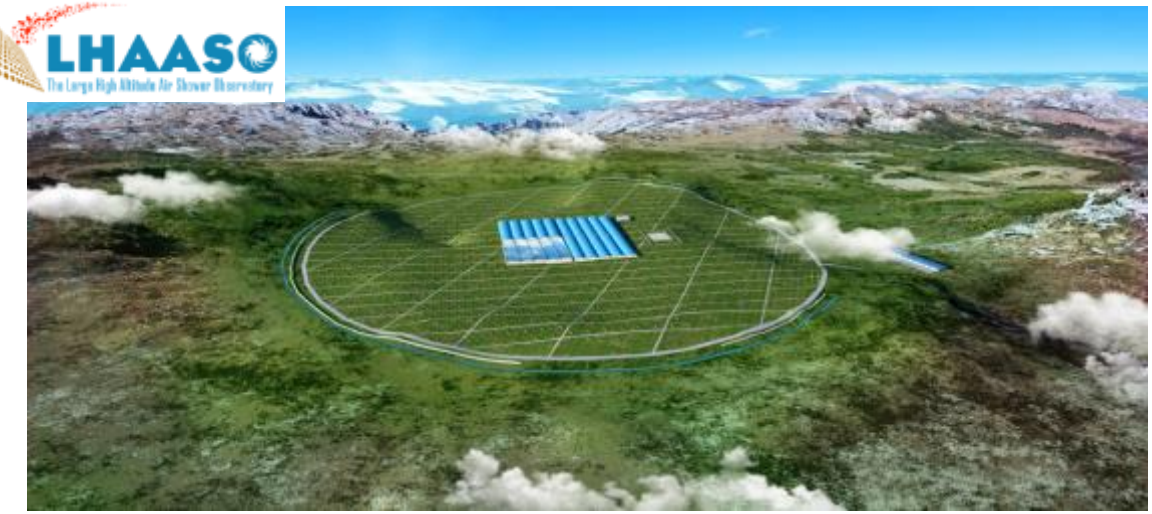
6100 Scintillator detectors and 1200 μ-detectors form an array covering 1 km^2 (KM2)

400 burst detectors for high energy secondary particles near the core of air showers

LHAASO Layout in 1 km^2



LHAASO site :
Sichuan province
(China)
4400 m



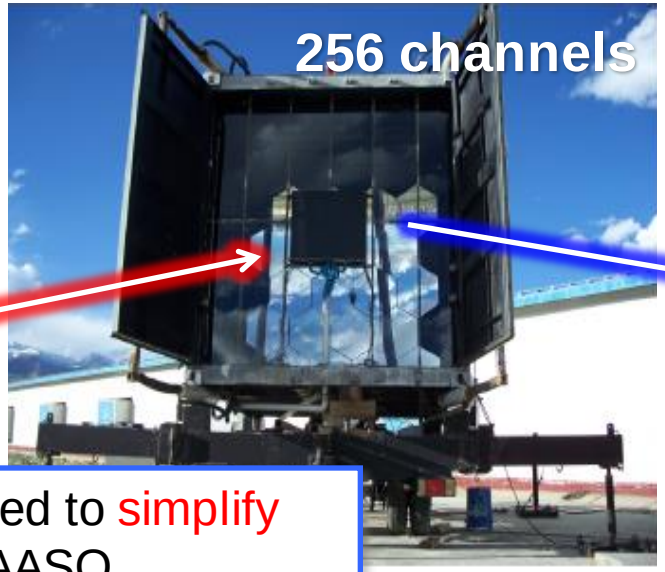
Challenge for electronics

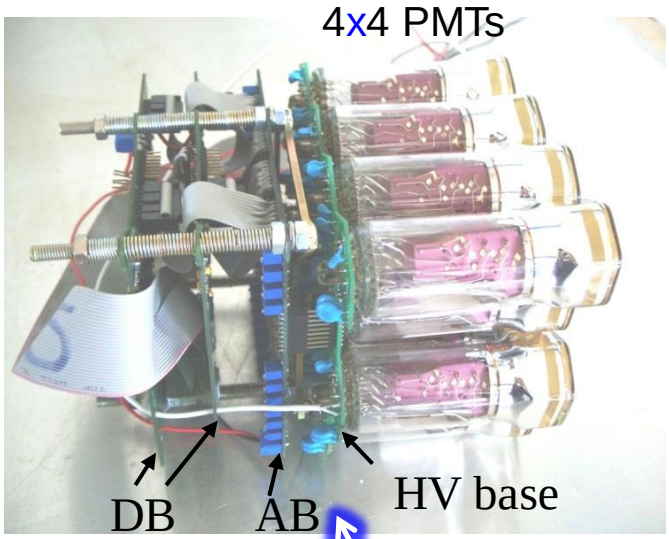
- ✧ High altitude and low air pressure ➔ *decreased heat dissipation*
- ✧ Large number of channels ➔ *increased density, complexity and power consumption*
- ✧ Harsh environment and remote location ➔ *require stability, reliability and maintainability*
- ✧ Design based on IC ➔ *simplified design, decreased power consumption, increased reliability*

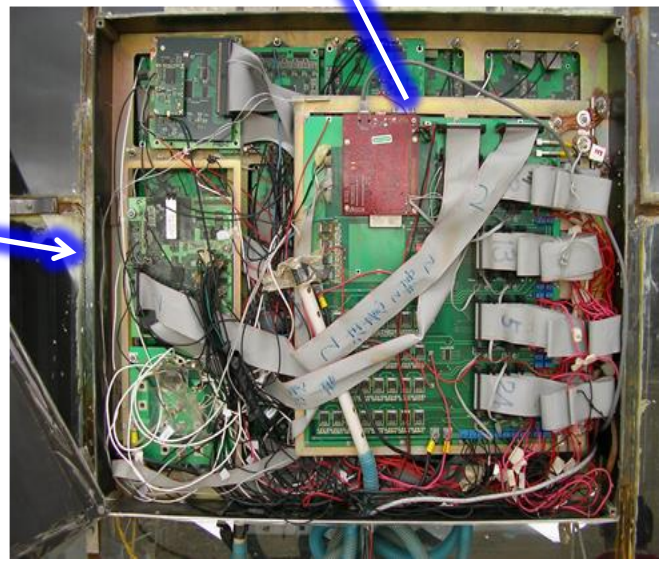
- Compact design
- High stability
- High reliability
- Easy to maintain

We focused on WFCTA at first

The ASICs can be used to simplify the electronics of LHAASO







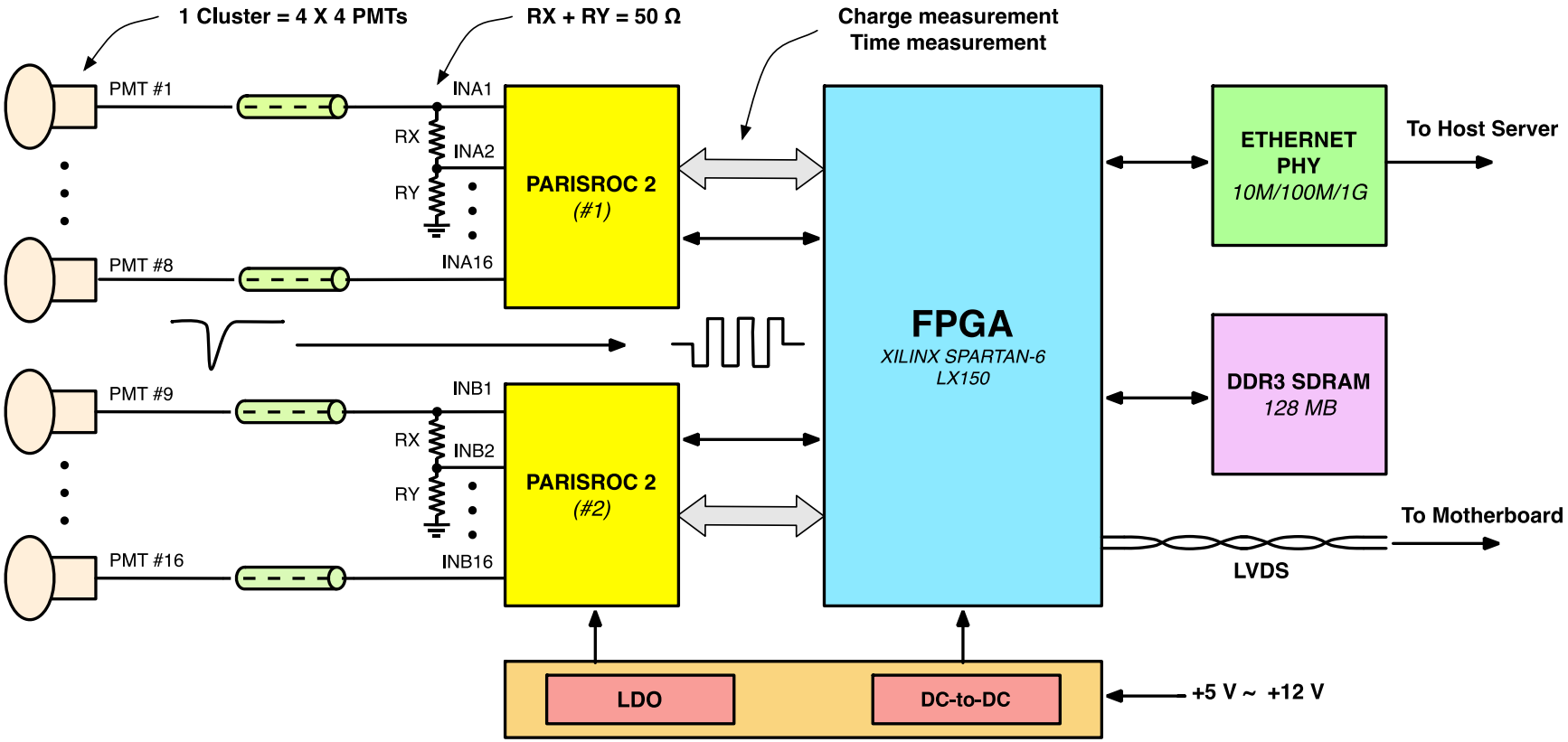
Prototypes in YBJ, Tibet

PARISROC for WFCTA

Property	WFCTA Specifications	Support or not
Signal polarity	*Negative (Anode) or Positive (Dynode)*	✓
Dynamic range	*160fC to 240pC, （10pe to 15000pe @ Gain = 10^5）*	✗ *(need combine two channels into one)*
Resolution	*< 20% @ 10pe and < 5% @ 15000pe*	✓
Nonlinearity	*< 2% or <±1%*	✗ *(need combine two channels into one)*
Time resolution	*20ns (RMS)*	✓
The adjustable threshold	*5pe to 100pe*	✓
Single channel event rate	*10kHz per channel*	✗ *(limited by USB interface and FPGA)*
Width of the signal	*6ns to 50ns (FWHM) for Cherenkov light*	✓
Pedestal monitoring	*Background of electronics and sky*	
Channels	*1024 channels per telescope*	
Power consumption	*260W per telescope*	

Performance limitations
- FPGA (Altera Cyclone III)
- USB Interface (FTDI FT245X)
- Specific ports (External trigger)

Schematic of the front-end board



- Two PARISROC 2 chips with 2 groups of 16 inputs
- Voltage dividers at input to extend the dynamic range and keep nonlinearity low
- New powerful FPGA (Xilinx Spartan-6 LX150) as the central controller
- Multiple transferring protocols, such as 1G Ethernet, LVDS
- Power supply: +5 V to +12 V
- Can be easily adapted to any other experiment with similar requirements

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IPN, Orsay, France

Picture of the front-end board

Trenz TE0600-01

- Spartan-6 LX150: 147K
- Size: **50 mm × 40 mm**
- **10M/100M/1000M Ethernet**
- 2 x 16-bit 256MB DDR3 SDRAM
- 128Mb (16 MB) SPI Flash
- Robust board-to-board connectors (B2B) LSHM up to 10 GHz / 20 Gbps
- Up to 52 differential I/O
- Up to 109 single-ended I/O

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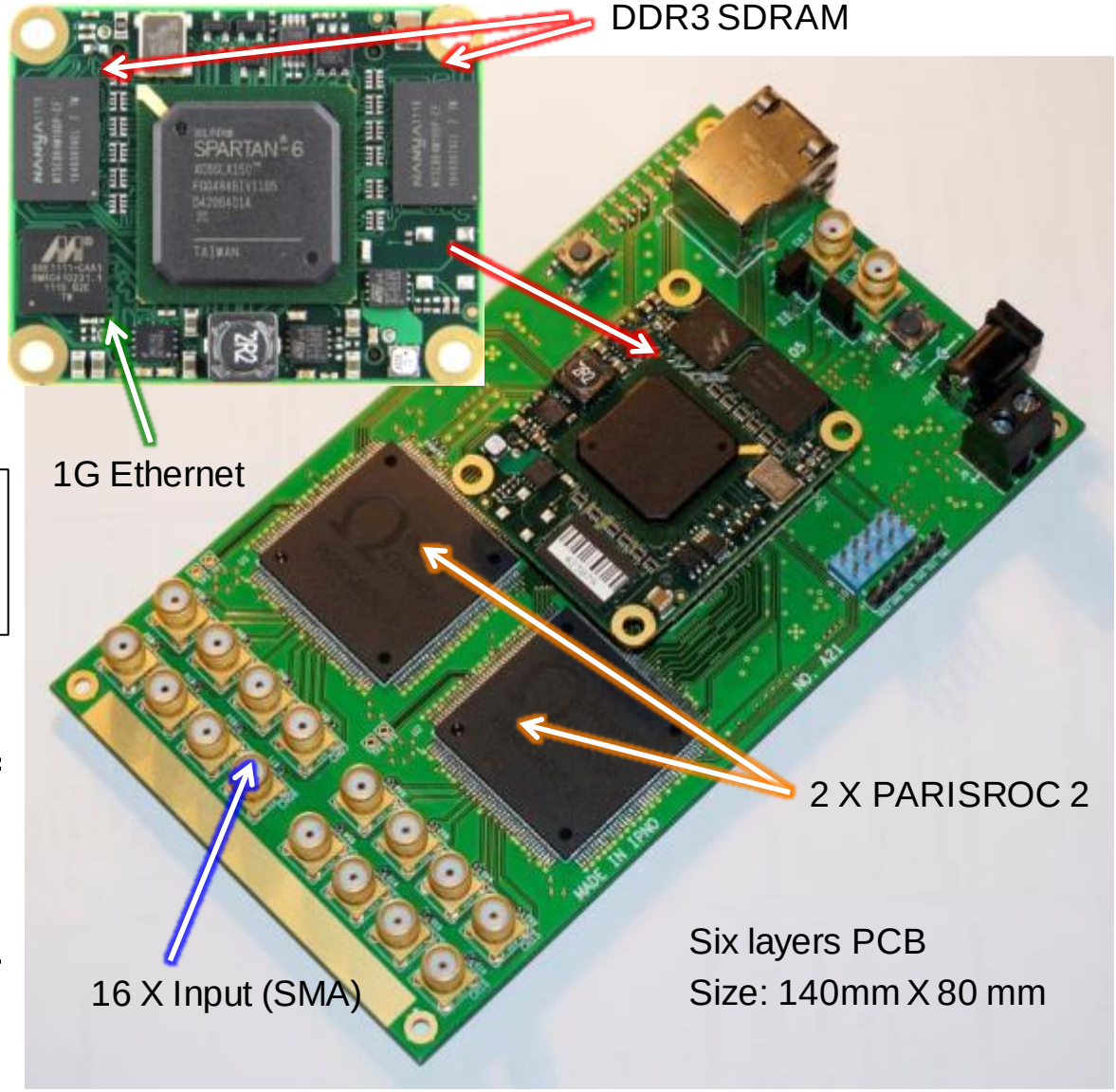
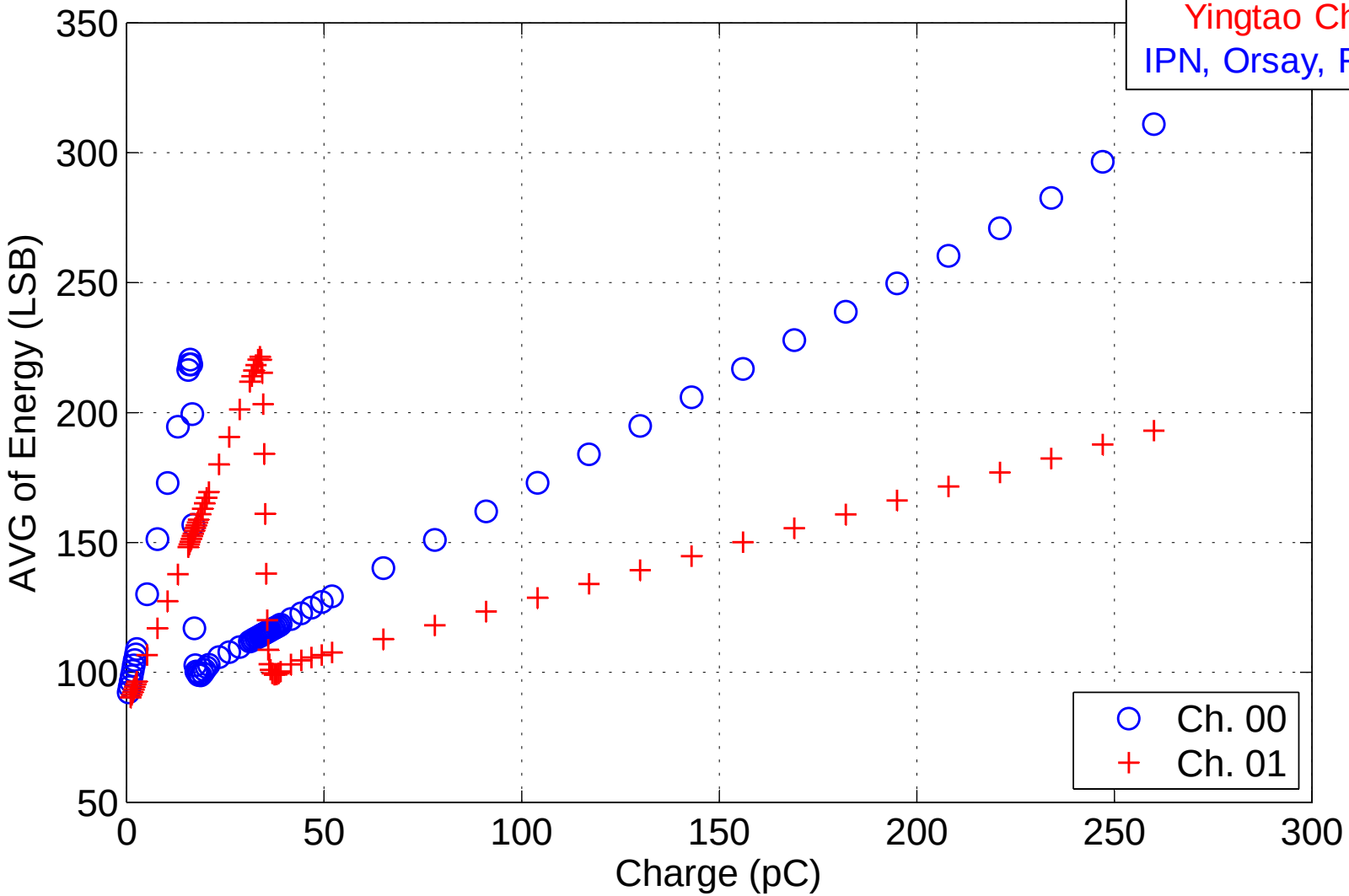
Unit	Power Consumption
PARISROC 2 X 2	~ 1.0W
Ethernet Interface	~ 1.1W
FPGA & Peripherals	~ 0.9W
	~ 3.0W (2.98W meas.)



Dynamic range & non-linearity

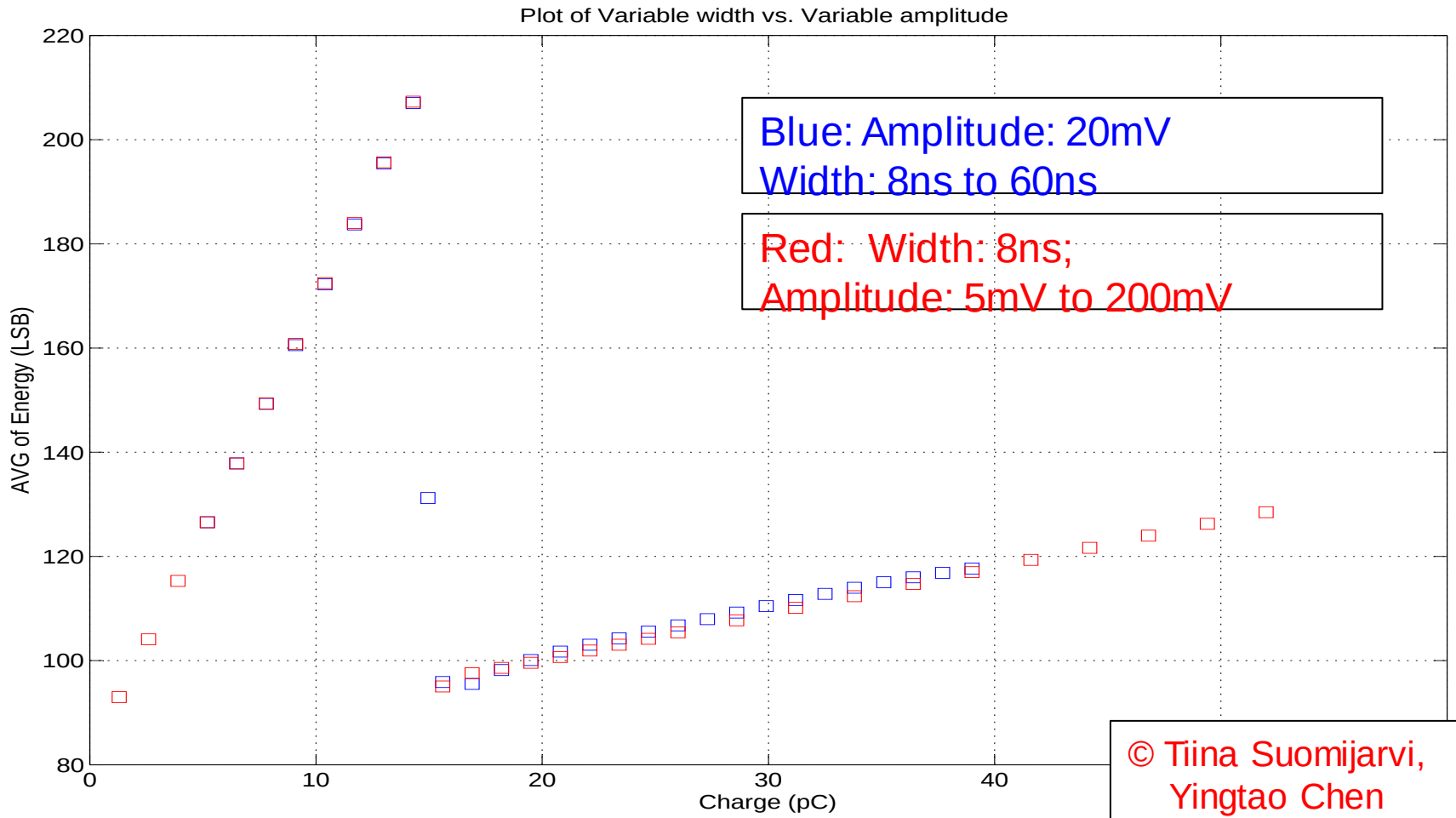
Voltage divider at the input extends the dynamic range and keeps nonlinearity low

DR: 0.16 pC to 250 pC with INL < ±1%



Variable width vs. variable amplitude

PARISROC can deal with signals with same charge but different shape.



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1 mV ≈ 260 fC; 0.6 mV ≈ 1 pe ≈ 160 fC @ PMT Gain 10^6

Single photoelectron spectrum (CR303)

By using external trigger, the SPE spectrum can be easily extracted with good P/V ratio.

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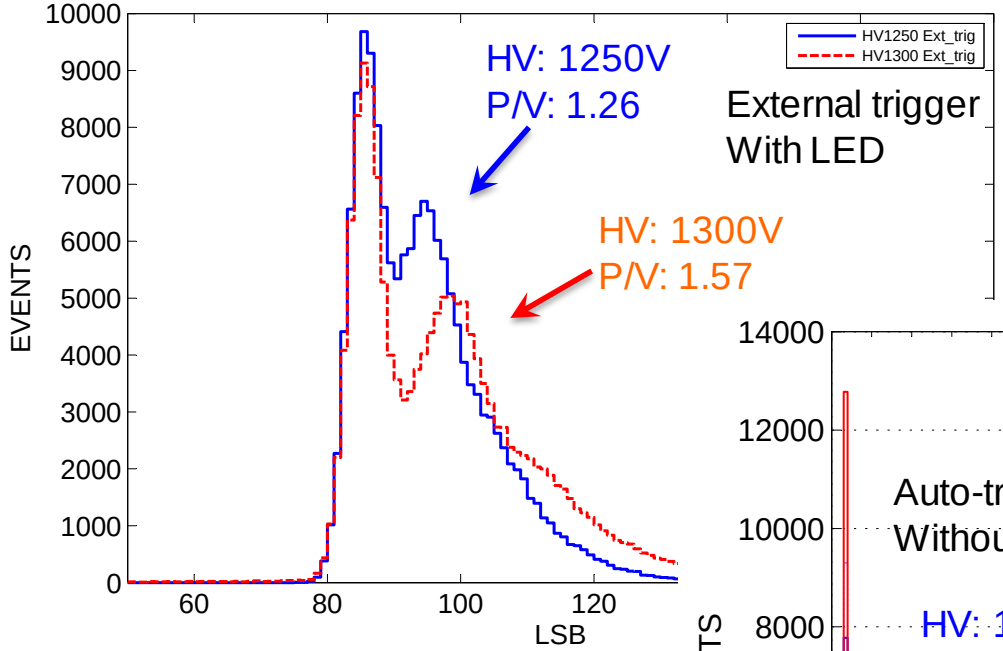

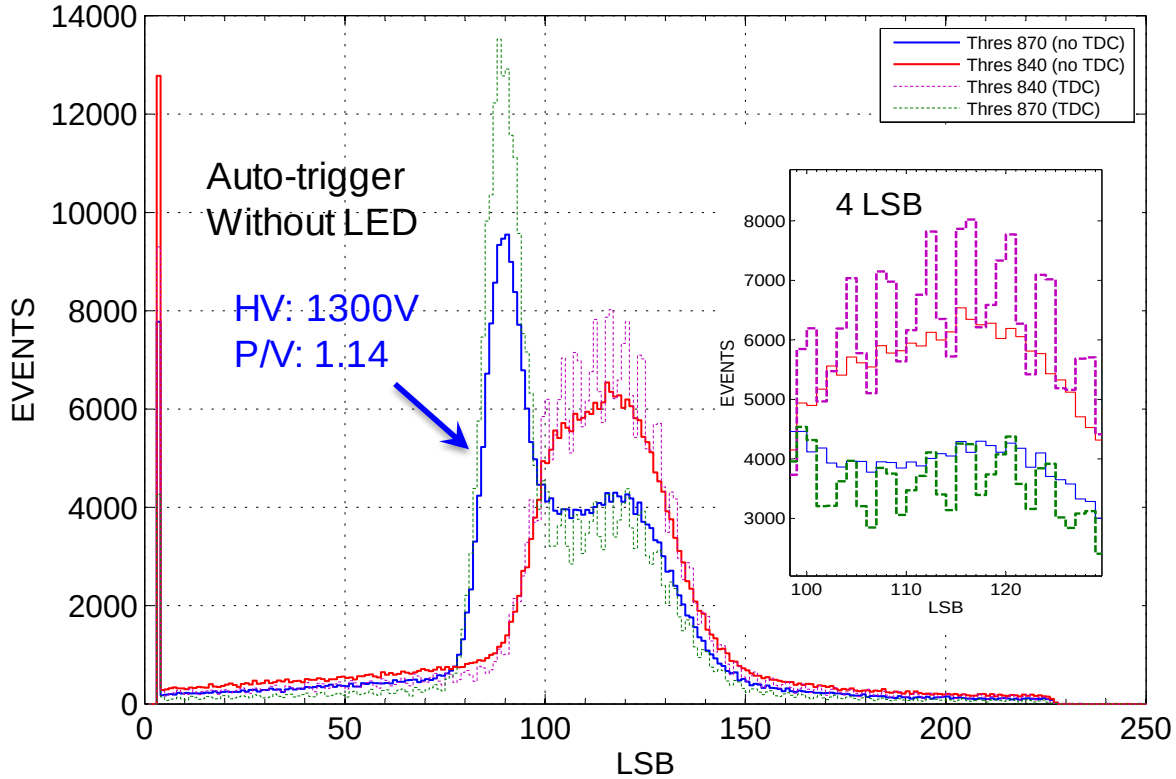

The periodical crosstalk from TDC unit will affect the accuracy of charge measurement when the internal trigger is used.

However, the threshold will not affect the location of the pedestal and the SPE peak.

Event rate & pedestal monitoring

Event rate (16 channels)

- For 51 bits data and 40 MHz clock
  - Maximum event rate: < 49 kHz (12.75 us)
  - Due to other factors: < 39 kHz (25.5 us)
- ASIC specification:
  - 20 kHz (best case)
  - 5 kHz (worst case)
- Measurement:
  - TDC on: ~ 24 kHz (53.24 Mbit/s)
  - TDC off: ~ 37 kHz (82.14 Mbit/s)

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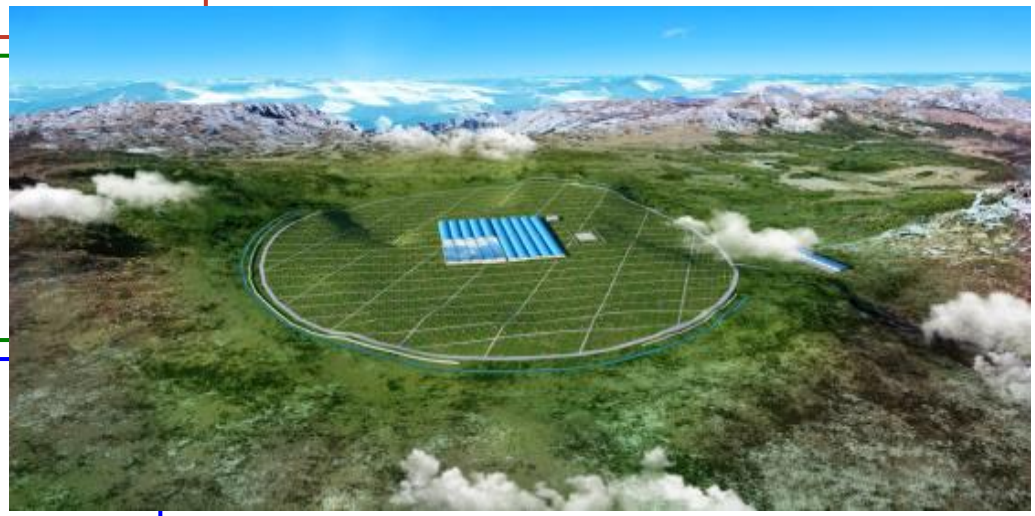
Performance

✓ Not related to
– Amplitude & Width
✓ Limited by
– FPGA & Interface



Pedestal monitoring

– Electronics: external trigger
– Sky: counting rate

LAGUNA-LBNO

LAGUNA-LBNO : **L**arge **A**pparatus for **G**rand **U**nification and **N**eutrino **A**strophysics - **L**ong **B**aseline **N**eutrino **O**scillations.

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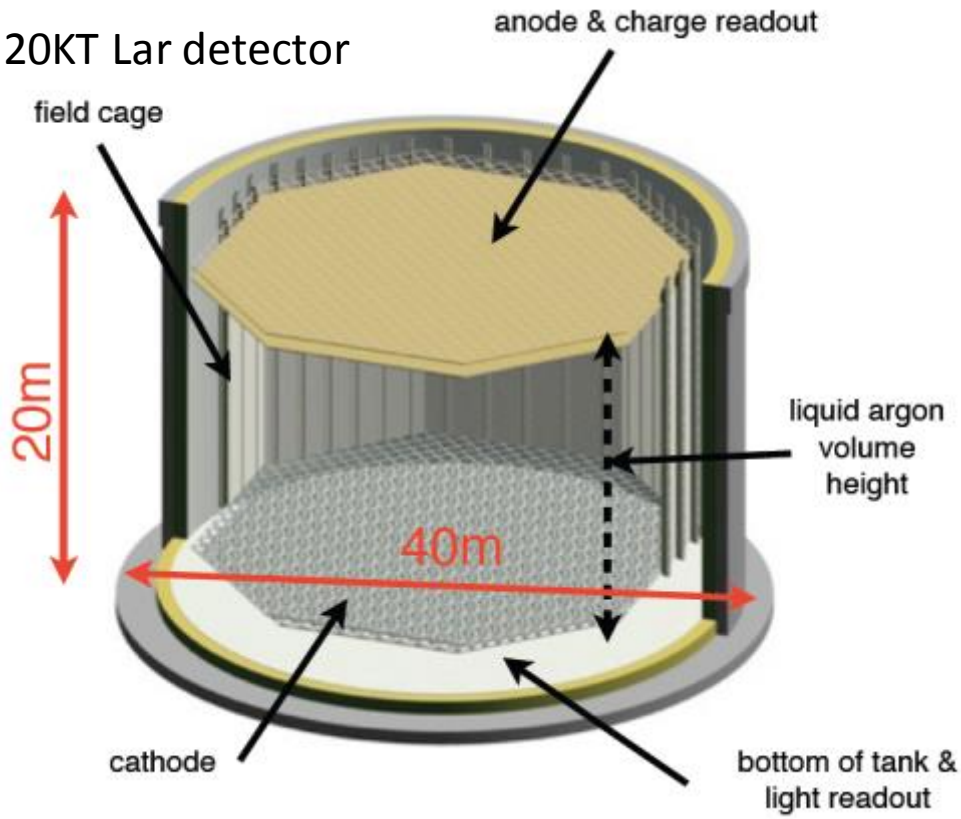
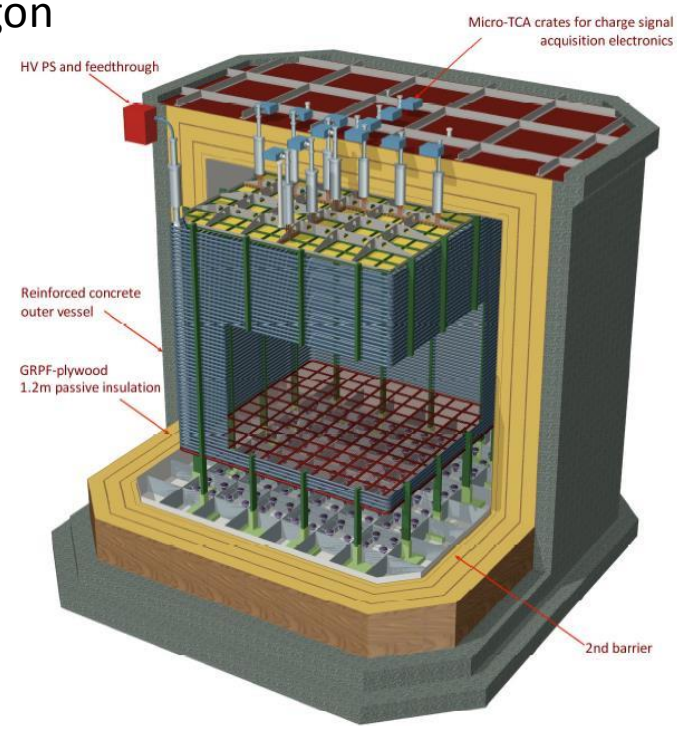
APC, Paris, France

20KT Lar detector



Large scale demonstrator with 7680 electronic channels in liquid Argon



SUMMARY

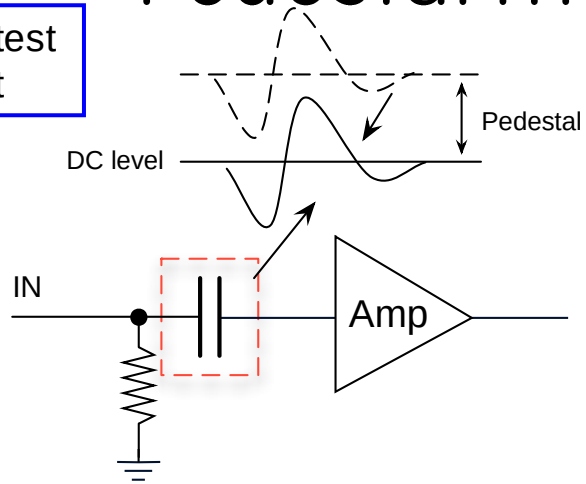
- PARISROC chip could be used as readout for large PMT area experiments
  - Data processing on detector : cost effective
  - Shared HV : reliability issues
  - Digital data : simpler feedthrus / signal integrity
  - Attractive for large systems

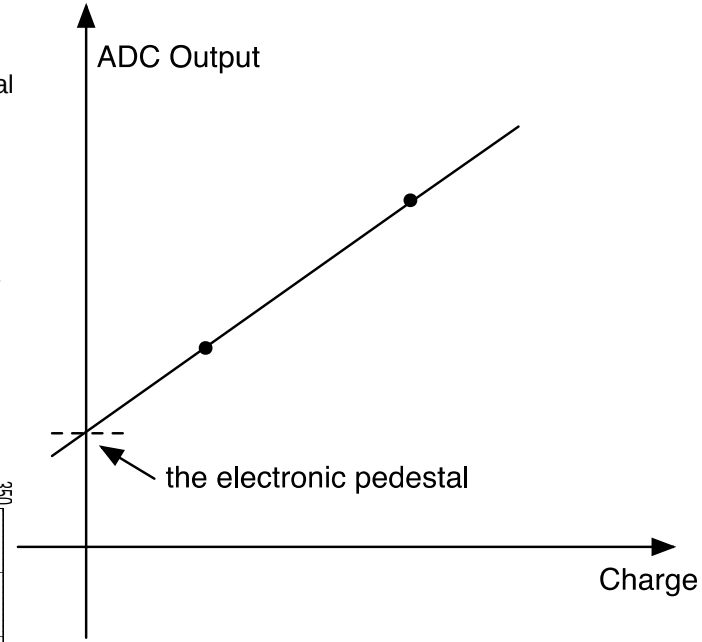
- Chip is now being studied by 2 experiments :
  - LHAASO : chip could be used directly for Cerenkov mode and could be adapted for fluorescence mode.
  - LAGUNA : chip can in principle work in LAr and should be tested on cryogenic PMs

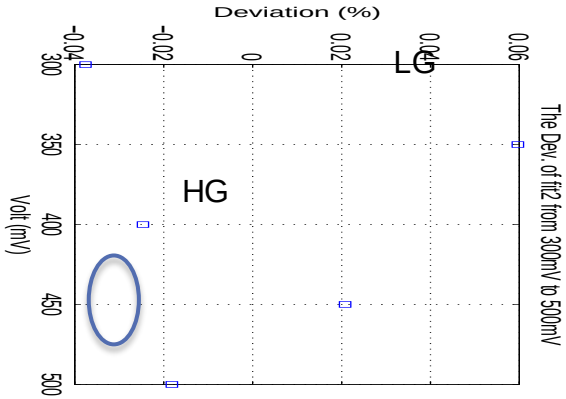
Thank you

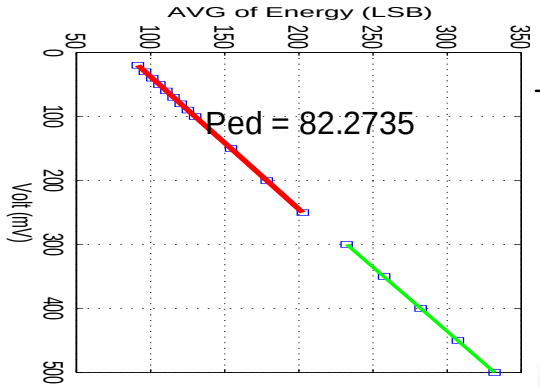
Pedestal monitoring

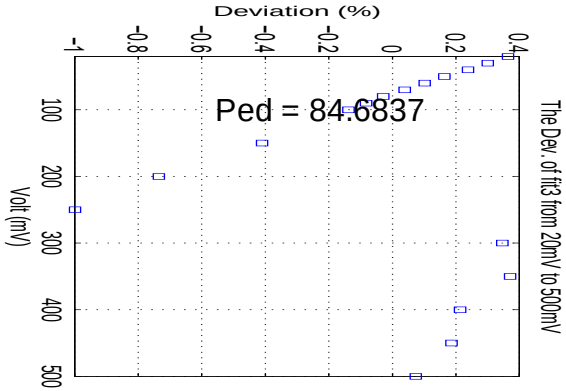
External test input port

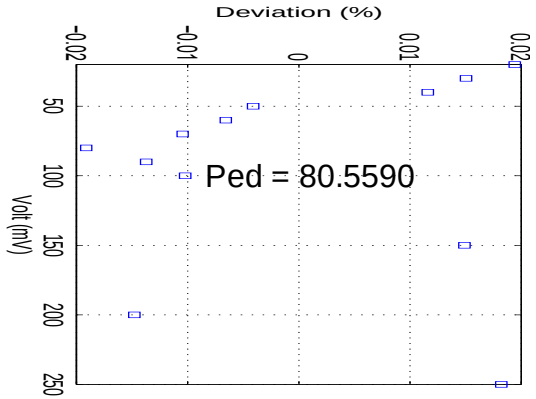


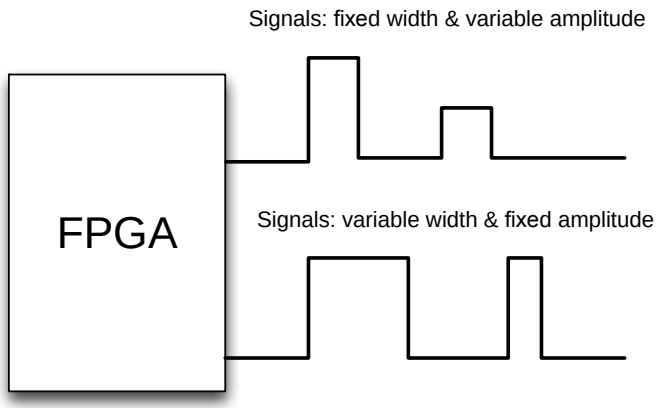








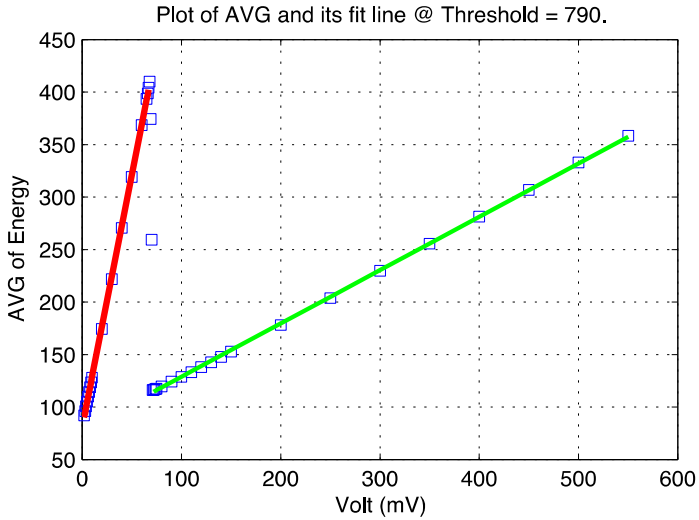


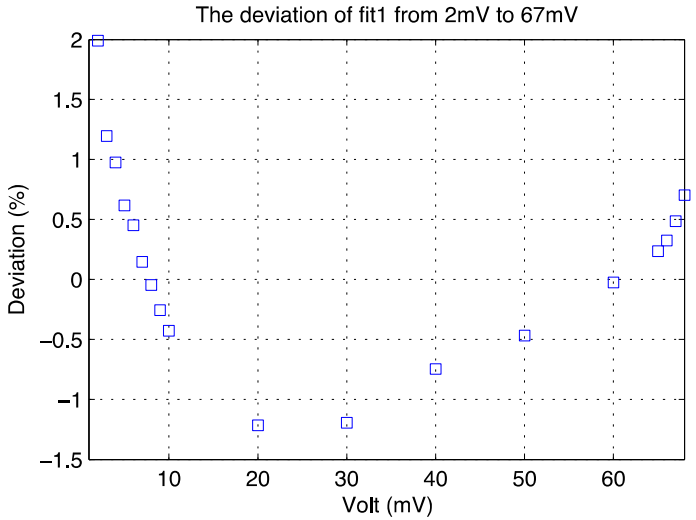


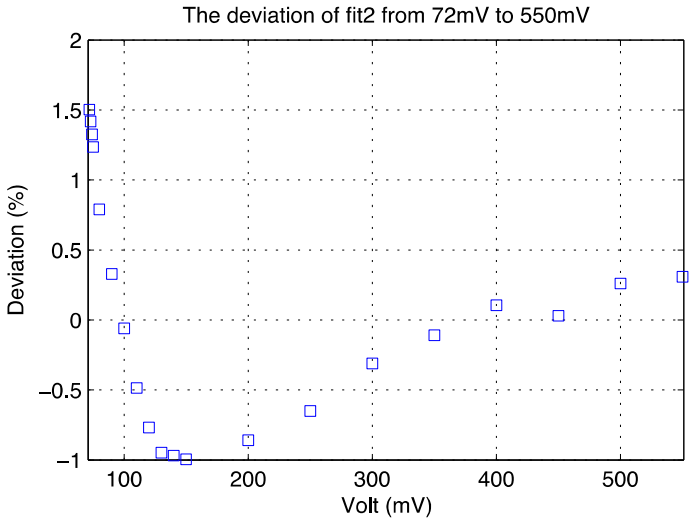
The dynamic range and the linearity

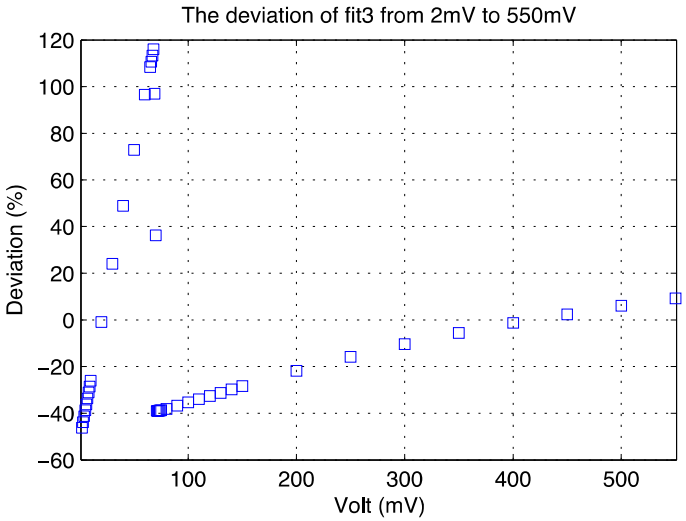
1 mV ≈ 260 fC; 0.6 mV ≈ 1 pe ≈ 160 fC

Default setting: (SSTC = 50 ns, TD = 8); Dynamic range: 2 mV to 550 mV

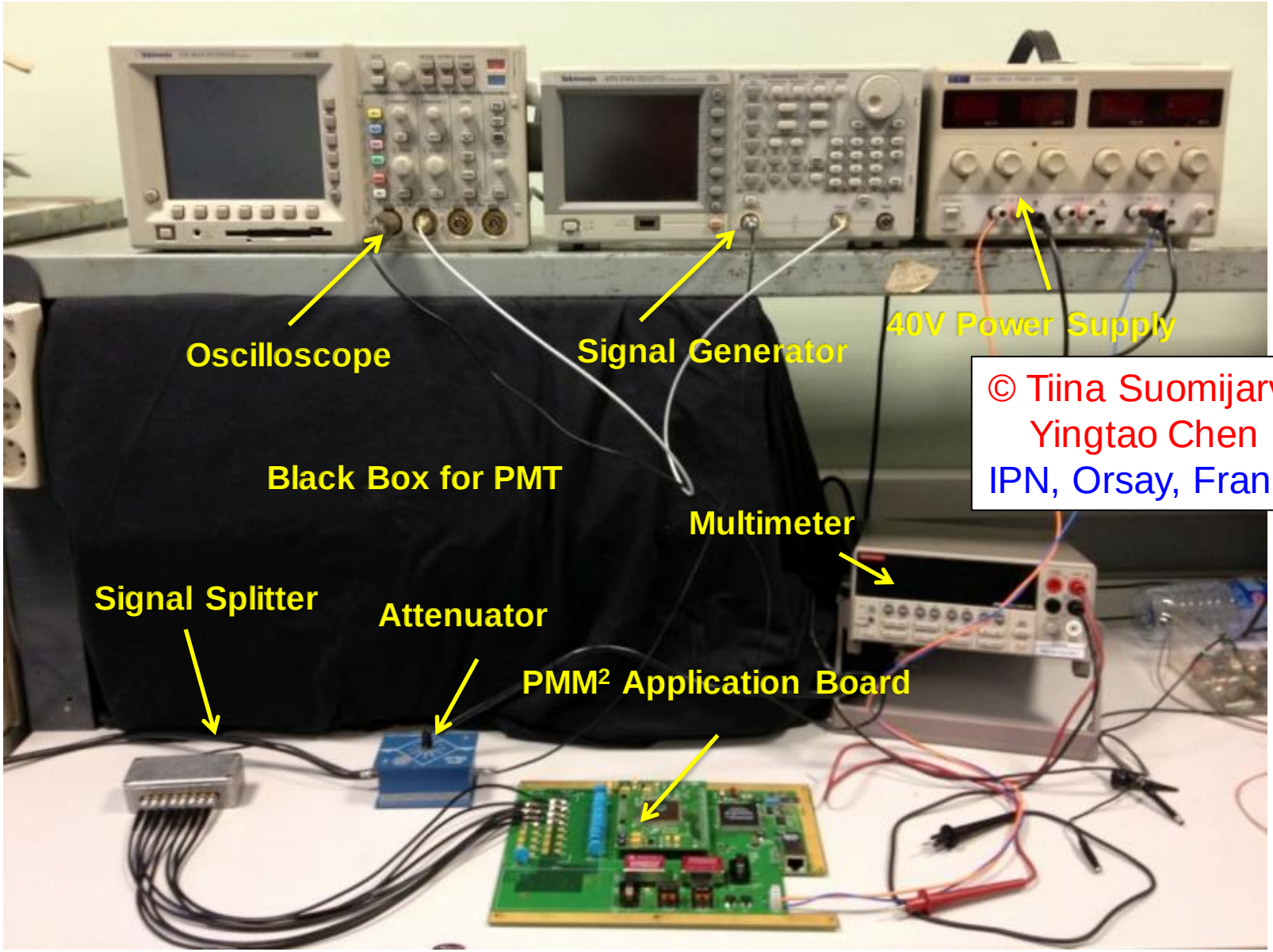








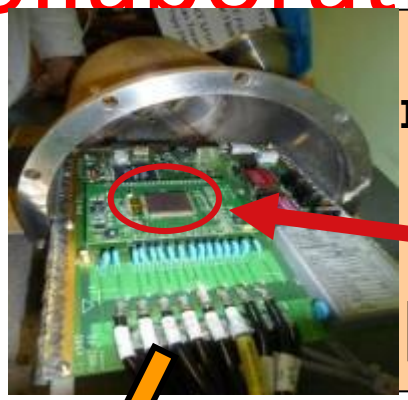
PARISROC Test Bench for LHAASO



© Tiina Suomijarvi, Yingtao Chen
IPN, Orsay, France

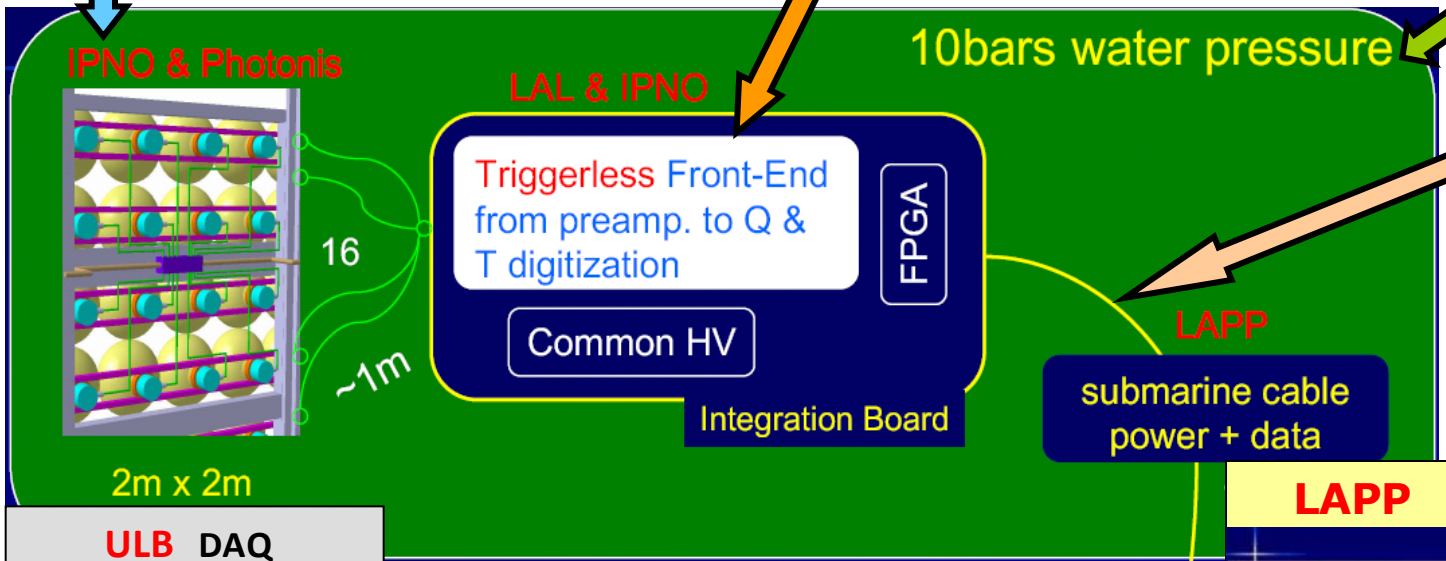
PMM2 Collaboration

IPNO
new shape
glass thickness
Photonis
realization



IPNO:
Integration Board
LAL:
PARISROC
Watertight Box

Pressure vessel
(BNL,USA)



LAPP
Hydrocable

ULB DAQ

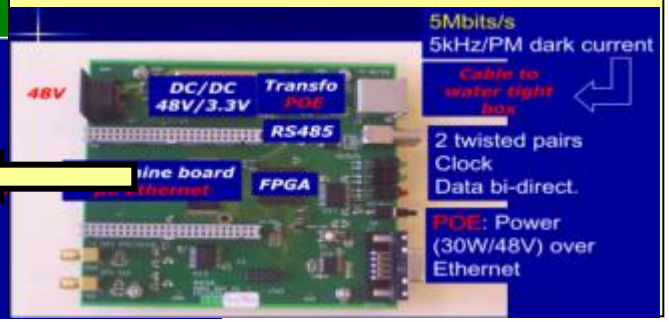
ULB

TCP/IP

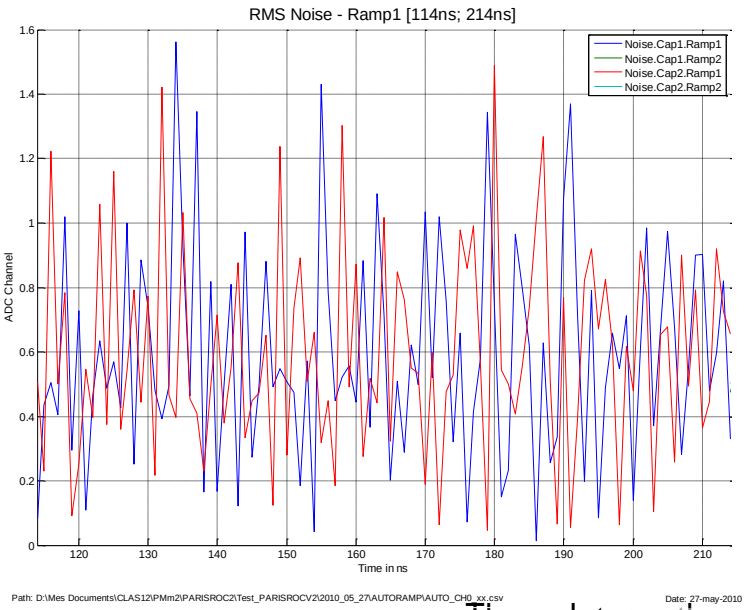
µControler | FPGA

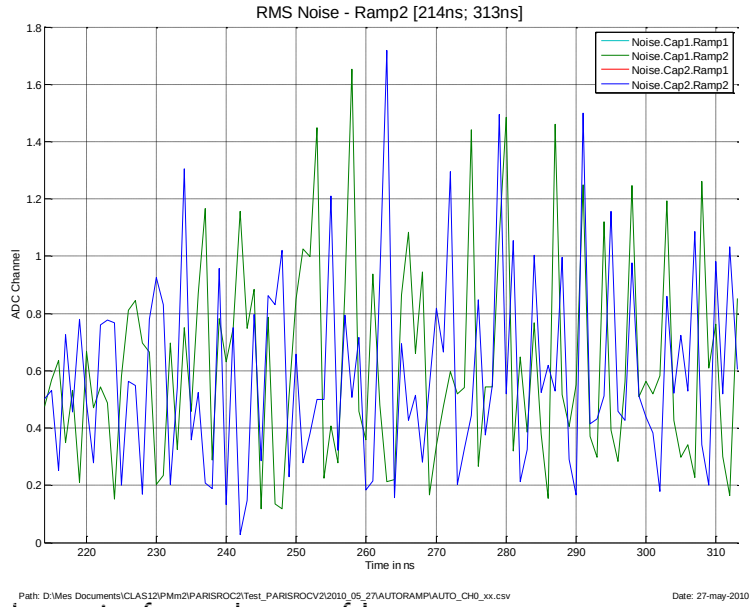
Power + Decoding Board

LAPP Submarine Card



PARISROC TDC ramps Noise





These plots are the row data noise for each step of 1ns.
Do not forget that the generator have a 107ps jitter.

Capacitor	Row Noise (Quadratic Mean)	TDC Noise (Quadratic Mean)	Max TDC Noise
Ramp1.Cap1	0.67ch = 146ps	99ps	322ps
Ramp1.Cap2	0.68ch = 148ps	102ps	306ps
Ramp2.Cap1	0.71ch = 154ps	111ps	341ps
Ramp2.Cap2	0.68ch = 147ps	101ps	356ps