Aerospace

Low-Power Analogue Receiver ASIC for Space Telecommand Applications

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SITAEL

Outline

Introduction

General Overview of Architecture

Description of main parts

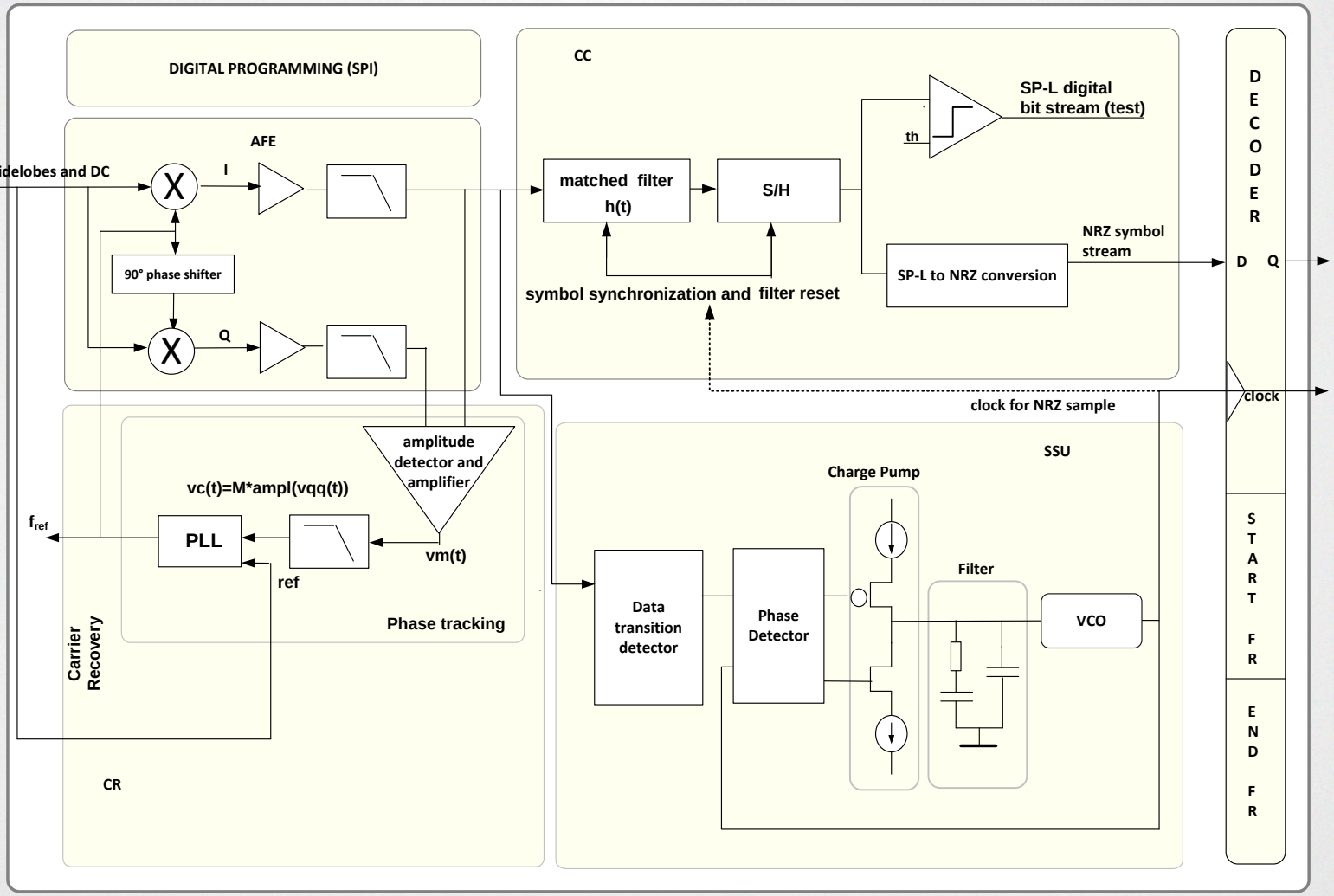
- Receiver Section
- Symbol Synchronization Unit
- Codify Conversion
- Start Frame Recognizer
- Data Memory
- Decoder Core

Conclusions

Introduction

- Nowadays, **on-board tele-command receivers** for space applications consume an important percentage of the offered power of the satellite.
- **Decoders**, in charge of elaborating received data and of providing error correction are currently implemented on *large FPGAs*.
- The increasing communication and data storage complexity and capacity makes the applicability of *error correction codes in a digital domain* more and more expensive in terms of **hardware resources** and **power consumption.**
- In the last 10 years, the **analogue decoding** has been recognized for its potential to decrease the overall power consumption
- Analogue domain implementation of error correction codes provides the following *advantages*:
  - Benefit from **similarity** between the *mathematical operations* required by the algorithms and the *physical laws* governing the circuit
  - Total system **efficiency**, because the analogue decoder is *much smaller* than its digital counterpart and consumes about one order of magnitude *less power* at the same frequency
  - High **modularity** design more immune to noise, by means of *differential operation*
  - Capability of providing a finer estimation of the *logic state of a single information unit* with respect to digital implementations (**no quantization**)

ASIC Block Diagram



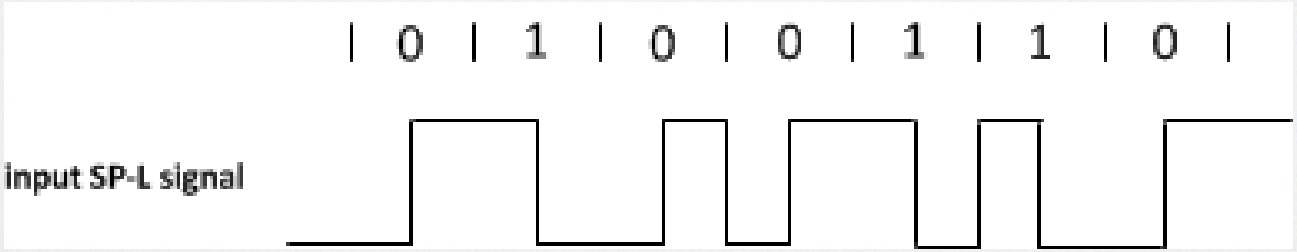
Architecture Description

- The analogue input to the ASIC is a 8 MHz intermediate frequency, DC component and the side-lobes of the modulated signal.
- In-Phase and In-Quadrature components of baseband signal are produced internally to the ASIC and they are filtered and amplified inside the AFE (Analog Front End) block after the final down conversion step.
- The CR (Carrier Recovery) section provides to the local mixer a signal with frequency (same as carrier frequency) and phase for down conversion purposes.
- The carrier tracking is performed by extracting the carrier frequency from the received signal by a PLL and by aligning the phase maximizing the signal energy of the In-Phase component.

The SSU (Symbol Synchronization Unit) operates the clock extraction from the baseband PCM/PM/BI-PHASE signal

- The SP-L codify guarantees always at least one transition per clock cycle
- A local PLL tracks the data transition synchronism
- Clock recovery is operated in the digital domain
- Digital configuration adopted for clock recovery needs a matched filtering inside the Codify Conversion block

Example of SP-L (Split Phase Level) signal



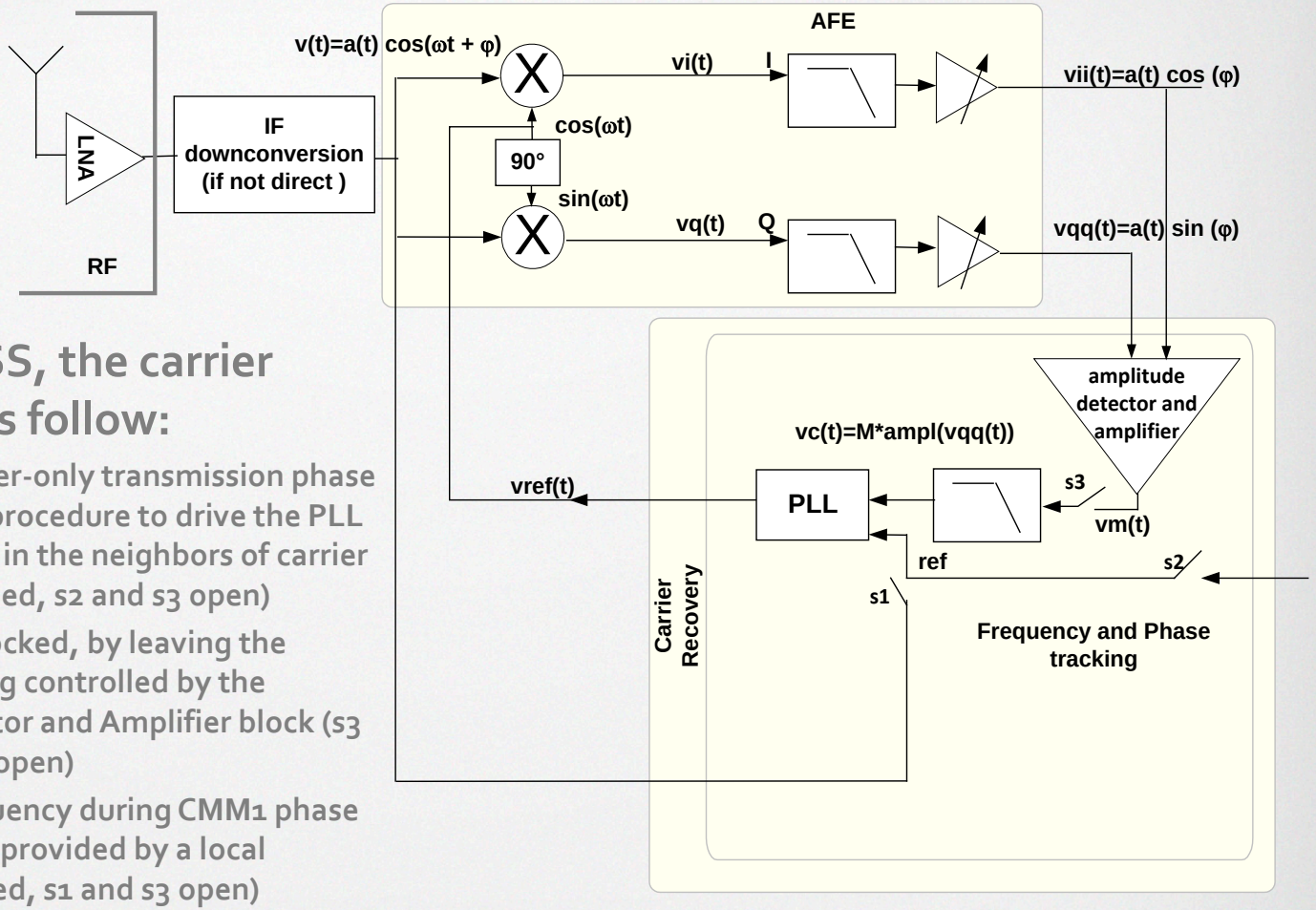
Architecture Description

- The CC (Codify Conversion) section converts the data codify from PCM/PM/BI-PHASE to NRZ.
- The PCM/PM/BI-PHASE to NRZ conversion task is performed by differentiating the left and right half symbol.

- The Decoder Block presides to data decoding and provides decoded digital data and clock output.
- It is triggered when a Start Frame pattern is recognized and the decoding is stopped once an End Frame command is detected.

It is composed by Analogue Front-End (AFE) and Carrier Recovery (CR) blocks

- The IF is fixed to 8MHz

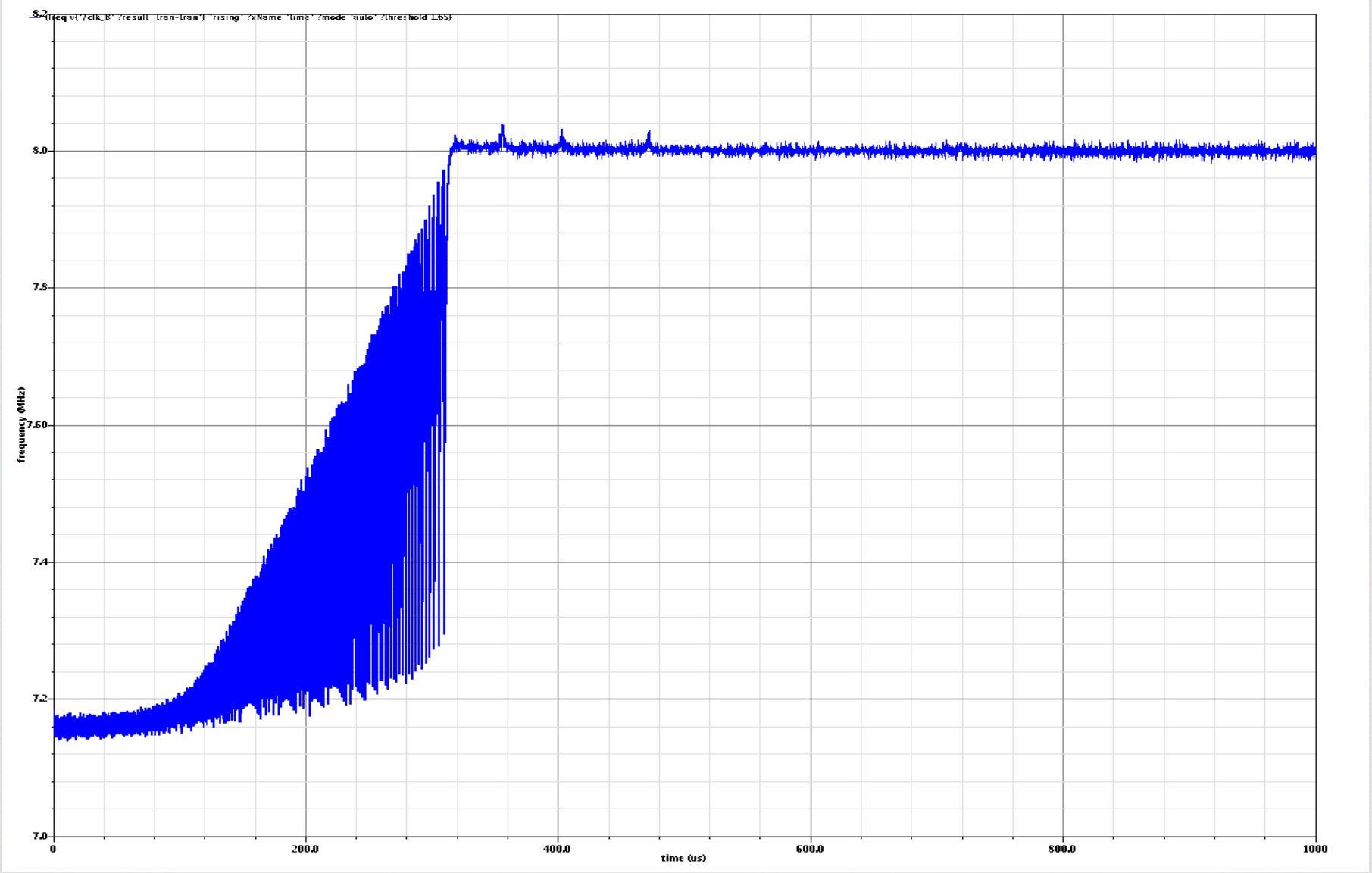


- According to ECSS, the carrier recovery works as follow:
  1. by using the carrier-only transmission phase CMM1 of PLOP2 procedure to drive the PLL output frequency in the neighbors of carrier frequency (s1 closed, s2 and s3 open)
  2. Once the PLL is locked, by leaving the internal VCO being controlled by the Amplitude Detector and Amplifier block (s3 closed, s1 and s2 open)
  3. The training frequency during CMM1 phase can be optionally provided by a local oscillator (s2 closed, s1 and s3 open)
  4. s3 and s1/s2 switch's activity is mutually exclusive in time and it is governed by the PLL lock signal

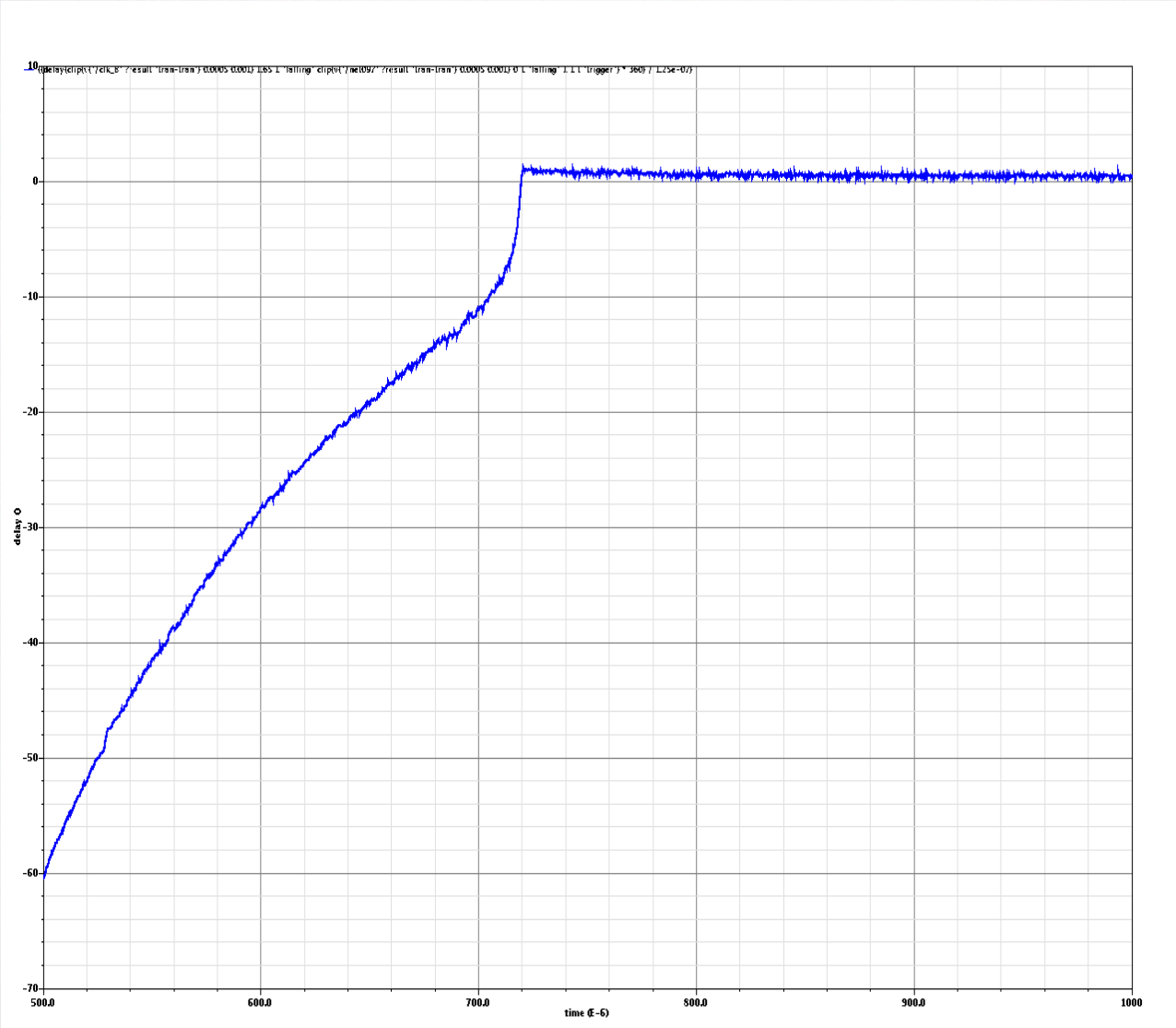
Receiver Section Description

- The phase correction implements a Costas loop and it re-phases the PLL output signal
- The PLL output is used for local mixing (demodulation) to maximize the *in-phase* signal energy with respect to the *in-quadrature* signal energy
- Downstream circuitry accepting the demodulated signal operates only on the *in-phase* demodulated baseband signal
- The amplifier and filter inside the AFE chain condition the down-converted signal and filter the out-of-band signal components
- Continuous time bi-quad filters have been used in order to reject the image frequency components

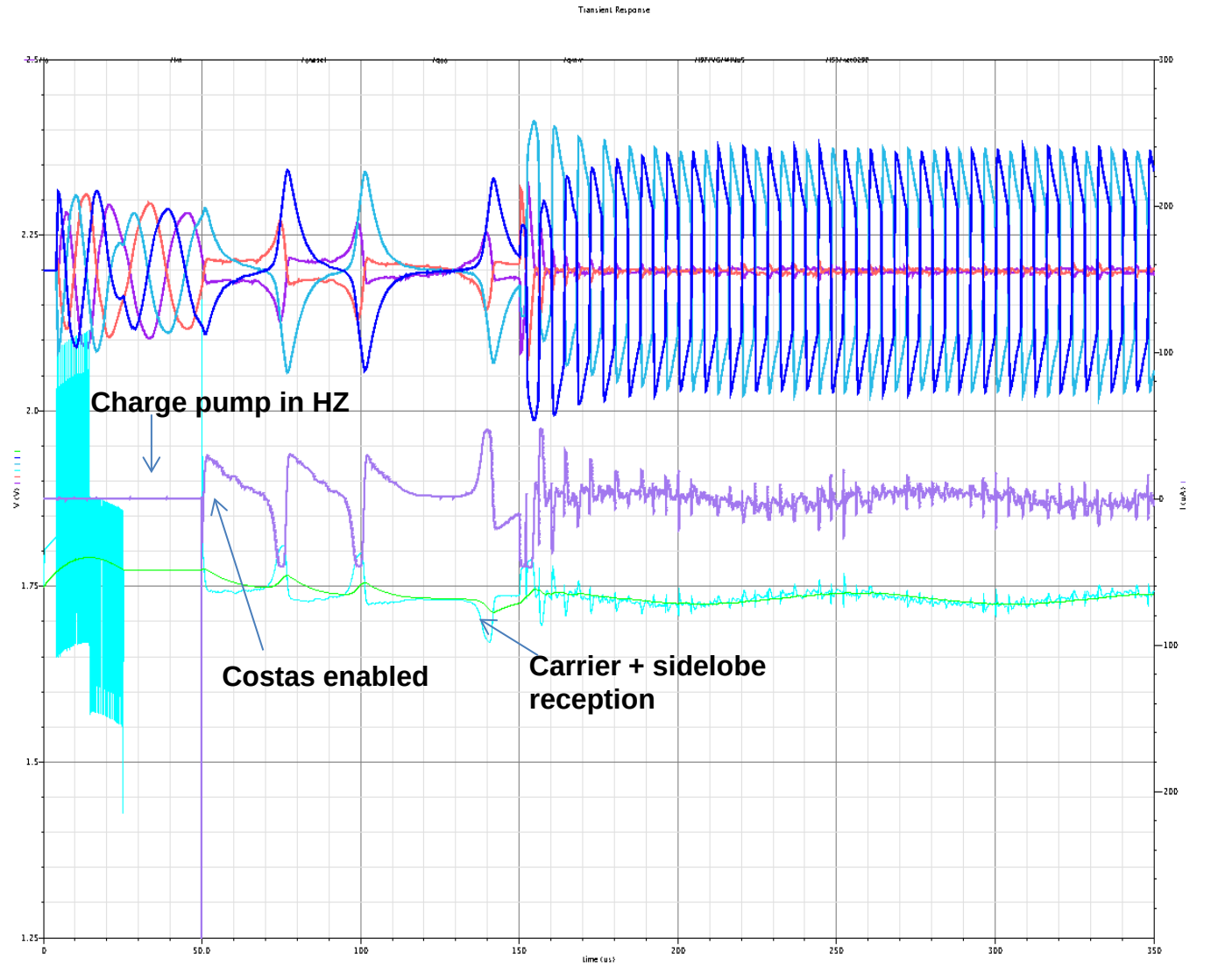
8MHz PLL frequency tracking starting from 7.2MHz



8MHz PLL phase tracking



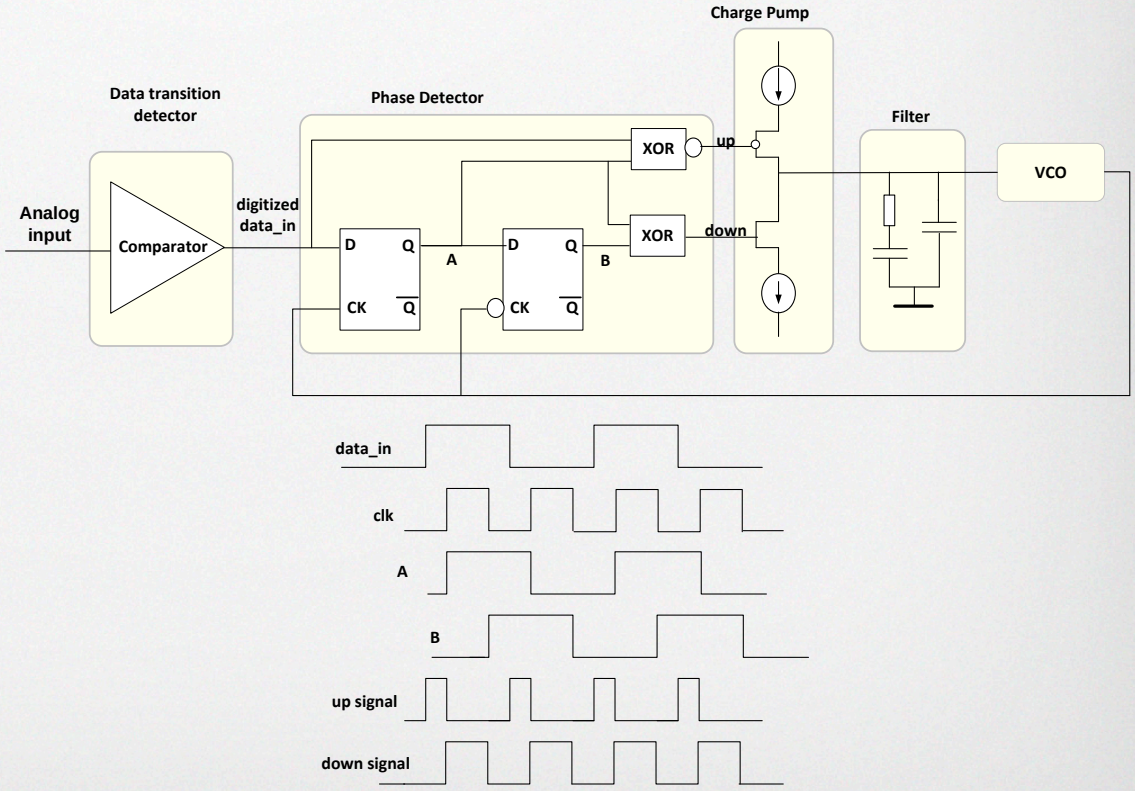
Receiver Section Description



Symbol Synchronization Unit Description

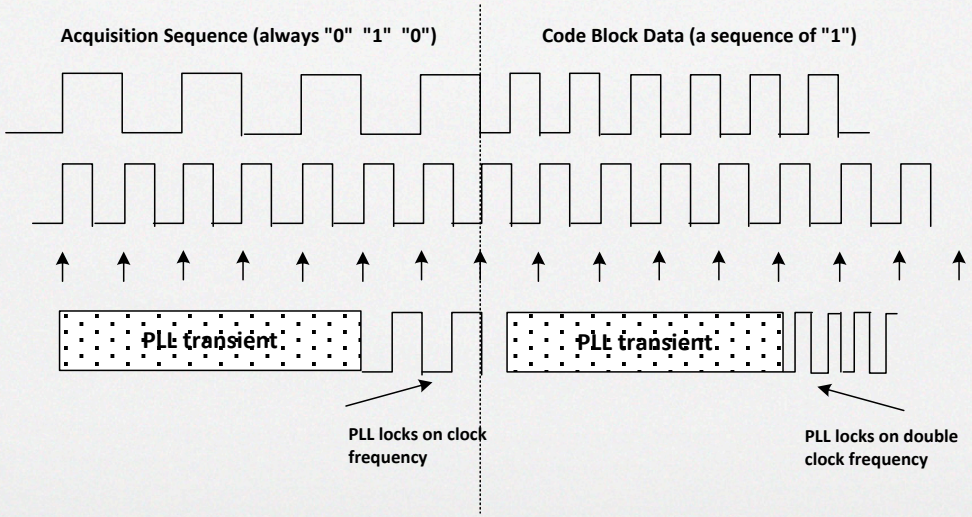
- It is composed by a Data Transition Detector and a Clock Recovery Unit
- The Data Transition Detector Unit is a simple comparator whereas the Clock Recovery Unit is a PLL which receives the 1-bit quantized data information, extracts the clock information from the demodulated symbol data stream and locks its oscillating frequency to the data transition frequency

- **The recovered clock is used for correct signal sampling inside the matched filter and decoder downstream sections**
- **Drawback: the phase detector response strongly depends on transition density, that has an heavy impact on clock phase jitter**



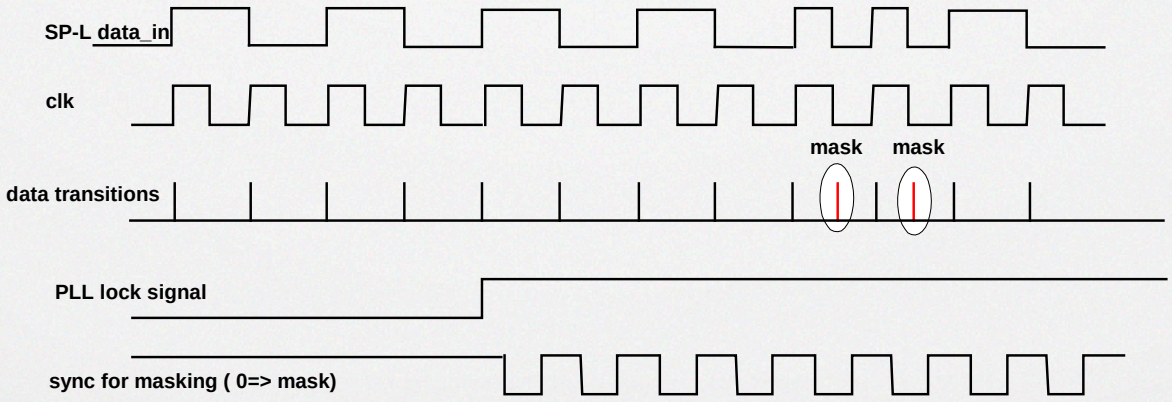
Symbol Synchronization Unit Description

- In PCM/PM/BI-PHASE signals, transitions happen or synchronously with the data clock (in strings of all “0” or “1”) or every clock rising edge (in string of alternating “0” and “1”)
- Since there is a factor 2 between the transition’s number corresponding to the 2 above different cases, the transition’s density is dis-uniform and it causes an important dispersion in the reconstructed clock phase
- Need to equalize the transition density

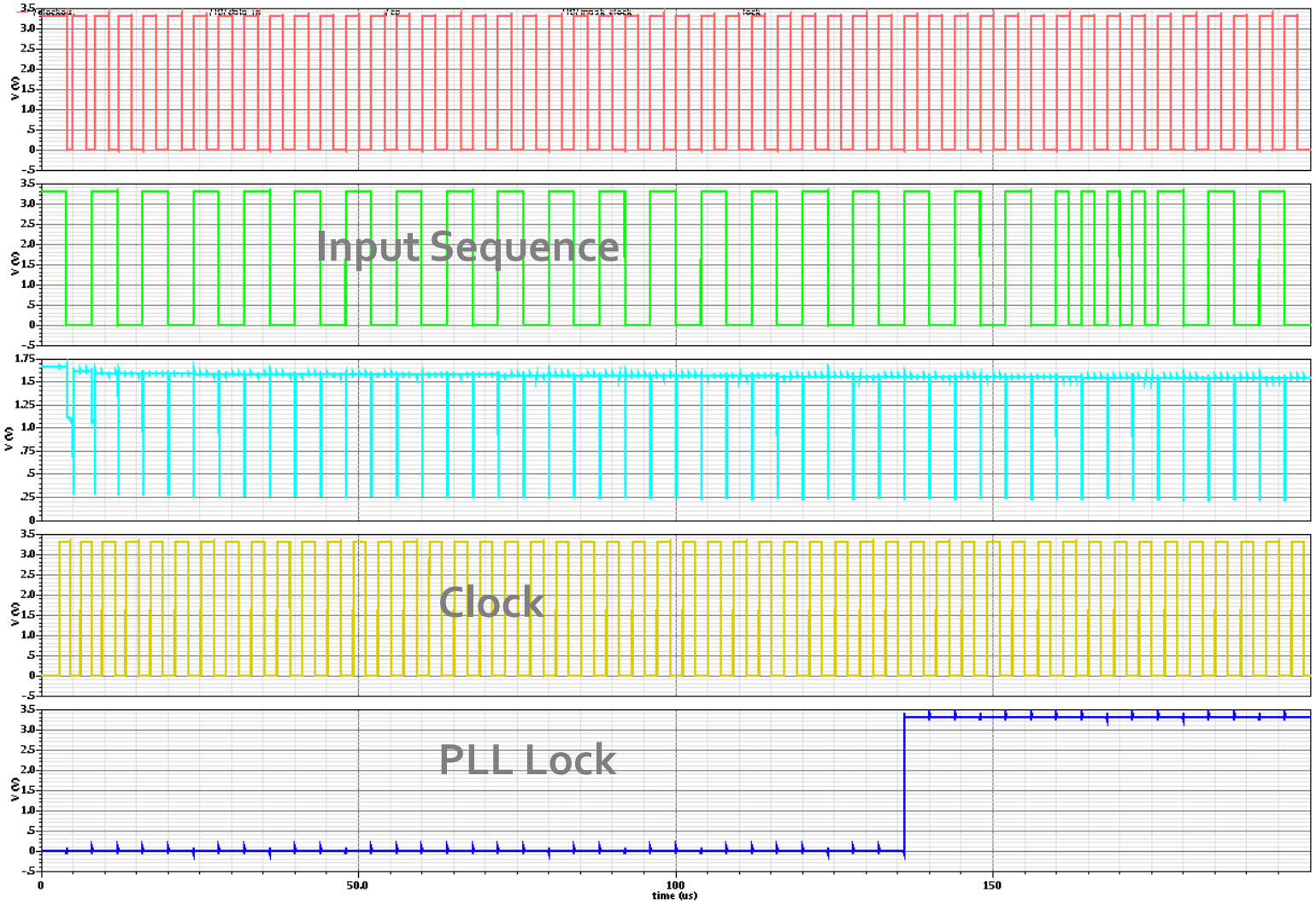


Symbol Synchronization Unit Description

- The PLL employs a standard linear phase detector and a programmable frequency divider in the feedback loop
- The high-frequency clock at the input of frequency divider (VCO output) is used as a synchronism in order to mask the undesired transitions from the input data sequence and to equalize data transition density over time
- After the PLL locks, the introduced synchronism allows to keep the transition density constant over time



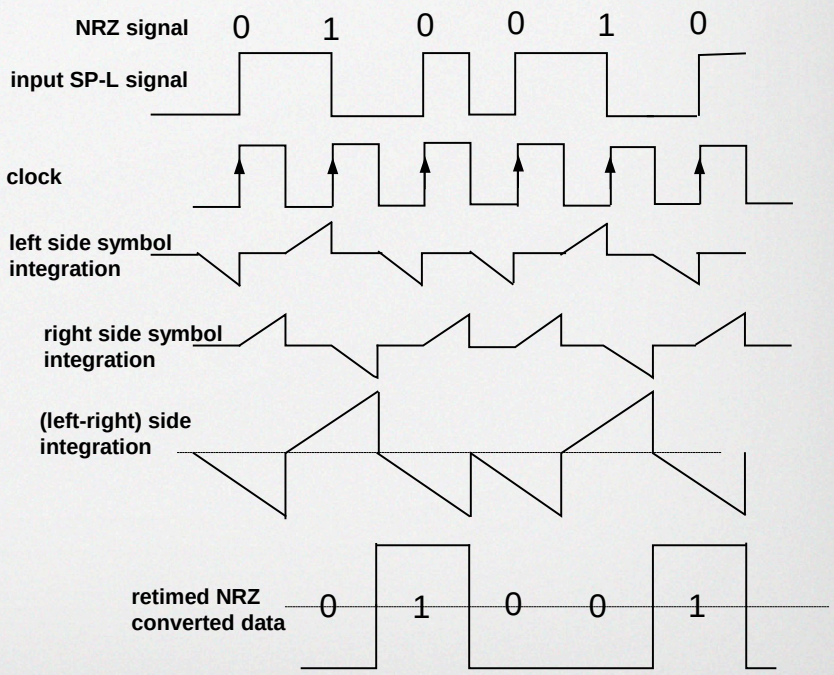
Symbol Synchronization Unit Description



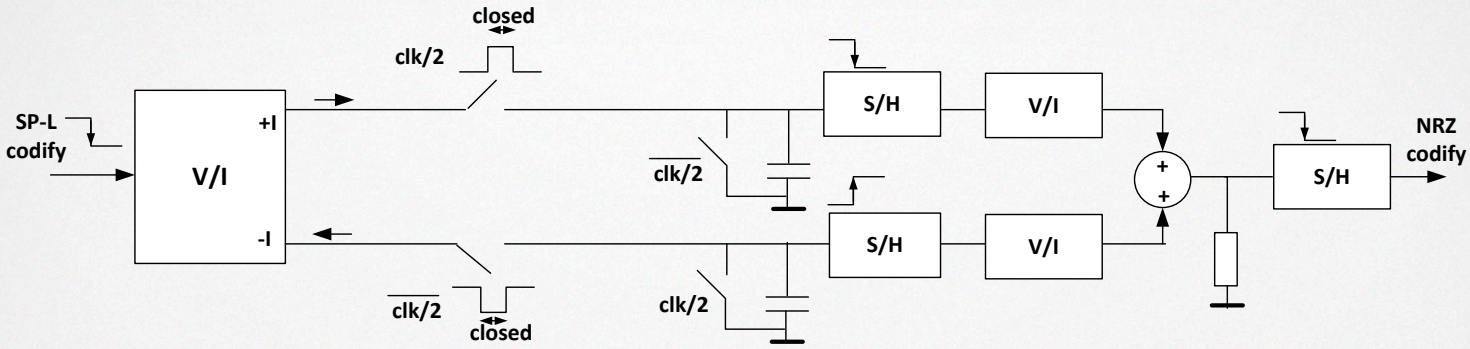
Codify Conversion Description

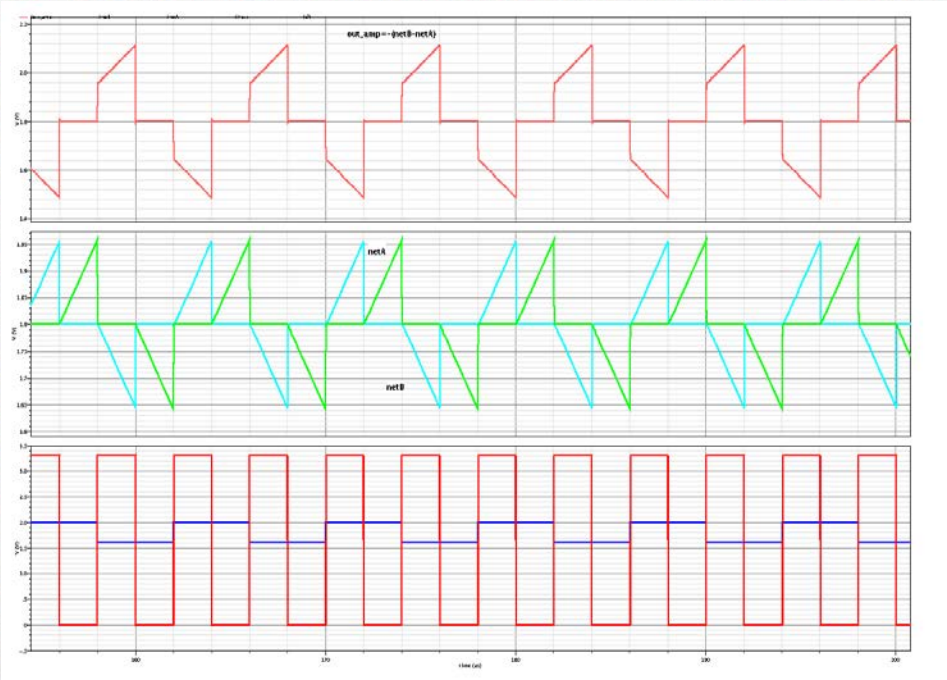
- Analogue values have to be passed to the analogue decoder, avoiding any squaring operation on analogue levels before decoding
- The analogue values stored inside the decoder memory is representative of the log-likelihood probability of corresponding bit
- The analogue values sampling could be affected by noise (for example large noise spike superimposed to the signal at sampling time)

- **The symbol level is subjected to a continuous integration operation during the symbol period**
- **The sampling of the result at symbol end will take advantage from the integration, allowing an effective noise filtering and an SNR maximization**



Codify Conversion block scheme and waveforms

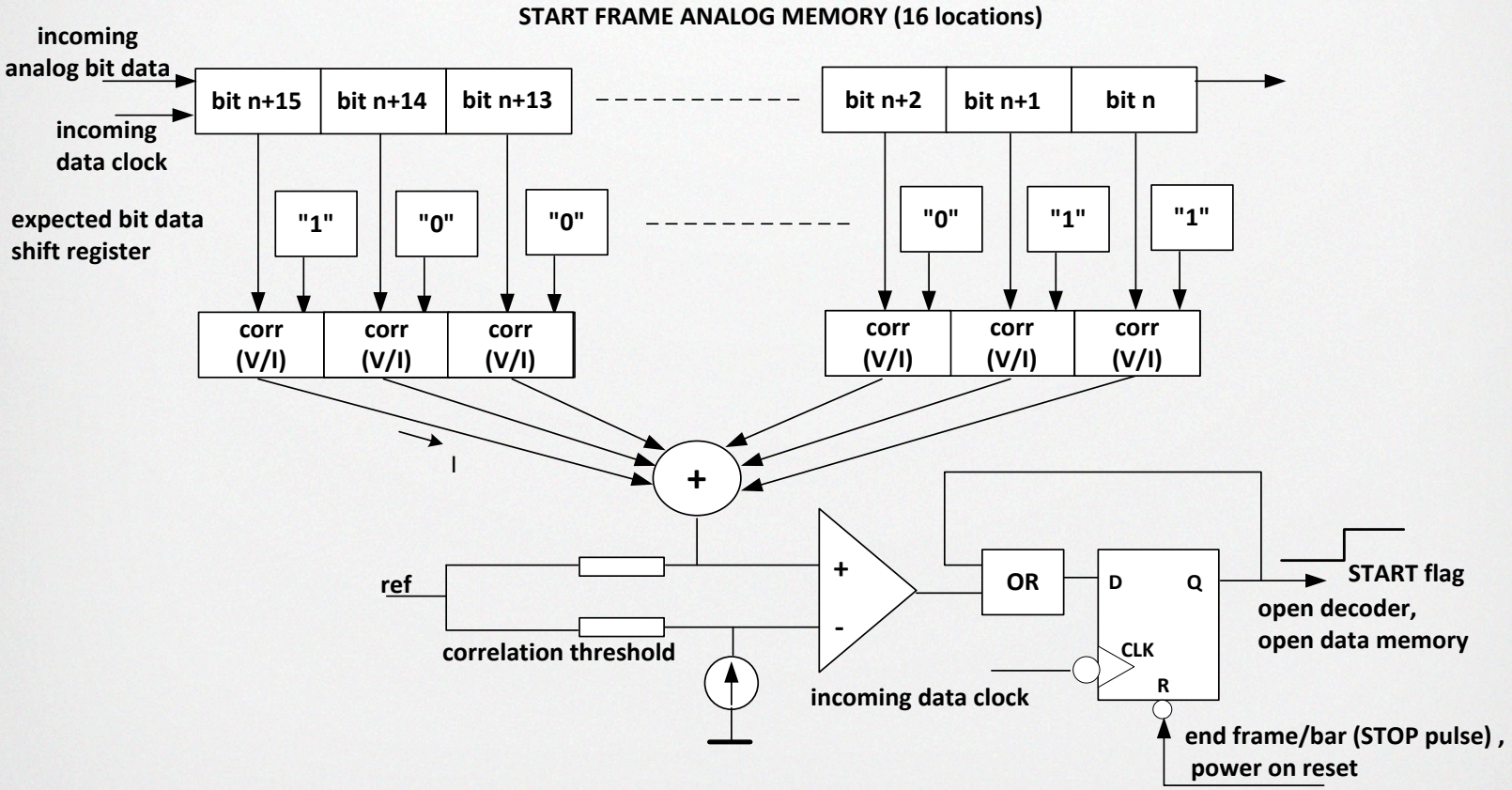




Start Frame Recognizer Description

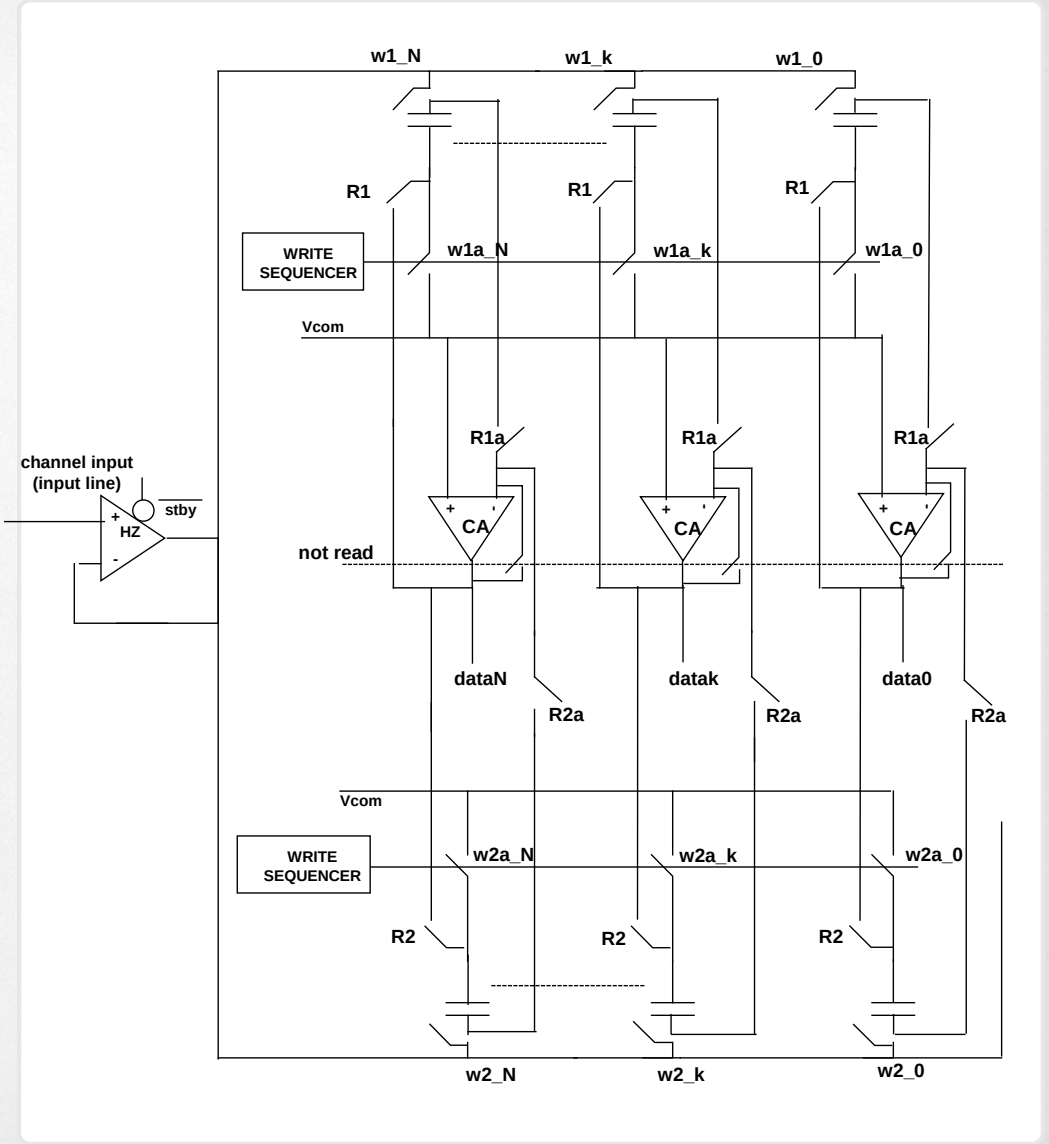
- Fixed stream data pattern to start decoding operation
- Target pattern programmable through SPI
- Sliding window approach has been adopted
- The incoming level is stored into a 16-bit analogue First-In First-Out chain
- Each value is compared with the 16 values corresponding to the pattern to be recognized
- The 16-bit correlations between received and expected bit are summed
- If the correlation result exceeds a certain (externally programmable) correlation threshold, the Start Frame pattern is recognized
- The START flag will remain asserted for decoding operation until an End Sequence will be recognized
- Multiple triggers caused by possible recognition of a Start Frame sequence during normal decoding operation has been carefully avoided

Start Frame Recognizer block diagram



Data Memory Description

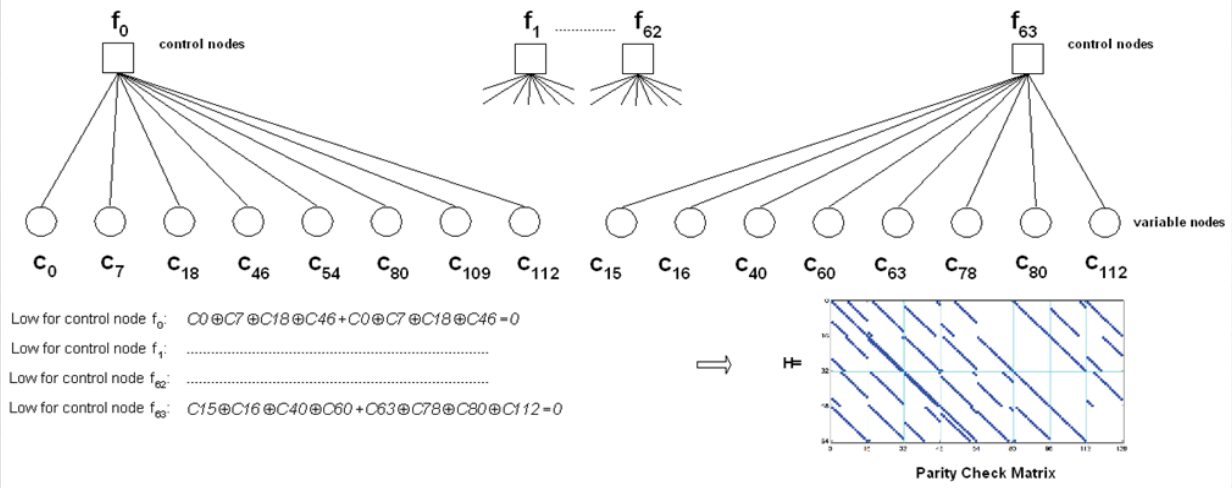
- For each clock cycle the Data Memory stores the incoming serial input analogue values in a dedicated memory cell
- The data memory feeds in parallel the values to the decoder core for elaboration
- To avoid "dead time" and guarantee continuous throughput ,a double buffer strategy has been adopted
- Double buffering allows to fill one memory with incoming analogue values while the second memory is being redirected in parallel to the decoder inputs



Decoder Core Description

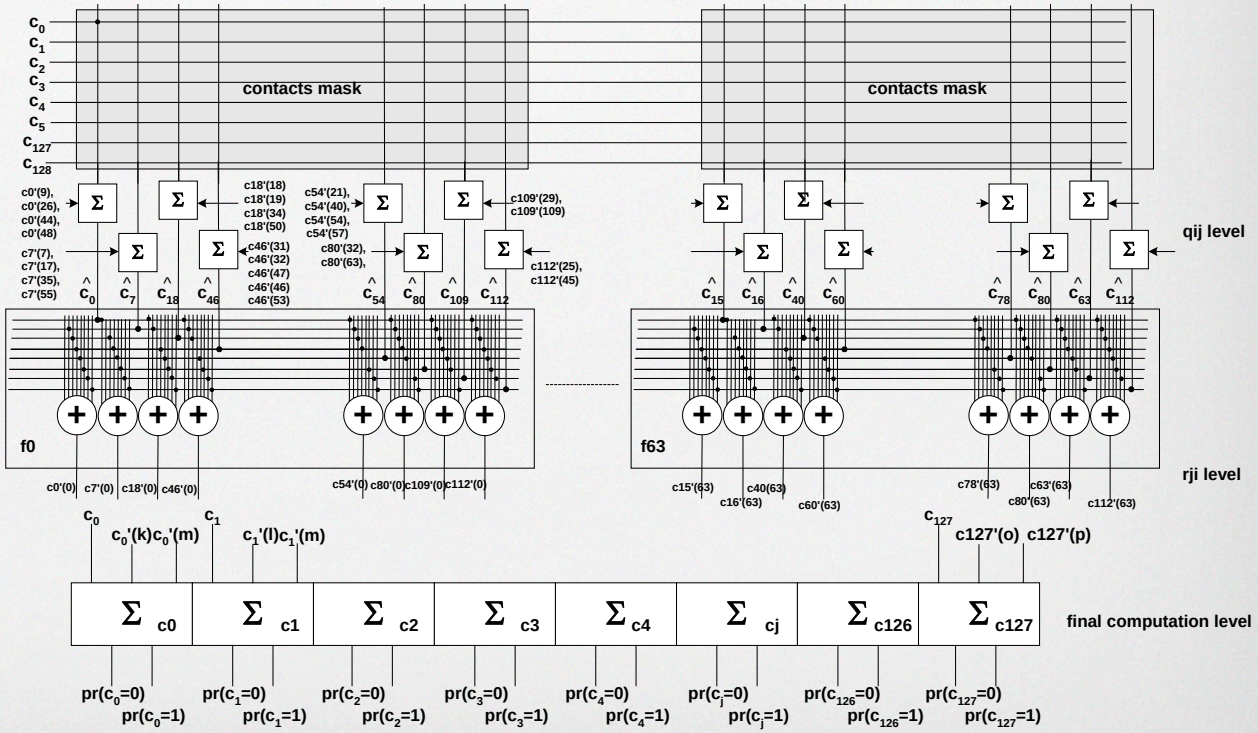
- According Low-Density Parity-Check (LDPC) short length code block for tele-command applications, the decoder implements the min-sum algorithm on the code LDPC (128, 64), which uses 64 check nodes, 8-bit-complexity each.
- The decoder is an asynchronous analogue network, built by two types of macro-cells:
  - Variable nodes
  - Check nodes
- The decoding law is established by the interconnections between the cells at routing level.
- The iteration principle of a digital implementation for solving the check law equations by progressively converging estimations has been substituted by a continuous back-connection of each estimation-process-output at the estimation-process-input that forces the network to find its stable "final" point estimations that satisfy the decoding law.
- Iterations and related overclocking with respect to input data throughput have been suppressed. → **Less power consumption**

Decoder Core Description



- Check nodes for (128, 64) code comprises 64 check nodes, each accepting systematically 8 bit from the variable node sequence

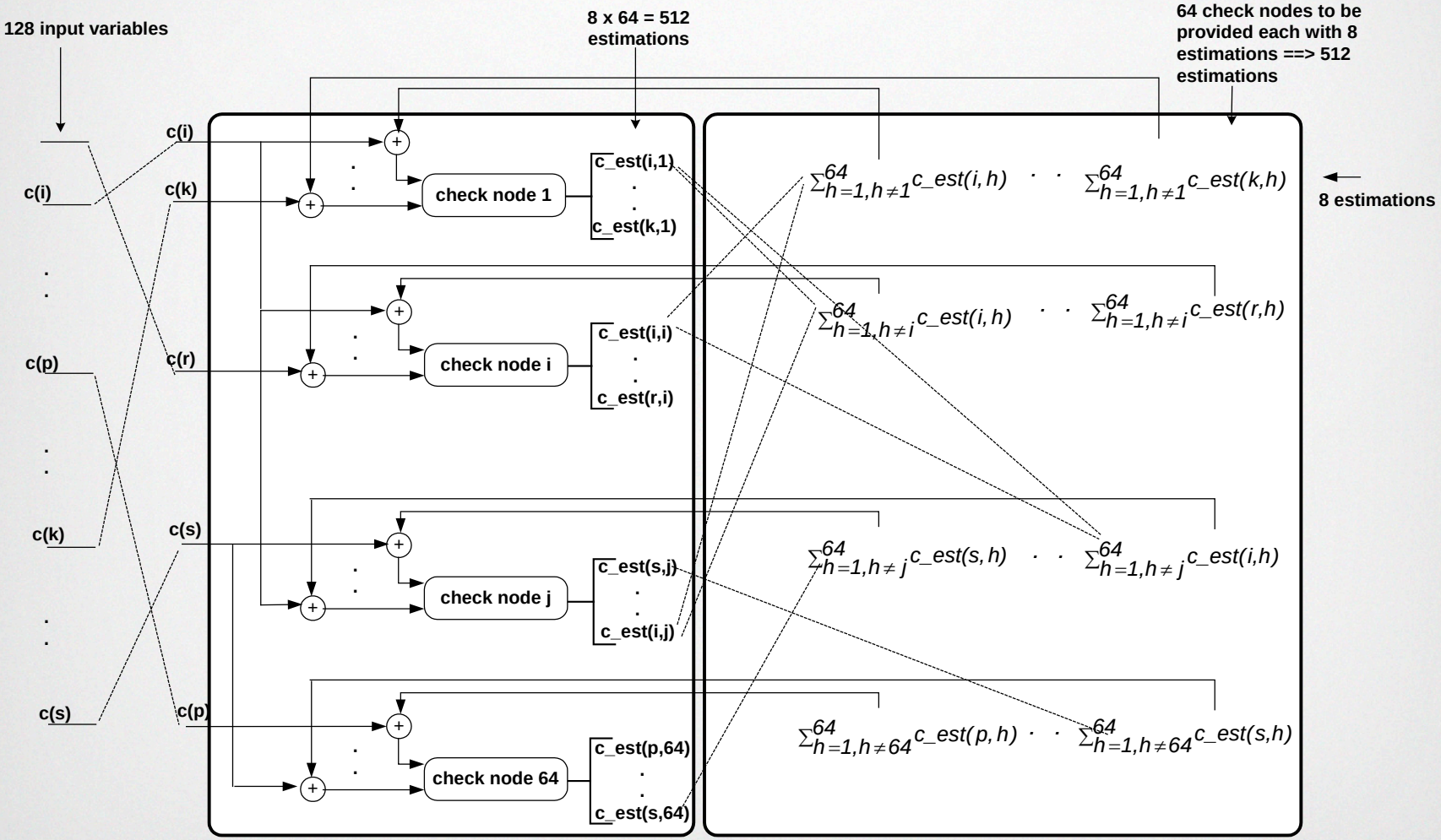
Low-level description of the min-sum algorithm applied to the parity check matrix (128, 64)



Decoder Core Description

- Each variable node "qij" evaluates its own estimation, based on input log-likelihood data and based on data provided by all check nodes which are providing an estimation for that variable node
- Each parity check node "rji" provides an estimation of each variable nodes afferent to it, by applying the parity check law (min-sum) to all other variable nodes afferent to it
- The *extrinsic information principle* has been adopted: the information produced by a node is never looped at its input
- The functionality of each *variable node* is log-likelihood probabilities summing
- The functionality of each *check node* is to select the minimum confidence (absolute value) of input log-likelihood probabilities and to assign it the expected sign

Decoder (128, 64) Block Diagram



Conclusions

A Low-Power Analogue Receiver ASIC for Space Telecommand Applications has been presented.

The mains blocks have been presented and their performances have been shown.

At the moment the following activities have been concluded:

- Architectural design
- Technology selection (XH018 by XFAB)
- Schematic design

The ASIC layout is on-going.

Availability of first samples: Q2 2015

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