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Low-Power Analogue Receiver ASIC for Space Telecommand Applications

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Nowadays, on-board telecommand receivers for space applications consume an important percentage of the overall offered power of the satellite, especially due to their always ON need of operation.
Decoders, in charge of elaborating received data and of providing error correction according to redundancy introduced by related encoding protocol are one of the fundamental components of a satellite receiver. They currently follow a digital development approach based on a large FPGA. Even though, initially, the power consumption of digital decoders was not a factor of concern, the increasing communication and data storage complexity and capacity rendered the applicability of error correction codes in a digital domain more and more expensive in terms of hardware resources and power consumption.
Therefore, in the last ten years, being analogue decoding recognized for its potential to efficiently decrease the overall power consumption of a receiver, an important growth in analogue decoding research programs is registered, although only a few VLSI integrated circuits have been developed satisfying a given communication standard. Analogue domain implementation of error correction codes, despite its lower power consumption potential with respect to its digital counterpart, seems to also provide some additional advantages: it takes benefit from the similarity between the mathematical operations required by the algorithms and the physical laws governing the circuit; it improves the total system efficiency, because the analogue decoder is much smaller than its digital counterpart and consumes about one order of magnitude less power at the same frequency; it offers high modularity design more immune to noise, by means of differential operation; it offers the capability of providing a finer estimation of the logic state of a single information unit with respect to digital implementations (no quantization); it needs a lower signal to noise ratio to properly correct a wrong input sequence of information unit.
Thus, the proposed paper will address such benefits of an on-board analogue decoder implementation by presenting, for the sake of completeness, an analogue receiver chain for telecommand applications for Category A missions (Return-to-Earth, lunar and even Lagrangian missions), being implemented on an ASIC chip. More specifically, despite the analogue decoder component, the ASIC receiver will also include other important blocks of the telecommand reception chain normally accomplished inside an FPGA device, such as IF coherent demodulation stage front end, carrier recovery, baseband clock recovery, data conversion from input SP-L signal codify to NRZ signal codify, Start Frame pattern recognition, analogue memory for input codeword storing and Low-Density Parity Check (LDPC) 128 bit analogue decoder.
In particular, LDPC Codes have been chosen as the design basis of the analogue decoder, since they showed in preliminary investigations a big potential for increased power gain when short length codes are concerned as of telecommand communication for Category A missions. Moreover, the analogue receiver will be compliant with the communication protocol described in ECSS-E-ST-50-04C “Telecommand protocols synchronization and channel coding”.
In this paper, the architecture of the ASIC is presented and overviewed. In particular, descriptive insights are provided in relation to the implementations of coherent demodulation and decoder basics. Some additional implementation details like schematic-level compact solutions which allow unifying different tasks are highlighted as well. A section is dedicated also to depict the design verification flow followed during receiver development and to highlight the main outputs of the simulations carried out during this activity that provide first high level indications on system behavior and performances.
Finally, the layout organization is briefly reported, with particular emphasis on decoder layout issues and

adopted solutions.
SITAEL S.p.A. has produced all relevant to be presented work in the frame of "RLP_AD: Receiver Low-Power Analogue Decoder"activity (ESA TRP), developed in the context of ESA ITT AO/1-6722/11/NL/GLC with the aim of investigating feasibility of analogue decoding for space applications.

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