

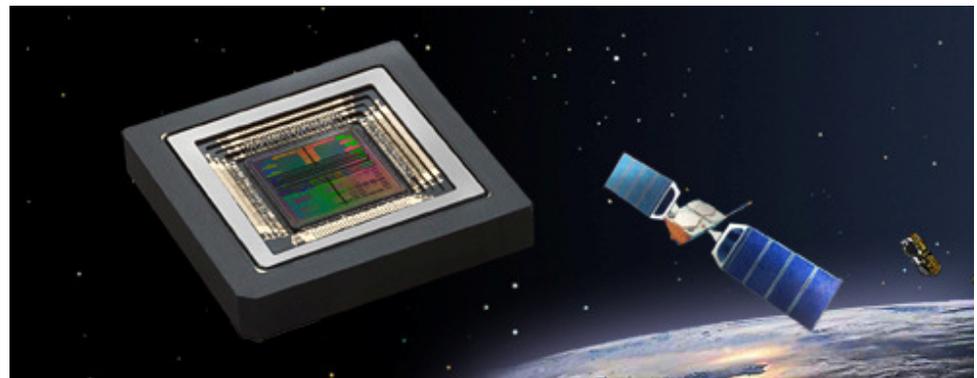


**ATMX150RHA
MIXED-SIGNAL ASIC offering for space
applications**

150nm SOI process

developed with support of CNES

AMICSA
2014, June 30th



ASIC PLATFORMS

Improving ATMEL Aerospace ASIC offering



Make durable the current digital ATC18RHA ASIC family, switching to an Atmel technology used in **qualified automotive business:**

- **with huge volumes,**
- **high reliability,**
- **long term stable process,**
- **ATMEL proprietary process**

Improve integration with versatile technology: a mixed-signal strategy

- Logic
- Analog
- 5V compatibility
- Embedded NVM option
- High voltage option



ATMX150RHA

General features

- 150 nm technology
Up to 15M equivalent NAND2 gates
- Double pad ring, 95µm Pad pitch
- Core supply 1.8V – regulators 5V / 3.3V → 1.8V available
- I/O's
 - 5, 3.3 & 2.5 V and a HV option (25-45-65V)
 - High Speed LVDS Buffers (655Mbps)
 - SERDES buffers in development (=> 3.125Gb/s)
 - PCI Buffers
- A catalog of pre-qualified Analog blocks
- SRAM/DPRAM generators and NVM blocks
- Standardized packages but also Dedicated packages

ATMX150RHA

Radiation features (1/2)

□ TID

Digital offer

- Tested up to 300 kRad(Si)
- 100krad(Si) - RHA-R level

Full offer

- Target from 60/100Krd with NVM to 300Krd tested for mixed

□ SEU

Digital offer

- SEU level equivalent to ATC18RHA

Mixed offer

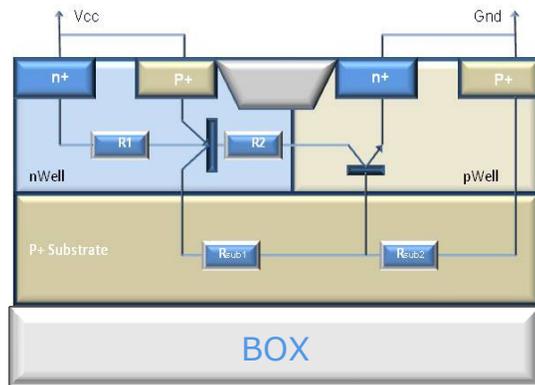
- Target LET > 30 MeV/mg/cm²

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Radiation features (2/2)

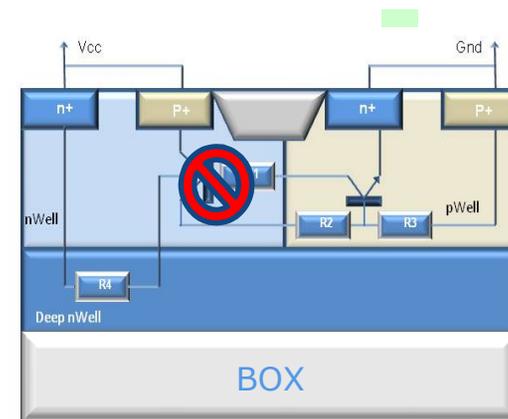
SEL: mitigation techniques

- **Deep trench**
To be used to isolate Analog blocks, Ios or sensitive area
Standard process with DT ($LET_{th} > 67 \text{ MeV.cm}^2/\text{mg}$)
- **Deep N- Well**
Noise reduction of the substrate
High reduction of the parasitic PNP base resistance
LET threshold can be improved close to 50% with the deep Nwell implant



Standard (without deep Nwell)

Deep-NWell
added beneath
CMOS inverter



With deep Nwell :
the Thyristor is not triggered

ATMX150RHA

Technology features

- Standard cell library
= ATC18RHA library (same layout and same electrical performances)
- 5V IOs with Deep Trench
- HV transistor 45V-65V with Deep Trench
- Operating temperature range
from -55°C to +125°C ambient temperature
- Life time
20 years at $T_j = 110^\circ\text{C}$

ATMX150RHA

The Full Management of your Mixed-signal flow

If customer analog blocks

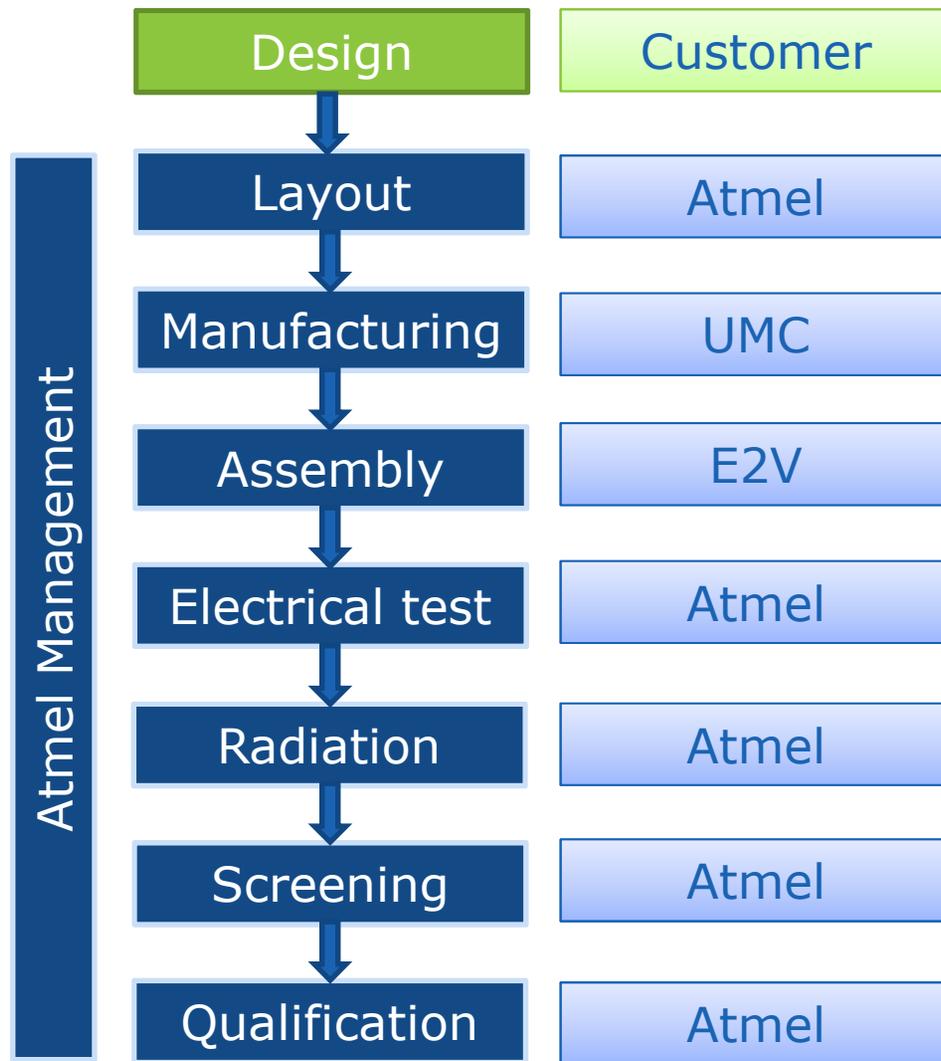
- Quarterly SMPW to embark test vehicles at low cost
- Atmel offers Probe/assembly/test services
- Qualification services (reliability, TID, SEE...)

If Atmel pre-qualified analog blocks

- Get access to a full qualified catalog
- No more test vehicles
- No more specific qualification tests

ATMX150RHA

The Full Management of your Mixed-signal flow



With Atmel global management, experience and volumes, customer get

- Pricing stability
- Time saving
- Risk mitigation

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A Design flow depending on ASIC type

Full analog

- PDK and DK provided to customer
- Atmel starting from GDSII
- With services of foundry/probe/assembly/test
- With services of qualification
- With management of package development

■ Tools

Task	CAD provider	Tool
Analog Schematic Entry	Cadence	Virtuoso Schematic Editor
Analog Simulation	Cadence	MMSIM / AMS
Analog Simulation	Synopsys	FineSim /FineSim-Pro
Extraction	Cadence	Assura
Analog Module Layout	Cadence	Virtuoso
Top Layout	Cadence	Virtuoso
Top Cheks	Mentor	Calibre

ATMX150RHA

A Design flow depending on ASIC type

Full Digital or ASIC Designed with Atmel analog blocks

- Atmel starting from synthesized netlist
- Atmel manages P&R, verifications
- Atmel manages the manufacturing flow foundry/probe/assembly/test and qualification
- Atmel manages the Package development

■ Tools

Task	CAD provider	Tool
Design Entry	-----	High Level Synthesis tool
HDL simulation	Mentor	Questasim
HDL synthesis	Synopsys	Design Compiler (topo/graphical)
DFT insertion	Synopsys	DFT Compiler
Memory BIST insertion	Mentor	Tessent MemoryBIST
P&R, Clock Tree, Crosstalk	Cadence	Encounter
Cross Talk	Cadence	Celtic
IR drop	Ansys/Apache	Redhawk
Extraction	Synopsys	Star RCXT
Formal Verification	Synopsys	Formality
Static Timing Analysis	Synopsys	Primetime Suite
ATPG	Synopsys	Tetramax
Post Layout Simulation	Mentor	Questasim
Top Checks	Mentor	Calibre

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A Design flow depending on ASIC type

Analog-on-top & Digital-on-top

- PDK and DK provided to customer
- Atmel manages the digital part (P&R, verifications, Cross-talk, IR drop, parasitics extractions...).
- Analog on top, Digital .LEF provided to customer for top-layout.
- Digital on top, Analog .LEF provided to Atmel for P&R.
- Atmel manages the manufacturing flow foundry/probe/assembly/test and qualification
- Atmel manages the Package development

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ATMEL Qualified Analog blocks

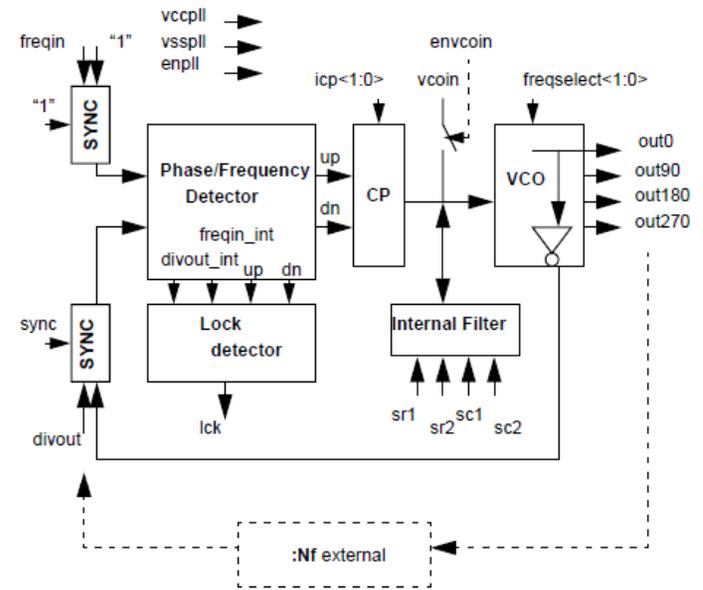
- PLL (multi-range)
- ADC (12 bits & 24 bits)
- DAC (10 bits & 24 bits)
- Multiplexer (4 / 8 channels)
- Oscillators (10 MHz, 45 MHz)
- Comparator
- BandGap reference
- Voltage regulator 1.8/5V
- DLL

ATMX150RHA



PLL - Phase-Locked Loop 40-450 MHz

- Already used in ATC18RHA
- Main features
 - Placement : Periphery
 - Supply: 1.8V
 - Programmable VCO - range from 40MHz to 450MHz
 - 4 phases VCO outputs (0,90,180,270 degrees)
 - Programmable internal Loop Filter
 - Dedicated 1.8V Power Supply (VCCPLL/VSSPLL)
 - Consumption: Dyn. 7.5mA, (max) ; Stat. 10uA (max)



Block diagram

- Dimensions (hardened)
 - X=250um, Y=552um, Area 0.14mm²
- Number of Pins
 - Total = 21

Parameter	Condition	Min	Typ	Max	Unit
Vdd		1.6	1.8	2.0	V
Temperature		-55	25	125	Deg C
F in	"freqin" input	8		120	MHz
Fout	VCO outputs (see table 2.3)	40		450	MHz
Fout/Fin				16	
Duty Cycle	VCO outputs	45		55	%
VCO Phases	90/0 or 270/180	-5		+5	Deg
Idd on	"enpll"="1"			7.5	mA
Idd off	"enpll"="0"			10	uA

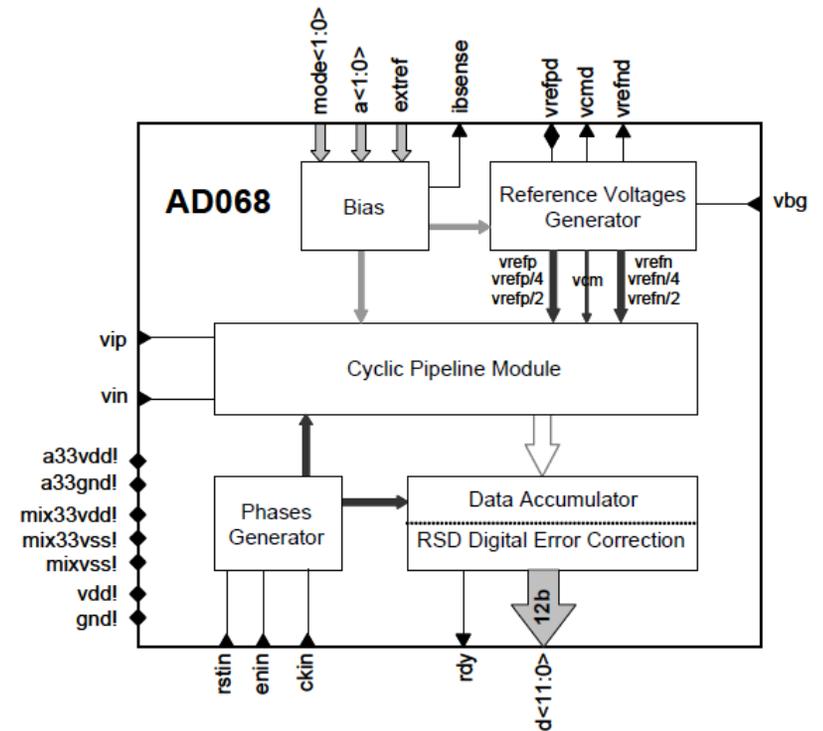
Specification over -55°C to +125°C

ATMX150RHA



ADC - 12bit Cyclic Pipeline ADC

- Features
 - Placement : Core
 - Supply: 3.3/1.8V
 - 12-bits Resolution
 - 2MHz Conversion Rate with 32MHz input clock
 - Differential Input Voltage Range 2Vpk-pk
 - Power Down Capability
 - INL +/- 1 LSB
 - DNL +/- 0.5 LSB
 - SNR 70 dB
- Dimensions
 - X=700um, Y=700um
- Number of Pins
 - Total = 35



Block diagram

ATMX150RHA

ADC 24 bits

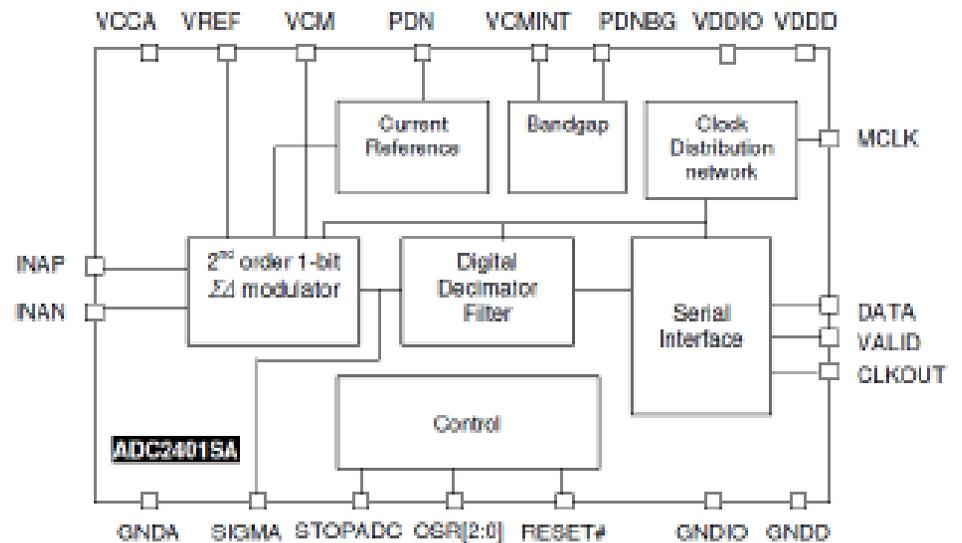


- Features

- Placement : Core
- Supply: 3.3/1.8V
- 24-bits Resolution
- Selectable oversampling ratios allow sampling rates up to 96kSa/s
- Analog bandwidth from DC to 16 KHz
- INL < 0.5 LSB
- DNL < 1 LSB
- SNR 130 dB

- Number of Pins

- Total = 29

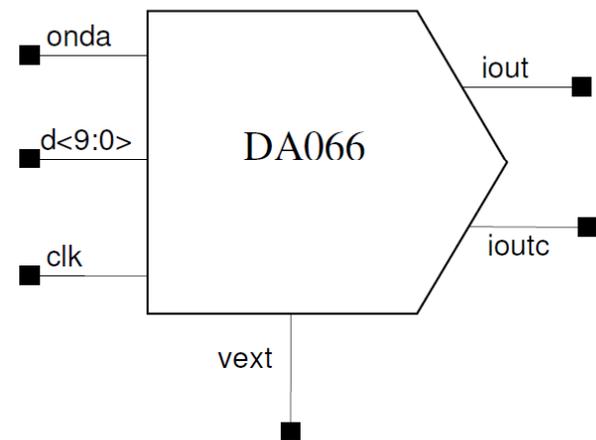


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DAC –10 bits Digital to Analog Converter

- Features
 - Placement : Core
 - Supply: 1.8/3.3V
 - Current dissipation 8mA
 - Resolution : 10-BIT, 15 MHz
 - INL 0.5 LSB
 - DNL 0.5 LSB
 - Standby to Active Delay 40 μ s
- Dimensions
 - X=800um, Y=600um



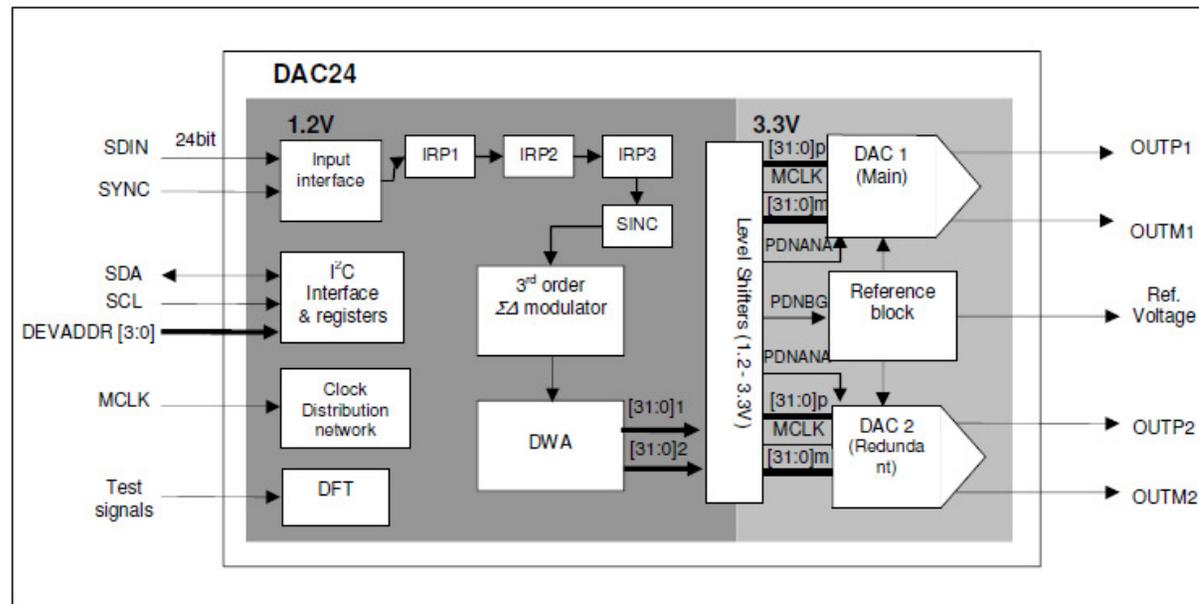
Block diagram

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DAC 24 bits



- Features
 - Placement : Core
 - Supply: 1.8/3.3V
 - Power consumption < 70 mW
 - Resolution : 24-BIT, Sampling frequency up to 2 MSa/s
 - Bandwidth DC to 330 kHz
- Number of Pins
 - Total = 36

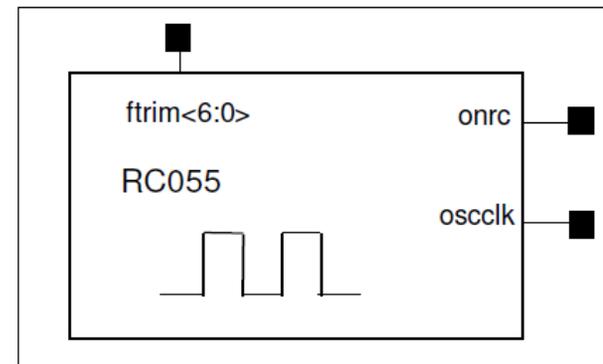


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OSCILLATOR - 10MHz trimmable RC Oscillator

- Main features
 - Placement : core
 - No external components
 - Supply: 1.8V
 - Power consumption 160 μ A @ 10MHz, 0.2 μ A standby
 - 10MHz typical frequency clock signal
 - Frequency +/-5 % by using the 7 trimming bits.
 - Stabilizing time 5 μ s
 - 1.8V Power Supply
- Dimensions
 - X=200um, Y=400um
- Number of Pins
 - Total = 11



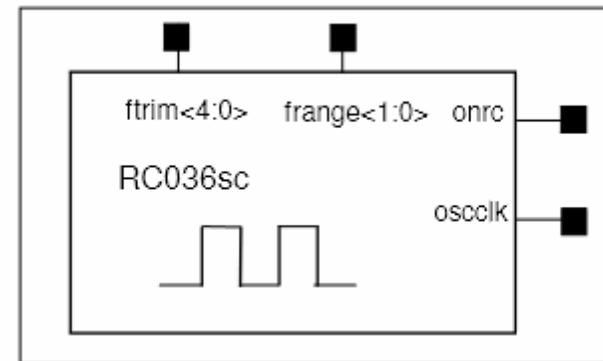
Block diagram

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OSCILLATOR – 45 MHz trimmable RC Oscillator

- Main features
 - Placement : core
 - No external components
 - Supply: 1.8V
 - Power consumption < 600 μ A @45MHz, 1 μ A standby
 - 45MHz typical frequency clock signal
 - Frequency +/-10 % by using the 5 trimming bits.
 - Stabilizing time 10 μ s
 - 1.8V Power Supply
- Dimensions
 - X=400um, Y=200um



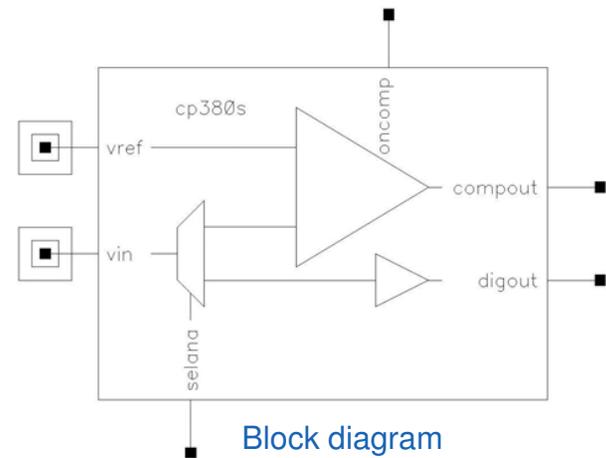
Block diagram

ATMX150RHA



Analog voltage comparator

- Features
 - Placement : Periphery
 - Supply: 3.3V
 - Vhyst 500 mV @ 3.3V
 - Consumption
 - Analog mode 30 μ A @ 1MHz
 - Digital mode 20 μ A @ 1MHz, 1pF load
 - Standby 1uA
- Dimensions
 - X=250um, Y=600um
- Number of Pins
 - Total = 10 (6 I/O + 4 Sup.)



ATMX150RHA



Low Power Bandgap voltage reference

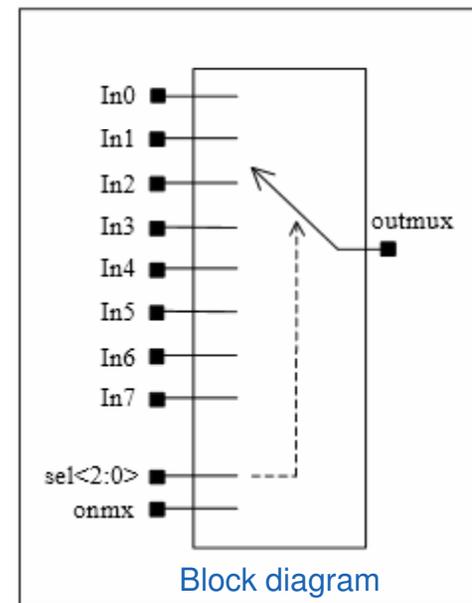
- Features
 - Placement : Periphery/Core
 - Supply: 3.3V
 - Output voltage : (1.21V/1.23V/1.26V)
 - Consumption
 - Dyn. 10 uA
 - Stat. 1uA
 - Temperature coefficient 50ppm/°C
 - PSSR
 - DC to 100Hz : 40dB
 - 10KHz to 100Khz : 5 dB
- Dimensions
 - X=300 um, Y=650um
- Number of Pins
 - Total = 3 (1 + 2 Sup.)

ATMX150RHA



Multiplexer

- Features
 - Placement : Core
 - Supply: 3.3/1.8V
 - 8 channels
 - R_{ON} 250 Ω
 - Analog bandwidth 10MHz
 - Cross talk > 60dB @1MHz
- Dimensions
 - X=700um, Y=150um

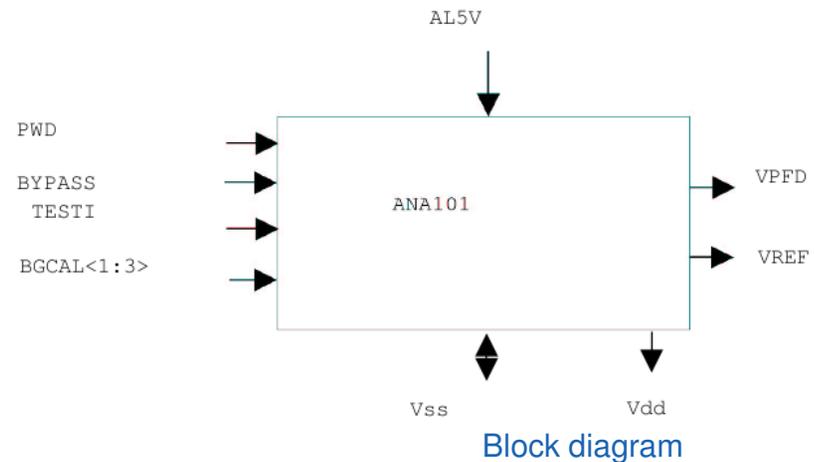


Analog IPs Library

Regulator (5V → 1.8V)

14Q3

- Features
 - Placement : Core
 - Supply: 5V down to 2.5V
 - LDO 700mV
 - Delivering 1.8V @50mA
- Dimensions
 - X=750um, Y=750um



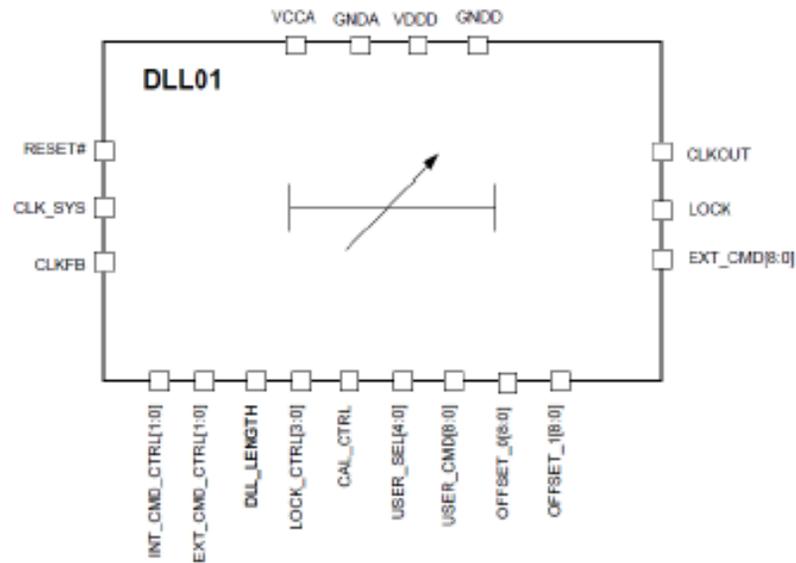
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DLL



Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_n (1)	Clock frequency				300	MHz
t_{DC} (2)	Delay Cell delay range		0.25		1.35	ns
t_{DL} (2)	Delay Line delay range	2 delay cells	0.5		2.7	ns
		5 delay cells	1.25		6.75	ns

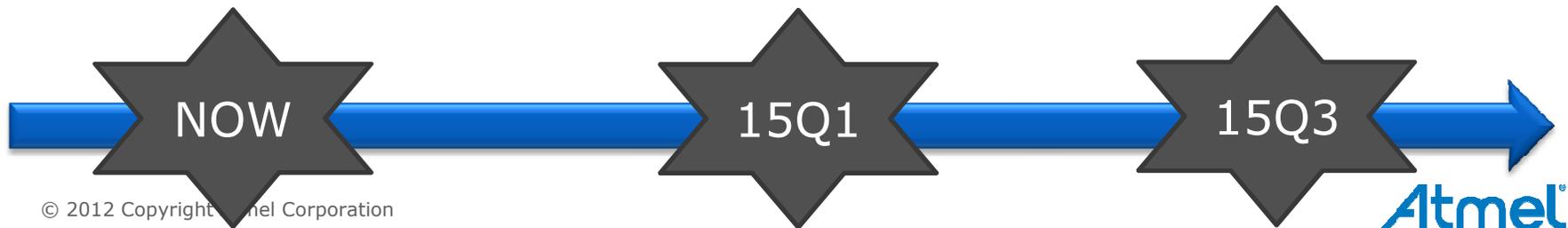
- Notes:
1. This is an indicative frequency range. Other operating frequencies can be provided upon request.
 2. The delay range values can be adapted to suit the needs of a particular application.



ATMX150RHA

KEY DATES

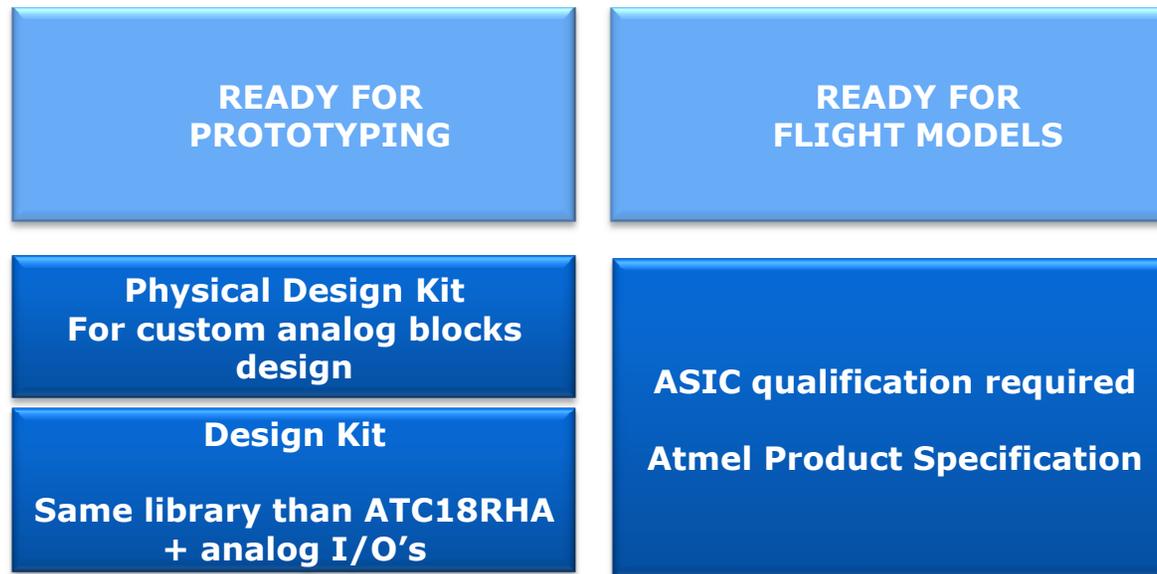
Digital ASIC



ATMX150RHA

KEY DATES

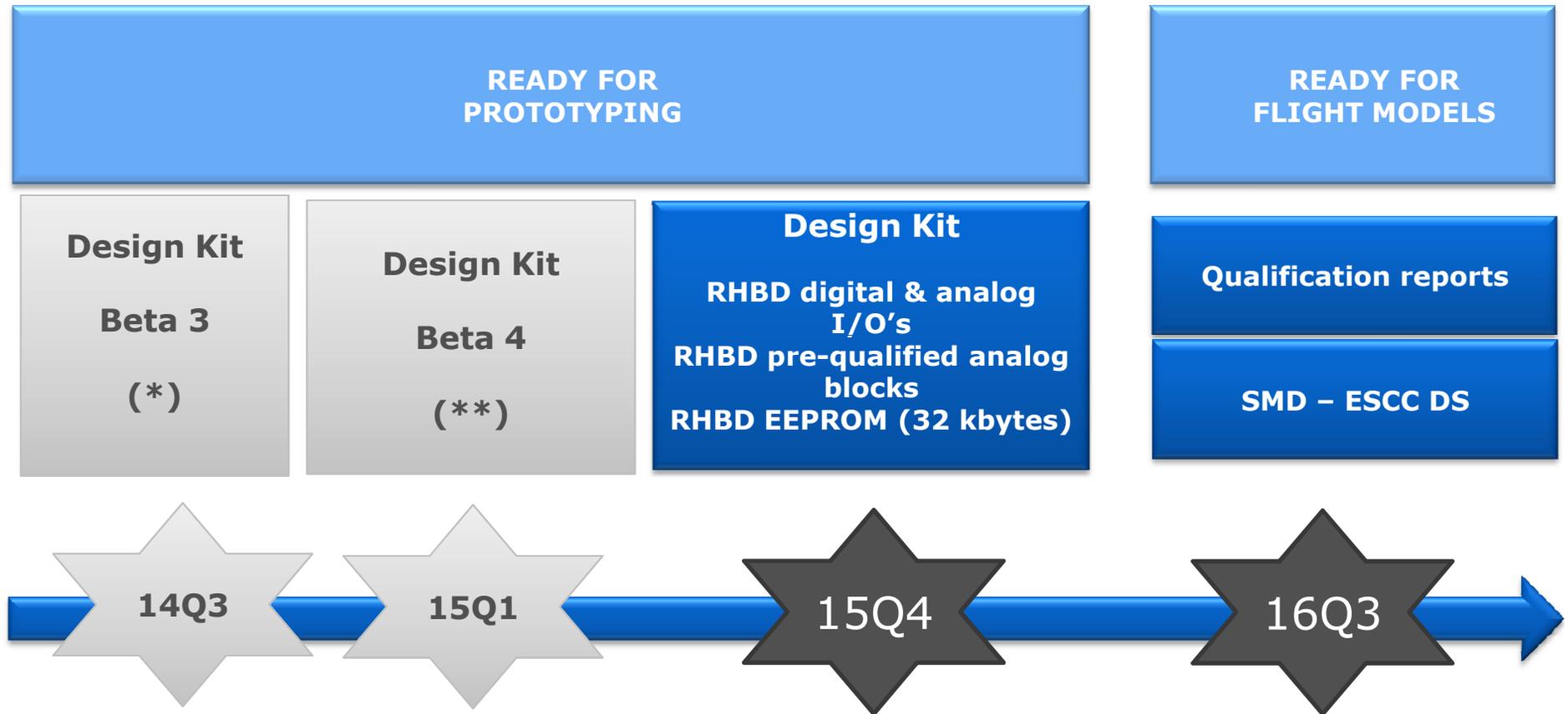
ASIC with Analog blocks designed by Customer



ATMX150RHA

KEY DATES

Intermediate & Full offering - ATMEL Mixed-signal qualified offer



Intermediate DK's

(*): equivalent to ATC18RHA one + RHB Regulator+ RHB Analog and digital HV and 5V I/O's

(**): last + RHB oscillators and bandgap + RHB eeprom block



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