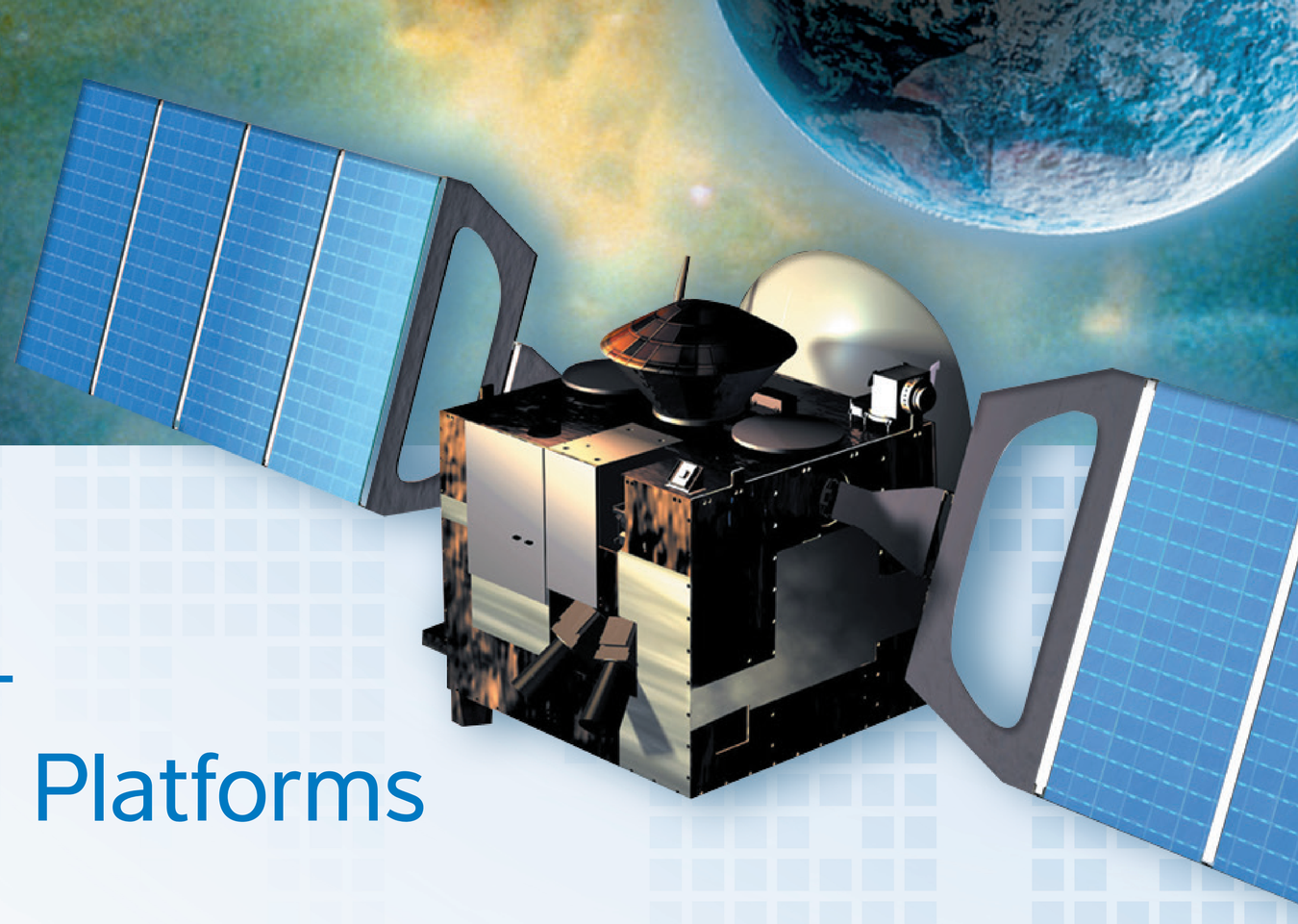
Atmel®
Enabling Unlimited Possibilities



Atmel Rad-Hard ASICs – Digital and Mixed-Signal Platforms

ATMEL ASIC Overview

	ATC18RHA	ATMX150RHA*	AT65RHA*
Process	**CMOS**	**SOI**	**CMOS**
Feature size (µm)	0.18	0.15	0.065
Library	**Digital**	**Mixed-signal**	**Digital**
Usable gates (equivalent NAND2)	7M	15M	30M
Maximum toggle frequency	7.5GHz	7.5GHz	30GHz
Gate Delay @25C (ps)	40	40	15
Signal I/Os	>400	>400	>1000
Flip-chip I/O available	N	N	Y
5V and HV (25/45/65V)option	N	Y	N
Specific I/Os	LVDS, PCI	LVDS, PCI	HSSL, LVDS, PCI
Supply Voltage	1.8/3.3/2.5V	1.8/3.3/2.5V	1.2/1.8/3.3/2.5V
Power consumption (nW/gateMHz) at 20% duty cycle	>10	>10	>0.5
Analog IPs Full-custom available	PLL	PLL, analog IP catalog	PLL
RAM compiler	Y	Y	Y
NVM	N	Y	N
Rad Hardness			
Functional TID (krads (Si))	300	300	100
Latch up (MeV/mg/cm²)	>95@125°C**	>95@125°C**	>60@125°C
Availability	Now	Now	Now
Qualification	ESCC, QML, QML-Q QML-V, QML-V RHA	2015	2015

(*): Targets (**): Maximum rate possible with test equipment

Robust Design Flow

The Atmel aerospace design flow uses a validated sequence of tools from RTL to GDSII.

Cadence	Floor planning, layout prototyping, signal integrity, package design
Synopsys	Logic/physical/test synthesis, physical design, power analysis, static timing analysis, formal verification, cell characterization tool
Mentor Graphics	Logic simulation, test synthesis, DRC/ARC/LVS verification
Magma	Library cell characterization
Atrenta	Power optimization, DFT, SDC/CDC verification at RTL level
Ansys	Power integrity

ASIC's FLIGHT HERITAGE

ATMEL Unrivaled Flight Heritage

Benefits of Atmel RHBD ASIC

- Digital & Mixed-signal ASIC
- Configurable RAM, NVM option
- Specific IO including LVDS, PCI and HSSL
- IP's portfolio
- Large portfolio of space-qualified packages
- Robust design flow
- Guaranteed radiation performance
- Multiple quality assurance levels: QML-Q, QML-V, ESCC

FPGA Retargeting to ASIC

- RTL code ⟶ QML certified ASIC
- Original functionality with low power consumption
- Pin to pin compatibility
- Optimized replacement cost :
  - ✓ Low NRE cost thanks to SMPW management
  - ✓ Lower unit cost through die size reduction
- European solution