DARE180X: A 0.18µm mixed-signal radiation-hardened library for low-power applications

G. Franciscatto[a], E. Geukens[b], G. Thys[a], S. Redant[a], Y. Geerts[b], M. Fossion[c], A. Van Esbeen[c]

[a]imec, 3001 Leuven, Belgium
[b]ICSense, 3001 Leuven, Belgium
[c]Thales Alenia Space, 6032 Charleroi, Belgium

francisc@imec.be, thys@imec.be, redant@imec.be
geukens@icsense.com, geerts@icssense.be,
marc.fossion@thalesaleniaspace.com, alain.vanesbeen@thalesaleniaspace.com

Abstract

DARE180X is a mixed-signal library solution for radiation applications implemented in the low-power 0.18 µm commercial technology from XFAB. This set of libraries comprising core standard cells, digital and analog I/O cells, analog IP and SRAM memory blocks is currently being developed using a guard-ring shielding approach to guarantee TID tolerance higher than 100 krad as well as SEL hardening for LET values higher than 60 MeV/cm^2.mg.

The DARE180X core library aims to offer good SEE hardening and low-power consumption capabilities by combining high density standard cells with SET hardened-by-drive-strength combinational cells and SEU hardened-by-design sequential cells. The DARE180X libraries also include a broad list of digital and analog I/O cells as well as several radiation-hardened analog IP blocks such as bandgap, ADC, DAC, PLL, etc.

This paper details the development of the DARE180X library and analyses its features and simulation results. A comprehensive comparison with the existing DARE180 library solution implemented in the UMC 0.18 µm technology is also presented.

I. Introduction

Harsh radiation environments constitute an essential challenge for space applications. Pervasive particles from cosmic rays induce cumulative and transient effects that can cause soft errors or even permanent damage in electronics circuits.

Mixed-signal integrated circuits implemented in deep submicron commercial technologies have already been qualified as a cost efficient solution for satellites and radiation applications [1]. Besides the low cost, these thin gate oxide technologies are inherently hardened against total ionizing dose (TID) and offer high speed, low power consumption and high yield.

Although commercial libraries are largely available they often present high single event latch-up (SEL) sensitivity when used in mixed-signal ICs. On the other hand, radiation hardened libraries are designed using special layout techniques to cope with such issues and still provide high density and low power consumption. As well, system designers can use these libraries within their traditional standard cell design flow.

The existing DARE180 library solution implemented in UMC 0.18 µm technology has already been validated in several space applications [2][3]. DARE180 was designed for general radiation systems and offers a very high TID tolerance at the cost of higher power consumption and lower gate density than commercial libraries.

The new DARE180X library platform aims to provide a solution tailored for space applications that require TID tolerance higher than 100 krad while keeping power consumption and gate density closer to the commercial libraries. Similarly to its UMC-based counterpart, DARE180X includes blocks specially designed to mitigate various single event effects (SEE).

II. Microelectronics Platform

The DARE180X libraries are part of a mixed-signal microelectronics platform that will deliver digital libraries, analog IP and memory blocks suitable for radiation hardened applications.

The 0.18 µm CMOS technology (XH018) from XFAB was selected because it provides high voltage devices and non-volatile memory blocks that may be interesting for a wide range of applications. This technology features triple-well junction isolation and transistor devices with different voltage thresholds.

A. DARE180X libraries

The DARE180X libraries are implemented using the junction-isolated low-power devices available in the XH018 technology. Junction isolation is used to improve SEL immunity in mixed-signal applications whereas high-Vt low-power devices are used to reduce leakage power consumption.

1) Digital core library

The digital core library comprises numerous combinational cells, SET-hardened cells and SEU-hardened sequential cells. All cells are designed to offer good SEL hardening in a very compact standard cell template. General library figures are listed in Table 1.

Several combinational functions and drive-strength variants are available to allow designers to synthesize and optimize their digital designs. These cells are intentionally not hardened against single event transient (SET) and should be

used in non-critical logic circuitry where low linear energy transfer (LET) thresholds are acceptable.

Table 1: DARE180X core library figures

Parameter	Value
Number of cells	86
Raw gate density	59 kGates/mm^2
Averaged cell area	127 µm^2
Horizontal pitch	0.62 µm
Vertical pitch	0.62 µm
Cell height	11 tracks

Critical logic paths such as set/reset and clock trees can be implemented using special SET-hardened cells available in the library. These cells are designed to withstand LET values of at least 60 MeV.cm^2/mg.

All the flip-flops and latches available in the core library were designed to be immune to single event upsets (SEU) due to LET values higher than 60 MeV.cm^2/mg. Since set/reset and clock trees are supposed to be implemented with the SET-hardened cells the SEU-hardened sequential cells were not designed to be immune to SET at their inputs. For this reason, flip-flops featuring SET filters at their data inputs are also included in the library.

The core library also includes several place & route cells such as filler cells, decap cells, tie cells and antenna cells.

2) I/O library

The I/O library includes several digital and analog pad-limited I/O cells. As in the core library, all I/O cells are hardened against SEL effects. Digital input I/O cells are also hardened against SET to prevent events from propagating to the core logic.

An extensive list of tri-state output, bidirectional and 5V-tolerant bidirectional I/O cells with different driving capabilities is available. The library includes fast slew-rate and slew-rate controlled versions of these I/O cells.

Power and ground I/O cells as well as breaker cells are available for the definition of multiple I/O power domains. Besides regular 3.3V analog I/O cells the library also includes high-voltage supply and I/O cells to be used with high-voltage blocks.

3) SRAM blocks

A set of five dual-port SRAM memory blocks is available in the DARE180X platform. The basic memory cell uses straight transistors and it is optimized for area and power consumption.

The memory blocks are designed to be insensitive to multi-bit upsets (MBU). This is achieved by arranging the bits of a same word far enough from each other. In this case every two bits of a same word are separated by 16 bits which corresponds to an interleaving distance higher than 60 µm. This way an error detection and correction circuit (EDAC) can be used to mitigate soft errors due to single-bit upsets (SBU) [4].

4) Analog blocks

Table 2 lists the most important analog blocks currently in design phase.

Table 2: Available analog cells

IP block	Supply	Provider	Status
PLL, 120MHz	1.8V	ICsense	Design
Bandgap	3.3V	ICsense	Design
Bandgap Low Power	3.3V	ICsense	Design
PoR / UVLO	3.3V	ICsense	Design
Relaxation Oscillator 100kHz (R/C)	1.8V	ICsense	Design
12b DAC 3.75MS/s	3.3V	ICsense	Design
13b ADC 1MS/s	1.8V / 3.3V	ICsense	Design
Linear Regulator 1.8V, 36mA	3.3V	ICsense	Design
HV Linear Regulator, Vout 3.3V	[4 – 16.5] V	ICsense	Design

a) Bandgap reference voltage

The bandgap reference can be considered the most critical analog block because it serves as a reference to all other analog cells. A large spike or bump on this reference voltage will translate into a decrease of analog performance and can be potentially harmful to the ASIC (e.g. over-voltage in case of an LDO).

The bandgap reference is made insensitive to SET by using techniques like for example the insertion of filtering caps and high current levels.

Table 3: Bandgap reference specifications

Parameter	Value
Reference voltage	1V ± 2%
Temp. drift	± 0.6%
Temp. drift (dig. comp.)	± 0.1%
SET hardening	60 MeV/mg/cm^2

b) 13b ADC 1 MS/s

A 13b cyclic ADC has been developed together with a passive sample-and-hold structure and a 16-channel multiplexer. The ADC is capable of measuring both single-ended and differential signals.

The ADC is designed to recover fast from SET events in order to have only a single sample affected. This affected sample can be easily filtered by digital post-processing.

Table 4: 13b ADC specifications

Parameter	Value
Resolution	13b
Data rate	1 MS/s
Input range SE	[0 – 2.5] V
Input range DIFF	±1.25V$_{diff,ptp}$
DNL	1 LSB
INL SE *(better in DIFF)*	6 LSB

c) 12b DAC

A monotonic 12b PMOS current DAC has been developed. Several techniques are used to minimize artifacts from non-uniform ageing and TID drifts.

Table 5: 12b DAC specifications

Parameter	Value
Resolution	12b
Output range	[0 – 4] mA
DNL	< 1 LSB
INL	3 LSB

d) 120 MHz PLL

A 120 MHz PLL is realized completely on-chip. SET-hardening techniques are used to create a very stable clock-period and duty-cycle.

Table 6: PLL specifications

Parameter	Value
Fout	[100 – 120] MHz
Fin	100 kHz
LPF cut-off	7 kHz
PLL order	3rd
Fout max. deviation during SET (peak)	±10%
SET hardening	60 MeV/mg/cm^2

e) 100 kHz Relaxation Oscillator

The implemented relaxation oscillator uses external components (R and C). A special topology is chosen for low jitter and temperature drift. In fact the temperature drift is dominated by the external components. The oscillator is hardened against SET.

Table 7: 100 KHz oscillator specifications

Parameter	Value
Fout	100 kHz
Temp. drift	< 5000 ppm
Temp. drift with ideal external components	< 1000 ppm

B. Radiation hardening by design methodology

1) TID & SEL hardening

All cells in the DARE180X libraries are designed to tolerate TID rates above 100 krad and to be immune to SEL under LET values higher than 60 Mev.cm^2/mg.

Thin gate oxide technologies already offer good TID hardening for most space applications. Radiation tests have shown that basic straight transistors in the XH018 technology can tolerate TID rates of at least 100 krad. Higher TID hardening could eventually be achieved by using enclosed layout transistors (ELT) [5] at the cost of higher power consumption and lower area density.

Fully enclosing P+ guard-rings together with junction-isolated devices (triple-well) are used to guarantee very good SEL hardening [6]. These guard-rings also help to reduce the impact of TID as they isolate possible leakage paths between N+ diffusions at different potentials. An example of this layout approach is shown in Figure 1.

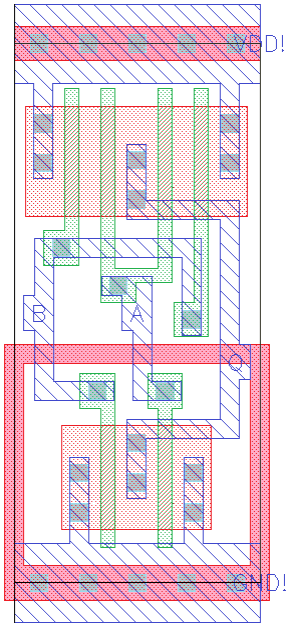

Figure 1: Guard-ring protections in core standard cell

2) SET-hardened cells

SET hardened cells were included in the library to be used in very critical paths such as set/reset and clock trees. These cells were hardened using a hardening-by-drive-strength approach where transistors are dimensioned to provide higher gate capacitance and driveability. Larger gate capacitances induce a higher critical charge on the driver's net whereas higher driveability increases the restoring strength on the driven net affected by a charge strike [7].

The hardening of a cell can be verified using charge injection simulations where critical charges corresponding to the desired LET threshold are individually injected on every cell node while the cell outputs are monitored for an event propagation. Every cell under test is connected to a load cell that matches the weakest flip-flop input stage in the library so that cell under test is considered hardened when no events propagate across this load cell. The charge injection in these simulations is modelled by a double-exponential current source [8].

3) SEU-hardened sequential cells

Flip-flops and latches are implemented using a Dual Interlocked Cell (DICE) architecture [9]. These SEU-hardened cells are based on redundant storage nodes and present very good SEU hardening.

C. DARE180XL core library

As already mentioned the XH018 technology features different flavours of transistors. The DARE180X libraries are implemented using the high-Vt low-power devices which provide low driveability and consequently higher SET

sensitivity. For this reason, a core library using low-Vt transistors (DARE180XL) was also implemented.

The DARE180XL core library contains the exact same cell set as the DARE180X one and the equivalent cells in both libraries have the exact same footprint, i.e. same size and pin placement. Moreover, the cells from both libraries are fully compatible and can be abutted in the same layout. These features provide designers with different alternatives for power and timing optimization.

Low-Vt devices offer twice the driveability of high-Vt transistors at the cost of higher leakage power consumption.

III. DARE180X AND DARE180 COMPARISON

The UMC DARE180 library implementation focused on general radiation applications that could require very high TID tolerance, above 1 Mrad. This was possible with the use of ELT devices combined with guard-rings. The downside of using this kind of transistor in a standard cell library is that the smallest feasible device has an equivalent W/L five times bigger than the minimum W/L allowed in this technology.

Besides the area penalty, this limitation leads to high cell input capacitances in the whole library which cause synthesis tools to use cells with high drive-strengths. As well, multiple stage cells cannot be effectively optimized for optimal delay and low internal power consumption as the input stages are limited by this minimum W/L value. All these elements contribute to increase power consumption in end-user system designs.

On top of that, the ELT's outer diffusion is relatively larger than diffusion areas of a straight transistor with equivalent W/L which can lead to higher cross-section values in some cases. Even if LET threshold is the most important parameter to define the SET sensitivity of a cell, it is also important to consider the cross-section value which depends on the node's diffusion sensitive area and denotes the probability of a strike on the node.

1) Cell-level comparison

Table 8 compares a NAND gate between the UMC library and the two versions of the XFAB library. Similar comparison is presented for the NOR gate in Table 9. Timing performance is compared in terms of fanout-of-4 (FO4) which gives a valid comparison figure that takes into account the different input capacitances in each library.

Table 8: NAND2 cell comparison (typical corner)

	DARE180	**DARE180X**	**DARE180XL**
Cell name	NAND2	NA2JIX4	NA2JILVTX4
Relative drive strength	X1	X4	X4
LET threshold	35 MeV.cm^2/mg	17.5 MeV.cm^2/mg	35 MeV.cm^2/mg
Saturation cross-section	3.45 cm^2	0.86 cm^2	1.31 cm^2
Cell area	39.5 µm^2	29.6 µm^2	29.6 µm^2
Rise FO4 delay	90 ps	140 ps	81 ps
Fall FO4 delay	66 ps	95 ps	61 ps
Average input capacitance	15 fF	15 fF	14 fF
Average leakage	52.68 pW	3.76 pW	2306.98 pW

Table 9: NOR2 cell comparison (typical corner)

	DARE180	**DARE180X**	**DARE180XL**
Cell name	NOR2	NO2JIX4	NO2JILVTX4
Relative drive strength	X1	X4	X4
LET threshold	12.5 MeV.cm^2/mg	12.5 MeV.cm^2/mg	25 MeV.cm^2/mg
Saturation cross-section	0.58 cm^2	1.43 cm^2	1.43 cm^2
Cell area	28.2 µm^2	29.6 µm^2	29.6 µm^2
Rise FO4 delay	159 ps	152 ps	119 ps
Fall FO4 delay	58 ps	88 ps	60 ps
Average input capacitance	12 fF	16 fF	15 fF
Average leakage	42.85 pW	4.2 pW	2441.5 pW

In general, the X1 cells from the DARE180 library compare to the X4 cells from the new DARE180X and DARE180XL libraries in many aspects. The new libraries also offer weaker drive-strength variants that can be used for power and timing optimizations in system designs but a trade-off between power consumption and SET hardening exists. For instance, the low driveability of high-Vt low-power devices in the DARE180X core library result in worse timing performance and higher SET sensitivity.

Sequential cells in DARE180X libraries were implemented using DICE cells whereas the ones in DARE180 library were based on the Heavy Ion Tolerant (HIT) architecture [10]. Although both designs offer very good SEU-hardening, DICE cells present some advantages such as lower power consumption and easier implementation. The flip-flops and latches implemented in DARE180X are also slightly smaller than the ones available in DARE180.

2) System-level comparison

Cell-level comparisons may be useful to evaluate aspects intrinsic to the technologies such as speed and leakage but timing performance and power consumption in entire designs

depend also on library characteristics such as the number of functions and drive-strength variants available.

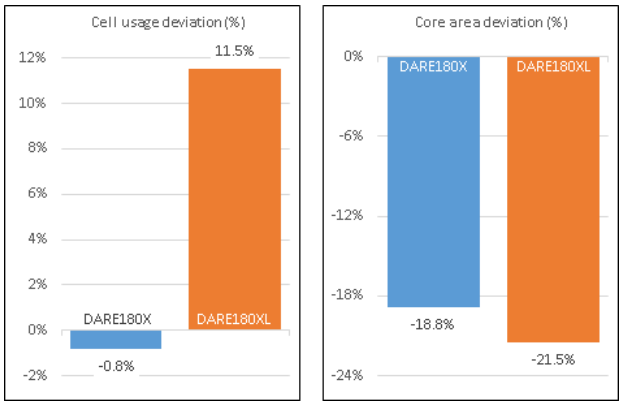

Figure 2: Synthesized design area variation from DARE180

A complex design was synthesized using the different core libraries in order to assess their efficiency regarding area and power consumption. Figure 2 and Figure 3 respectively show the synthesis and power analysis results achieved with the DARE180X libraries in terms of deviations from the results obtained with the DARE180 library.

As expected, both versions of the DARE180X core library are able to deliver better area and power consumption results. Even if leakage penalty with DARE180XL is high the total power consumption in absolute values is reduced.

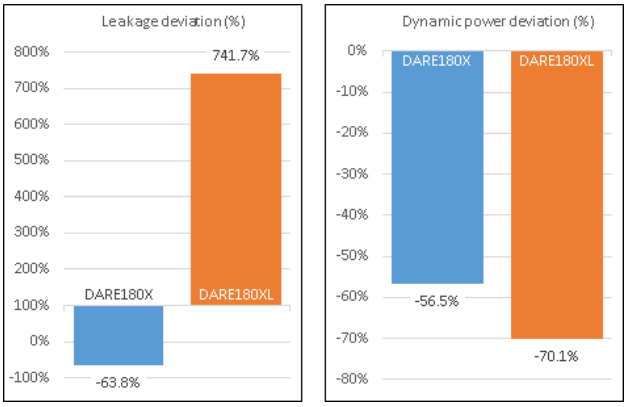

Figure 3: System-level power variation from DARE180

An overall comparison between DARE180 and DARE180X library sets is summarized in Table 10.

Table 10: Comparison summary of DARE180X vs. DARE180

	DARE180	**DARE180X**
Technology	UMC 0.18 µm	XFAB 0.18 µm (XH018)
Process	Mixed-mode/RF	Junction-isolated (triple-well)
Metal support	6 layers	6 layers
Core supply range	1.8 V ± 10%	1.8 V ± 10%
I/O supply range	3.3 V ± 10%	3.3 V ± 10%
Temperature range	-55 ºC to 125 ºC	-55 ºC to 125 ºC
TID tolerance	> 1 Mrad	> 100 krad
Transistor type	ELT	straight
Sequential cell hardening	HIT	DICE
Raw gate density	25 kGates/mm^2	59 kGates/mm^2
# core cells	130	86
# I/O cells	83	48
SRAM	Single-port/dual-port SRAM compiler	5 dual-port blocks available

IV. Further Work

Currently the SRAM and the analog blocks as well as the I/O library are being finalized. The complete DARE180X library platform is scheduled to be available by the end of June. A test chip is scheduled to be made after the official library release.

The test chip shall include test structures to assess the radiation hardening and verify the functionality of the different libraries elements.

V. Summary

This paper introduced the development of a new radiation-hardened library platform for mixed-signal space applications. A set of libraries including numerous core cells, I/O pads, SRAM blocks and analog circuits is being developed and will offer a complete solution for low-power applications that require TID tolerance above 100 krad.

These libraries are implemented in the 0.18 µm technology from XFAB which includes triple-well junction isolation and high-voltage devices. Different design and layout techniques are used to mitigate SEE and improve TID immunity.

The core library is available in both low-power and low-Vt versions which are compatible with each other. Cell-level and synthesis comparisons show that DARE180X core libraries are able to give better results in area and power consumption than the DARE180 core library.

The I/O library, SRAM and analog blocks are currently being designed and scheduled to be released in June. Further investigation on performance and radiation hardening of these new libraries is planned to be done through a test chip.

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