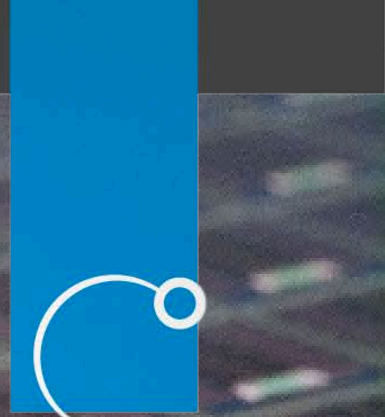
Aerospace



Assessment of Mixed Signal Technology

M. Bacci , F. Bigongiari, C. Boatella Polo, R. Dittrich, M. Inversi, R. Jansen

5th Analogue and Mixed-Signal Integrated Circuits for Space Applications Workshop

Geneve (CH), June 29th – July 1st, 2014

Outline

- Introduction
- Description of Surveys
- Analysis of Surveys
- Conclusions

Introduction

- "**Assessment and characterization of Mixed Signal Technology**" is an activity in the frame of European Component Initiative program.
- Purpose: collect information about mixed signal ASIC processes with particular focus on their capability for space applications.
- Information sources:
  - Previous AMICSA workshops
  - Round table at AMICSA 2012
  - ESCCON Conference
  - Surveys through space community
- The collected data on the **user needs** have been compared against the **processes capabilities available** in Europe for mixed signal ASIC manufacturing.
- Moreover to avoid duplicating the efforts, information about similar on-going activities and on existing analogue, digital and mixed signal libraries or ASICs for space applications already manufactured or designed have been collected.
- At the end of this process review **one technology has been chosen** for a further reliability and radiation characterization.

CONFIDENTIAL
SITAEL Property

Three different Surveys have been carried out:

I. Comparative assessment and verification about the *availability of several existing European mixed signal technologies*.

II. Collection of inputs covering *the needs* for mixed-signal ASICs from the space community and the Agency's planned missions.

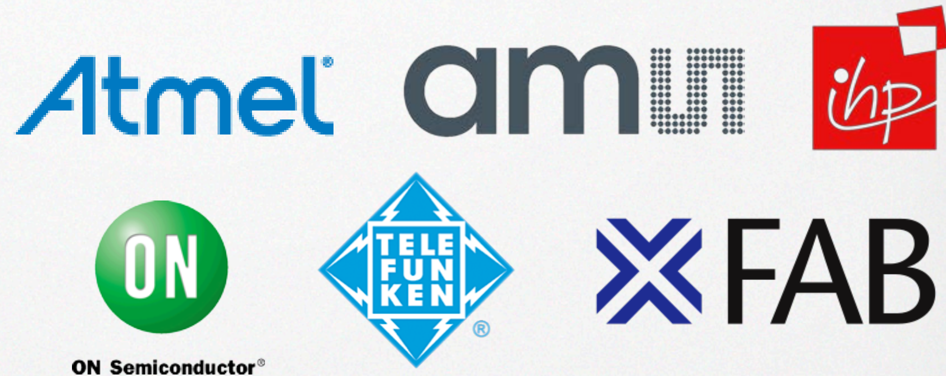
III. Collection of information about the *existing rad hard libraries and design kits* in terms of primitive devices, SEEs, TID and reliability performances.

CONFIDENTIAL
SITAEL Property

First Survey: **Mixed Signal Technologies Availability**

Twelve (12) European and Non-European manufacturers have been contacted obtaining reply from six (6) of them:

- ATMEL
- Austria Micro Systems
- IHP Microelectronics
- ON Semiconductor
- Telefunken Semiconductor
- XFAB



In total, **information from 18 technology processes have been collected and analyzed.**

Focus of the surveys

- *General items related to foundry availability*
- *Environment*
- *Quality*
- *Digital performances*
- *Analogue performances*

First Survey: **Mixed Signal Technologies Availability**

General items related to foundry availability

- Licensing and conditions for use
- Foundry expected lifetime
- Foundry loading and product range
- Foundry process options
- Manufacturing turnaround time
- Manufacturing options (Full mask, MPW, MLM; Runs per year; longer availability)
- Cost of the supported tool chain (external and custom)
- Cost of the digital and analogue design-kit (front- and back-end)
- Supported batch manufacturing
- Supported Digital and Analogue development flows and constraints
- Foundry macro libraries cost
- Third party macro libraries access, conditions, cost and license
- Design kit for usage within space user community and the right for modifications
- Eventual technical support and maintenance of space-DK/libraries for European Space community

CONFIDENTIAL
SITAEL Property

First Survey: **Mixed Signal Technologies Availability**

Environment

- Temperature range (operational and storage)
- Voltage range
- Radiation tolerance (TID, SEE, SEL, SEU, SET, SEGR, ...)
- ESD and EMC levels supported

First Survey: **Mixed Signal Technologies Availability**

Quality

- Intrinsic reliability data/performance
- Wafer thickness
- Process lifetime
- Mean time to failure (FIT)
- Manufacturing yield
- Manufacturing quality systems
- Inspection of the manufacturing quality system and PID
- Cost associated with quality inspection
- Reporting and inspection of the process control monitors
- Process stability reporting the manufacturing process changes
- Failure analysis support
- Manufactured high-reliability and space qualified flows/components

First Survey: **Mixed Signal Technologies Availability**

Digital Performances

- Gate density
- Power consumption
- Clock frequency
- Supply voltage range
- Number of metal layers
- Leakage
- Cell library (combinational and sequential; commercial and rad hardened variants)
- Foundry and/or Third party digital macro libraries (commercial or rad-hardened; development/qualification state)
- IO Pads (Voltage levels, ESD, EMC, ...)
- Manufacturing spread (power consumption, clock frequency, leakage)
- Accuracy of the models
- Development tool flow supported
- Sign-off tool chain

First Survey: **Mixed Signal Technologies Availability**

Analogue Performances

- Analogue IO Pads (Voltage levels; ESD; EMC; …)
- Number of poly layers
- Accuracy of the models
- Availability of: MOS transistors, Bipolar transistors Diodes and Passive
- Development tool flow supported
- Sign-off tool chain
- Foundry or Third-Party analogue macro libraries (commercial or radiation-hardened; development/qualification state) and their support

CONFIDENTIAL
SITAEL Property

First Survey: **Mixed Signal Technologies Availability**

List of the analyzed processes

Foundry	Process	Process Features
Austria Micro System	C35B4C3	0.35um
	H35B4D3	High Voltage 0.35um
	C18	0.18um
	H18	High Voltage 0.18um
ATMEL	AT77.9K	High Voltage 0.15um
	AT58K85	High Voltage 0.15um
IHP Microelectronics	SGB25RH	0.25um
	SG13RH	0.13um
ON-Semi	C3/D3	0.35um
	C05	0.5um
	I3T25	High Voltage 0.35um
	I3T50	High Voltage 0.35um
	I3T80	High Voltage 0.35um
Telefunken	TFSMART1-HV	High Voltage 0.8um
	TFSMART2	High Voltage 0.35um
XFAB	XH035	High Voltage 0.35um
	XH018	High Voltage 0.18um
	XT018	High Voltage 0.18um

Second Survey: **Agency and Space Community Needs**

Twenty-eight (28) entities have been contacted,
collecting eighteen (18) compiled surveys

- 2 Large Scale Integrators
- 5 Large Industries
- 7 Small and Medium-sized Enterprises
- 4 Research Institutions

CONFIDENTIAL
SITAEL Property

Third Survey: **Investigation about Comparable Activities**

Aim:

- To avoid efforts duplication
- To harmonize and coordinate with future or on-going existing activities

Questions about Rad Hard Libraries have been grouped in four (4) sections:

- *Primitive Devices*
- *Single Event Effects Tests*
- *Total Dose Ionization Tests*
- *Reliability Tests*

CONFIDENTIAL
SITAEL Property

Third Survey: **Investigation about Comparable Activities**

Primitive Devices

- Funding mechanism used for rad hard libraries development (self-funding, public funding, private funding, etc.)
- Availability free of charge of the results (libraries, design-kits,…) for scientific research
- List of scientific papers published about the performances of Rad Hard libraries
- Technology process used to develop the Rad Hard libraries
- List of primitive devices with increased radiation tolerance
- Description of the modified introduced on primitive devices
- List of the violated design rules, accepted by the foundry
- List of modification on the fabrication process (i.e. masks sequence)
- List of the modified primitive devices model
- List of analog simulators supported by these new models (i.e. spectre, hspice, …)
- List of digital libraries developed based on this library
- Type of characterization performed on digital libraries

Third Survey: **Investigation about Comparable Activities**

Single Event Effects Tests

- List of test(s) to evaluate the Single Event Effects
- Description of manufactured test vehicle/custom ASIC for SEE characterization/modeling
- Parts or devices included in the test vehicle
- Parts or devices not included in the test vehicle
- Description of source used (i.e. heavy ions or protons …)
- Description of heavy ions/protons cocktail and LET used
- List of primitive devices tested against SEE
- Measured performances in terms of SEL, SEU, SET, SEB, SEGR, SEFI
- Test procedure used (i.e. ECSS 25100)
- Description of the SEE test by laser
- Description of simulation model to take into account the SEE effects
- List of analog simulators supported by these new models (i.e. spectre, hspice, …)

CONFIDENTIAL
SITAEL Property

Third Survey: **Investigation about Comparable Activities**

Total Dose Ionization Tests

- List of test to evaluate the performances in terms of Total Ionization Dose (TID)
- Description of manufactured test vehicle/custom ASIC for TID characterization/modeling
- Parts or devices included in the test vehicle
- Parts or devices not included in the test vehicle
- Description of the source used and dose rate
- Final TID accumulated
- Test procedure used (i.e. ECSS 22900)
- Description of simulation model to take into account the TID effects
- List of analog simulators supported by these new models (i.e. spectre, hspice, ...)

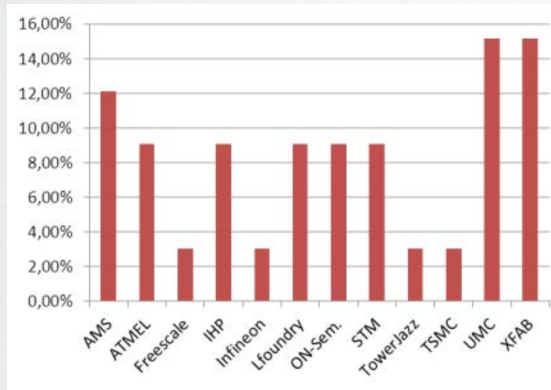
Third Survey: **Investigation about Comparable Activities**

Reliability Tests

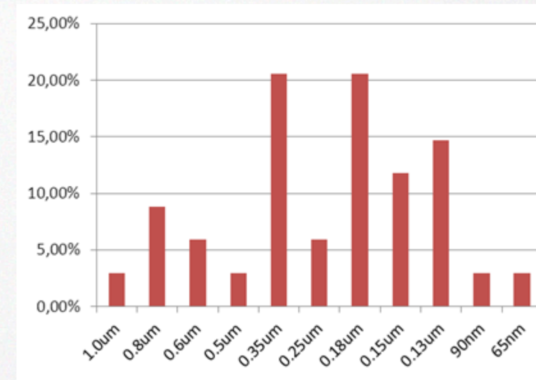
- Description of reliability test performed on the library
- Description of manufactured test vehicle/custom ASIC for Reliability characterization/modeling
- Parts or devices included in the test vehicle
- Parts or devices not included in the test vehicle
- Test procedure used
- Description of the obtained results

CONFIDENTIAL
SITAEL Property

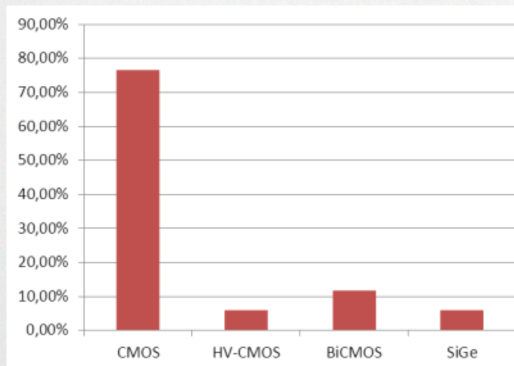
- Preferred mixed-signal ASIC



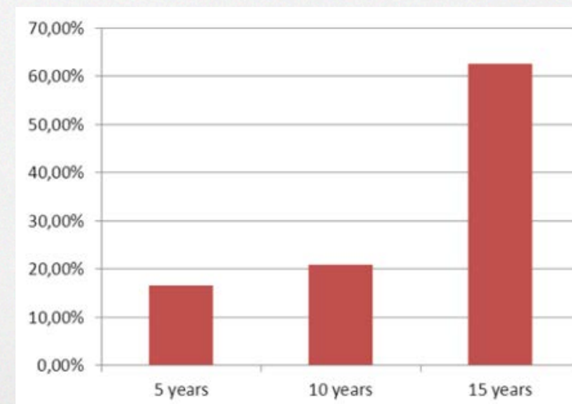
- Preferred mixed-signal ASIC process gate length



- Preferred mixed-signal ASIC technologies options

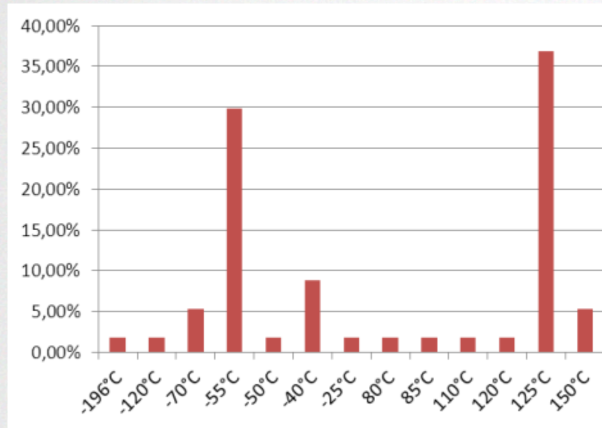


- Expected technology's lifetime

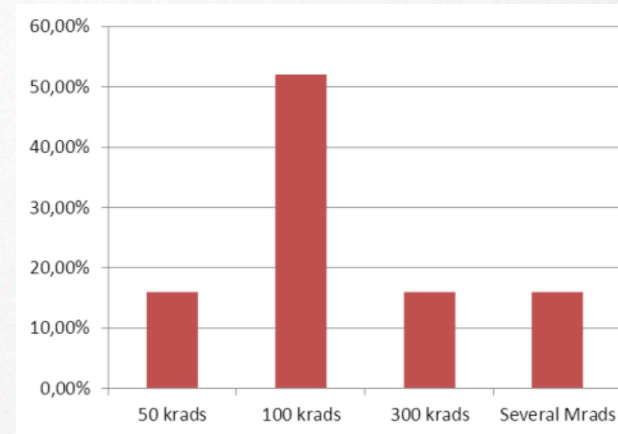


CONFIDENTIAL
SITAEL Property

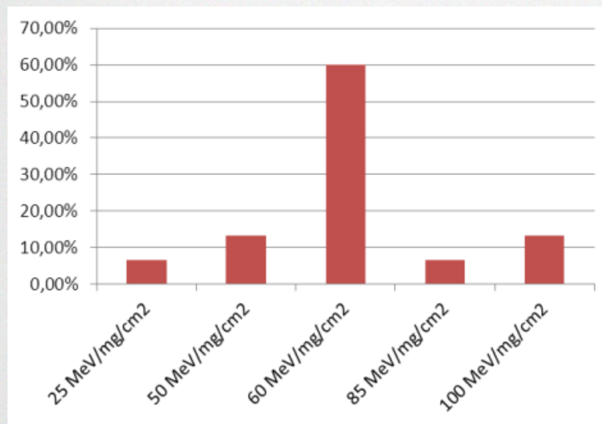
- Expected operational temperature range



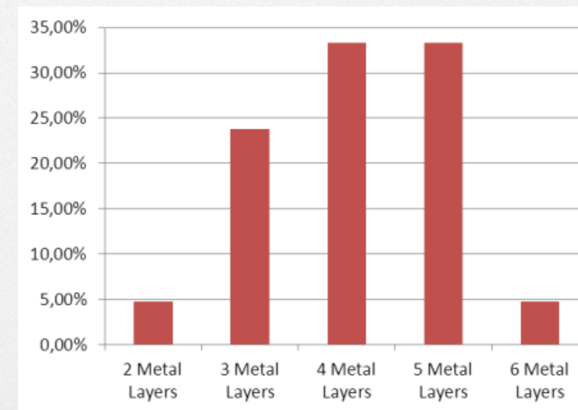
- Expected TID performances



- Expected SEE performances

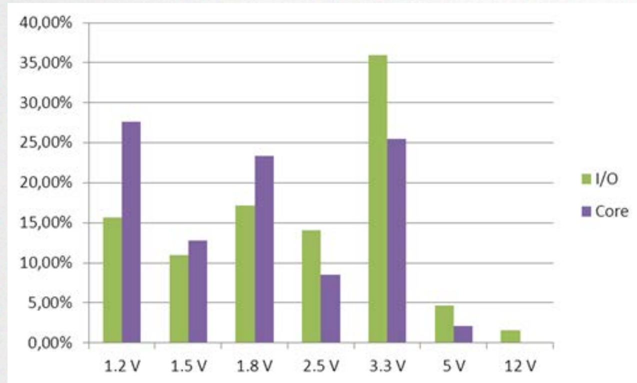


- Expected number of metal layers

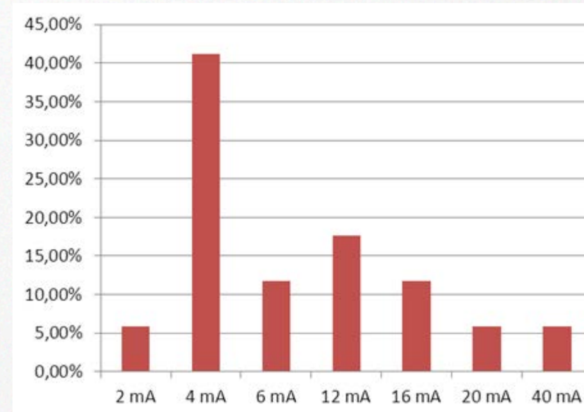


CONFIDENTIAL
SITAEL Property

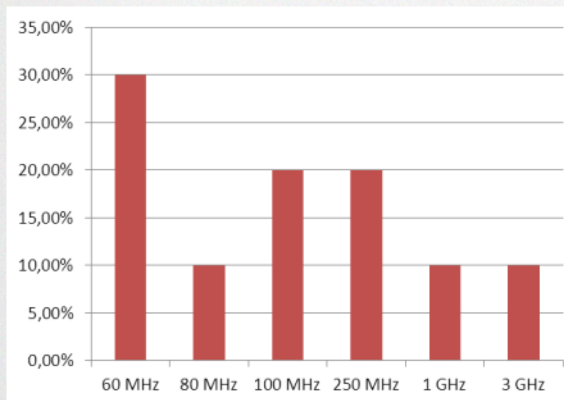
- Expected I/O and digital core power supply



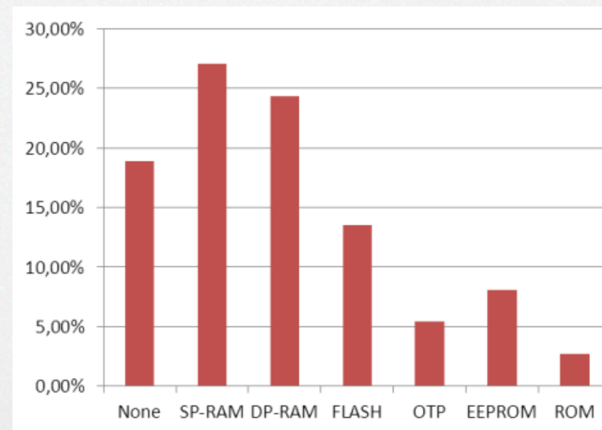
- Expected digital pad output current capability



- Expected toggle rate

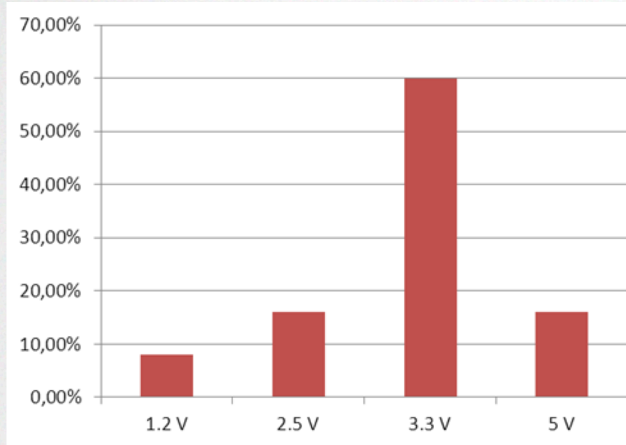


- Expected memories type need

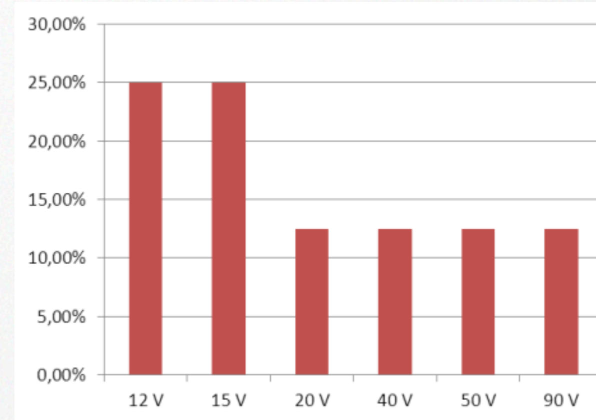


Analysis of Surveys

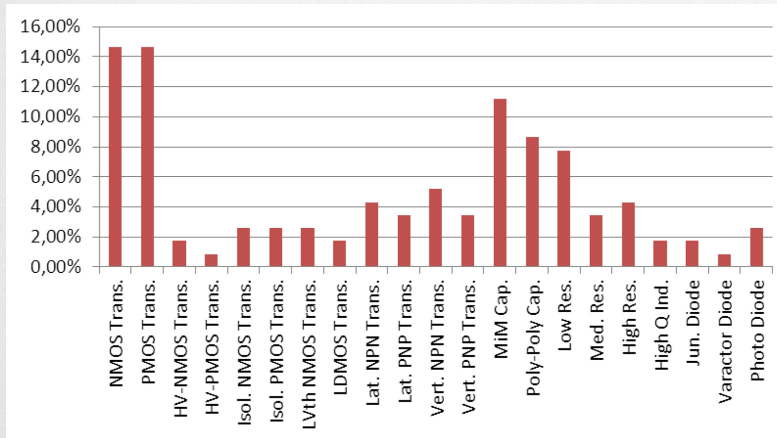
- Expected analogue core power supply



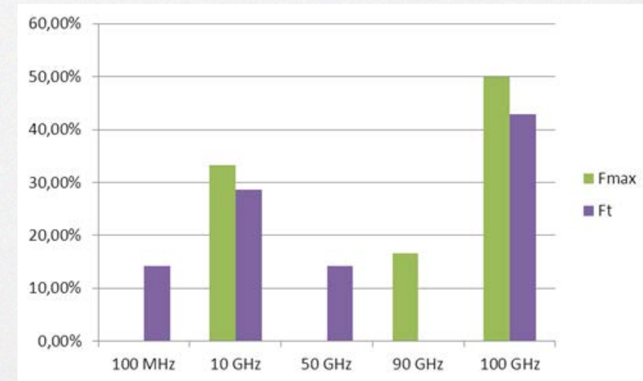
- Expected High Voltage capability



- Expected primitives availability



- Expected F_{MAX} and F_T



Conclusions of Surveys

The survey conclusions have been reported as a **grade of coverage of the needs against the features** of technologies process analyzed

The values have been calculated by a **weight average**, taking into account

- *Requirements*
- *Grade of needs*
- *Process features*

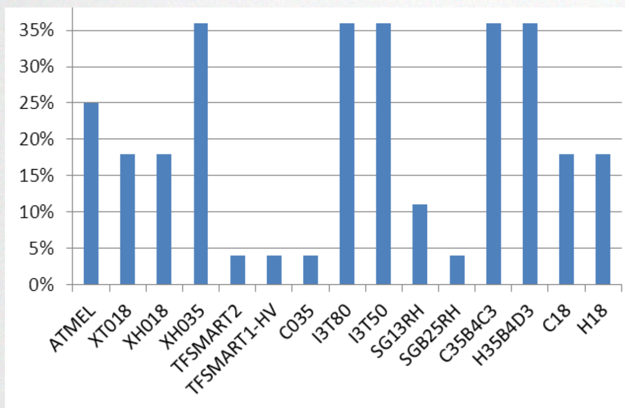
Parameters like

- Cost
- Qualification
- MPW runs per year

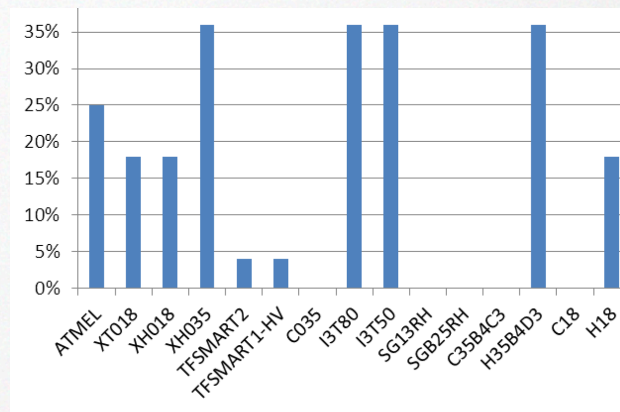
have **not been taken into account**.

Conclusions of Surveys

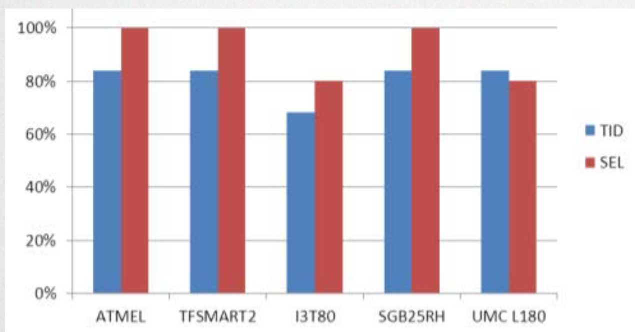
- Coverage of the required process gate lengths



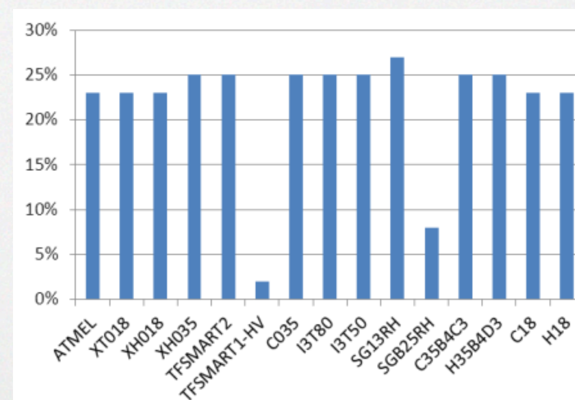
- Coverage of gate lengths and HV requirements



- Coverage of the TID and SEL performances

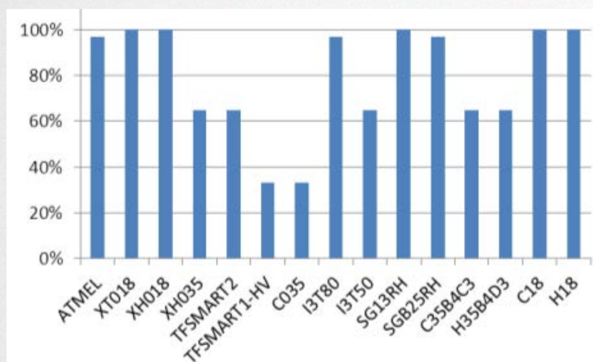


- Coverage of the required core digital power supply

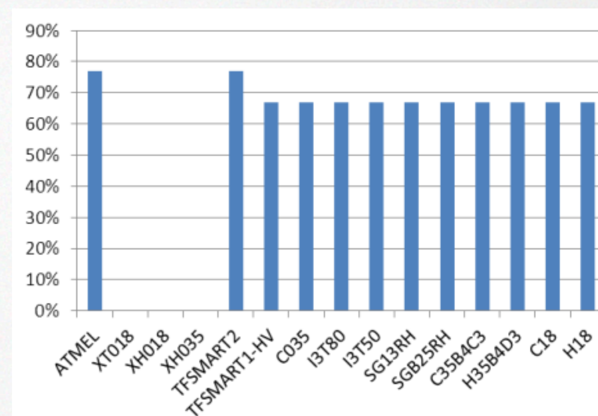


Conclusions of Surveys

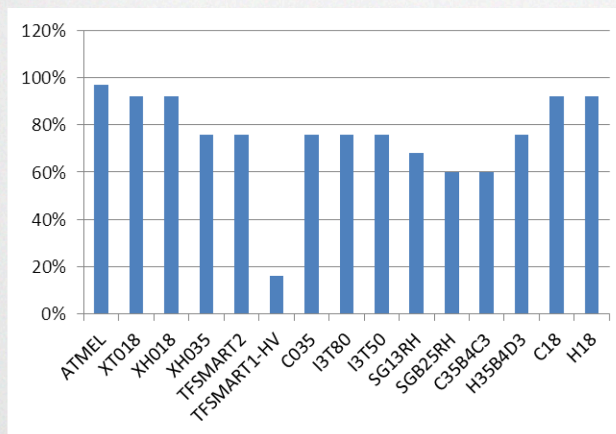
- Coverage of the number of requested metal layers



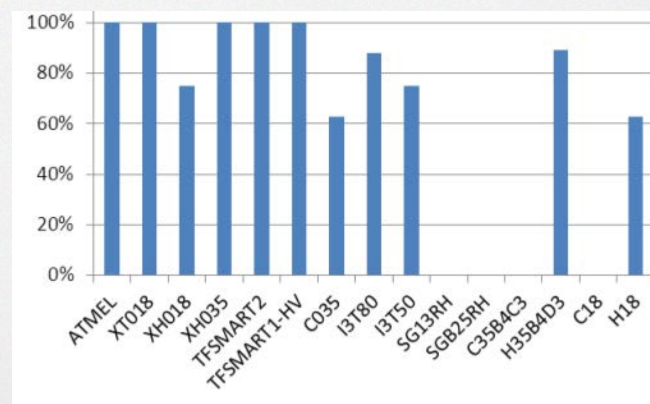
- Coverage of required speeds



- Coverage of the required analogue core low-range power supplies



- Coverage of the required analogue high voltage-range power supplies



Conclusions of Surveys

CONFIDENTIAL
SITAEL Property

- Growing demand of **High Voltage devices**
  and consequently
  Need to characterize an High Voltage technology process.

- On some High Voltage technologies, this activity is already planned for the future or it is in development status.

- Increasing importance on the availability of **Non Volatile Memory** (mainly FLASH memories but also EEPROM).

- Extend the **European technologies portfolio** usable for design of space applications ASIC.

Conclusions of Surveys

CONFIDENTIAL
SITAEL Property

Foundry	Process	Process Features	HV Option	NVM
Austria Micro System	C35B4C3	0.35um	No	EEPROM FLASH
	H35B4D3	0.35um	Yes	EEPROM
	C18	0.18um	No	N/A
	H18	0.18um	Yes	N/A
ATMEL	AT77.9K	0.15um	Yes	EEPROM
	AT58K85	0.15um	Yes	EEPROM
IHP Microelectronics	SGB25RH	0.25um	No	N/A
	SG13RH	0.13um	No	N/A
ON-Semi	C05	0.5um	No	EEPROM
	I3T50	0.35um	Yes	EEPROM
	I3T80	0.35um	Yes	EEPROM
Telefunken	TFSMART1-HV	0.8um	Yes	N/A
	TFSMART2	0.35um	Yes	N/A
XFAB	XH035	0.35um	Yes	EEPROM
	XH018	0.18um	Yes	EEPROM FLASH
	XT018	0.18um	Yes	EEPROM

Conclusions of Surveys

CONFIDENTIAL
SITAEL Property

Considering similar on-going activities on other technologies, higher digital density capability, FLASH availability, possibility to expand the technology portfolio for space device development, different gate length, the **XH018 process by XFAB** has been selected for the characterization activities planned in the second phase of the contract.

CONFIDENTIAL
SITAEL Property

A **Test Vehicle** is currently under design.

It will contain **primitive** devices and **simple analogue** circuits.

For each devices type, the evaluation will focus on:

- *I-V curves extraction*
- *C-V curves extraction*
- *Noise characterization*
- *End of life (EOL) test*
- *Total Ionization Dose (TID) test*.

The **Single Event Transient (SET)** will be characterized in term of pulse width and charge injected by a test session based on pulsed laser. A comparative test session will be applied with proton or heavy ions.

At the end of test campaign **analogue models** for simulations will be extracted in different condition (EOL, TID, SET,….) and they will be incorporated into the design-kit to allowing to designer a more accurate design and verification under critical conditions.

Franco Bigongiari
Technical Office Responsible
franco.bigongiari@sitael.com

THANK YOU!

SITAEL S.p.A.
S. P. 231, KM. 1+300 - 70026 Modugno (BA)
Via Livornese 1019 - 56122 Pisa (PI)
ITALY
phone: +39 080 53 21 796
Fax: +39 080 53 55 048
info.space@sitael.com
www.sitael.com