Assessment of Mixed Signal Technology

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Abstract

In 2013, within the ECI (European Component Initiative) program of the European Space Agency, the activity "Assessment and characterisation of Mixed Signal Technology" has been initiated. In this paper the activities performed for the assessment of an European mixed signal technology for the development of ASICs for space applications will be described. The assessment has been conducted through different surveys and the results obtained from them will be presented and analysed. Finally a brief description of the test vehicle for the technology characterization will be provided.

I. Introduction

The "Assessment and characterisation of Mixed Signal Technology" activity has been funded by European Space Agency in order to collect information of mixed signal ASIC processes with particular focus on their capability for space applications. The information on requirements to be supported by mixed signal technologies have been collected from [1], [2] and [3] and through a survey with the collaboration of space community. The tentative was addressed to look for information about similar on-going activities and on existing analogue, digital and mixed signal libraries or ASICs for space applications already manufactured or designed to avoid to duplicate the efforts.

The collected data on the user need has been compared against the processes capabilities available in Europe for mixed signal ASIC manufacturing. At the end of this review one particular process has been choosen for a further reliability and radiation characterization.

The paper is organized as follows: in the Section II the surveys carried out will be described. The results will be shown and discussed in Section III. In Section IV, a description of the test vehicle will be reported together to the test procedure and the list of the parameters to be measured; finally the conclusion will be reported in Section V.

II. Description of Surveys

The assessment of an European mixed signal technology for ASIC design and manufacturing has been driven by 3 different surveys. In the first survey a comparative assessment and verification about the availability of several existing European mixed signal technologies has been performed. In the second survey, inputs covering the needs for mixed-signal ASICs from the space community and the Agency's planned missions have been collected. In last survey, information about the existing rad hard libraries and design kits in terms of primitive devices, SEEs, TID and reliability performances have been collected.

In the next paragraphs each survey will be described and detailed.

A. First Survey: Mixed Signal Technologies Availability

This survey has been addressed to European foundries accessible to the Agency's member states. Twelve (12) European and Non-European manufacturers have been contacted obtaining reply from six (6) of them: Atmel, Austria Micro Systems (AMS), IHP Microelectronics, ON Semiconductor, Telefunken Semiconductor and XFAB. In total, data from 18 technology processes have been collected and analyzed.

The survey was split into 2 sections.The first part focused on general items related to the foundry availability, in particular addressing following questions:

- Licensing and conditions for use
- Foundry expected lifetime
- Foundry loading and product range
- Foundry process options
- Manufacturing turnaround time
- Manufacturing options (Full mask, MPW, MLM; Runs per year; longer availability) and their cost
- Cost of the supported tool chain (external and custom)
- Cost of the digital and analogue design-kit (front- and back-end)
- Supported batch manufacturing
- Supported Digital and Analogue development flows and constraints
- Foundry macro libraries cost
- Third party macro libraries access, conditions, cost and license
- Design kit for usage within space user community and the right for modifications
- Eventual technical support and maintenance of space-DK/libraries for European Space community

In the second part of the survey, specific information about environment, quality, digital performances and

analogue performances of different processes have been collected.

i. Environment

The questions related to environment features have been:

- Temperature range (operational and storage)
- Voltage range
- Radiation tolerance (TID, SEE: SEL, SEU, SET, SEGR, ...)
- ESD and EMC levels supported

ii. Quality

The questions related to quality features have been:

- Intrinsic reliability data/performance
- Wafer thickness
- Process lifetime
- Mean time to failure (FIT)
- Manufacturing yield
- Manufacturing quality systems
- Inspectibility of the manufacturing quality system and PID
- Cost associated with quality inspection
- Reporting and inspectibility of the process control monitors
- Process stability reporting the manufacturing process changes
- Failure analysis support
- Manufactured high-reliability and space qualified flows/components

iii. Digital Performances

The questions related to digital performances features have been:

- Gate density
- Power consumption
- Clock frequency
- Supply voltage range
- Number of metal layers
- Leakage
- Cell library (combinational and sequential; commercial and radiation hardened variants)
- Foundry and/or Third party digital macro libraries (commercial or radiation-hardened; development/qualification state)
- IO Pads (Voltage levels, ESD, EMC, ...)
- Manufacturing spread (power consumption, clock frequency, leakage)
- Accuracy of the models
- Development tool flow supported
- Sign-off tool chain

iv. Analogue Performances

The questions related to analogue performances features have been:

- Analogue IO Pads (Voltage levels; ESD; EMC; ...)
- Number of poly layers
- Sub-threshold conducting model
- Accuracy of the models
- MOS transistors availability
- Bipolar transistors availability
- Diodes availability
- Passives availability
- Development tool flow supported
- Sign-off tool chain
- Foundry or Third-Party analogue macro libraries (commercial or radiation-hardened; development/qualification state) and their support

Table 1 summarizes the list of contacted foundries and the corresponding 18 processes analyzed (processes which require manufacturing steps in USA have been excluded from the analysis due to the resulting ITAR export restriction which may be implied for space applications):

Table 1: Foundry processes analysed.

Foundry	Process	Process Features
Austria Micro System	C35B4C3	0.35um
	H35B4D3	High Volt. 0.35um
	C18	0.18um
	H18	High Volt. 0.18um
ATMEL	AT77.9K	High Volt. 0.15um
	AT58K85	High Volt. 0.15um
IHP Microelectronics	SGB25RH	0.25um
	SG13RH	0.13um
ON-Semi	C3/D3	0.35um
	C05	0.5um
	I3T25	High Volt. 0.35um
	I3T50	High Volt. 0.35um
	I3T80	High Volt. 0.35um
Telefunken	TFSMART1-HV	High Volt. 0.8um
	TFSMART2	High Volt. 0.35um
XFAB	XH035	High Volt. 0.35um
	XH018	High Volt. 0.18um
	XT018	High Volt. 0.18um

B. Second Survey: Agency and Space Community Needs

The survey has been addressed to the space community in order to collect feedbacks covering the needs of mixed-signal ASICs for the planned missions.

Twenty-eight (28) companies have been contacted, collecting eighteen (18) compiled surveys.

C. *Third Survey: Investigation about Comparable Activities*

To avoid to duplicate the effort and in order to harmonize and coordinate with on-going existing activities, a third survey addressed to the space community has been prepared to collect information about the existing rad hard libraries and design kits in terms of primitive

devices, SEEs, TID and reliability performances. The questions have been grouped in the four (4) sections: Primitive Devices, Single Event Effects Test, Total Dose Ionization Test and Reliability Test

i. Primitive Devices

- Funding mechanism used for rad hard libraries development (self-funding, public funding, private funding, etc.)
- Availability free of charge of the results (libraries, design-kits,…) for scientific research
- List of scientific papers published about the performances of Rad Hard libraries
- Technology process used to develop the Rad Hard libraries
- List of primitive devices with increased radiation tolerance
- For each primitive device, list of updated parametric cells (symbol and layout view)
- List of the violated design rules, accepted by the foundry
- List of modification on the fabrication process
- List of the modification on the design and layout-versus-schematic rules taking into account the modifications on primitive devices
- List of the modified primitive devices model
- List of analog simulators supported by these new models
- List of digital libraries developed based on this library
- Type of characterization performed on digital libraries

ii. Single Event Effects

- List of test(s) to evaluate the Single Event Effects
- Description of manufactured test vehicle/custom ASIC for SEE characterization/modeling
- Parts or devices included in the test vehicle
- Parts or devices not included in the test vehicle
- Parts or devices tested
- Heavy ions or protons source has been used
- Description of heavy ions/protons cocktail and LET used
- List of primitive devices tested against SEE
- Measured performances in terms of SEL, SEU, SET, SEB, SEGR, SEFI
- Test procedure used (i.e. ECSS 25100)
- Description of the SEE test by laser
- SEE performances obtained with laser test
- Description of simulation model to take into account the SEE effects
- List of analog simulators supported by these new models

iii. Total Dose Ionization Test

- List of test to evaluate the performances in terms of Total Ionization Dose (TID)
- Description of manufactured test vehicle/custom ASIC for TID characterization/modeling
- Parts or devices included in the test vehicle
- Parts or devices not included in the test vehicle
- Parts or devices tested
- Description of the source used
- Final TID accumulated
- What was the dose rate?
- List of primitive devices tested against TID
- Test procedure used (i.e. ECSS 22900)
- Description of simulation model to take into account the TID effects
- List of analog simulators supported by these new models

iv. Reliability Test

- Description of reliability test performed on the library
- Description of the obtained results

III. Analysis of Surveys

In the next figure haves been summarized the main results extracted from the three (3) surveys.

Figure 1 summarizes the preferred mixed-signal foundries expected to be used for future ASIC manufacturing;. Figure 2 -Figure **7** summarizes the users preference with respect to The process gate length, the technology lifetime, the operational temperature range, the TID and the SEE performances expected from technologies for development of mixed signal ASIC for space applications.

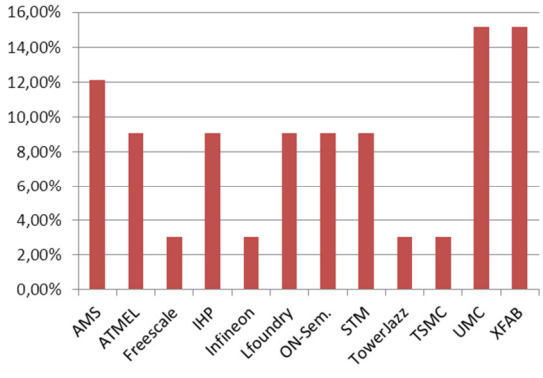

Figure 1: Preferred mixed-signal ASIC foundries.

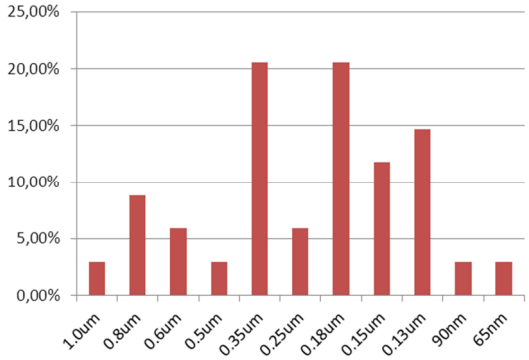

Figure 2: Preferred mixed-signal ASIC process gate length.

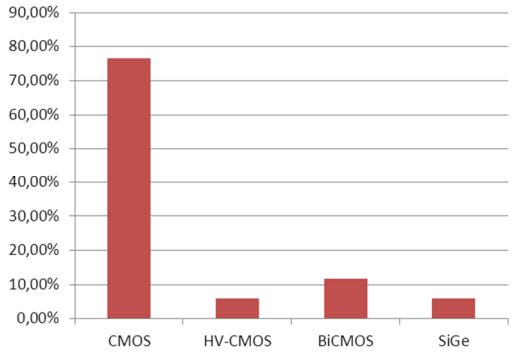

Figure 3: Preferred mixed-signal ASIC technologies.

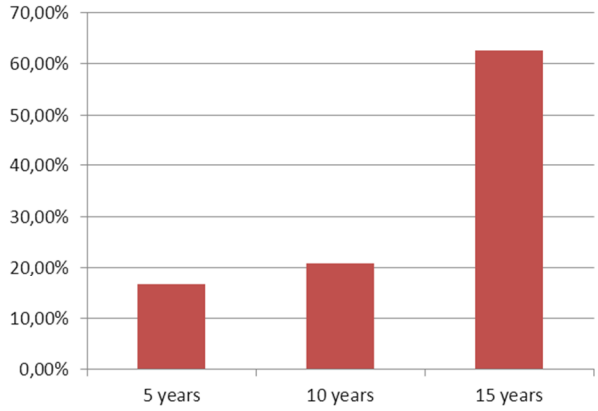

Figure 4: Expected technology's lifetime.

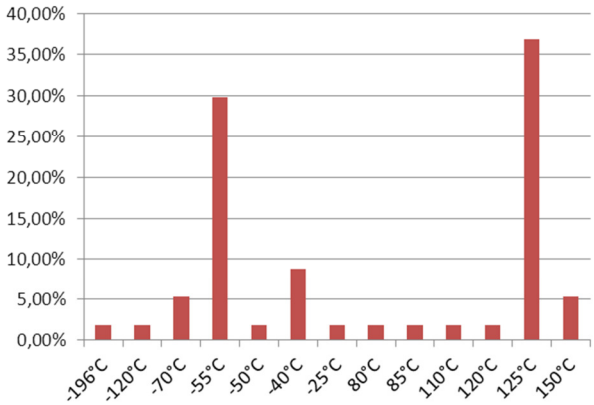

Figure 5: Expected operational temperature range.

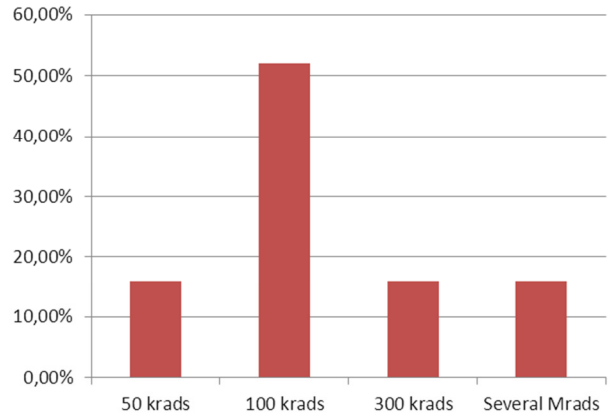

Figure 6: Expected TID performances.

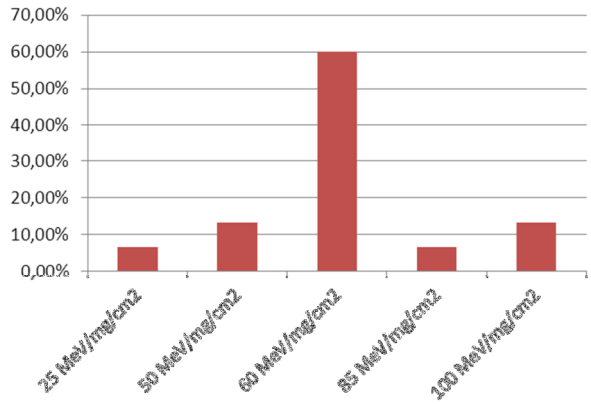

Figure 7: Expected SEE performances.

From Figure 8 to Figure 12 the expected performances and requested features to the preferred mixed signal technologies for the digital devices is shown, such as the I/O and digital core power supply, the number of metal layers, the digital output pad current capability, the toggle rate and the memories type needs.

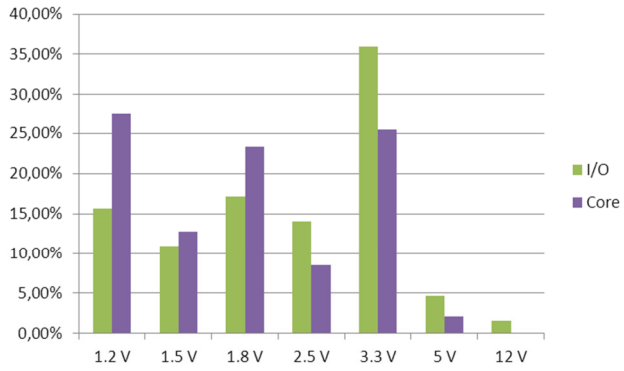

Figure 8: Expected I/O and digital core power supply.

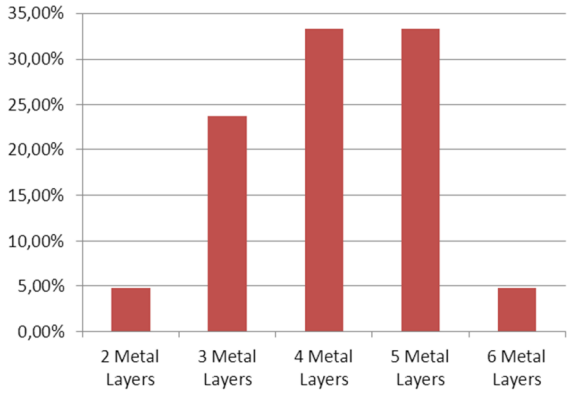

Figure 9: Expected number of metal layers.

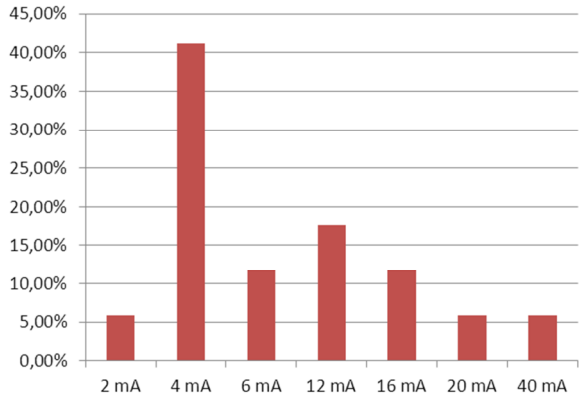

Figure 10: Expected digital pad output current capability.

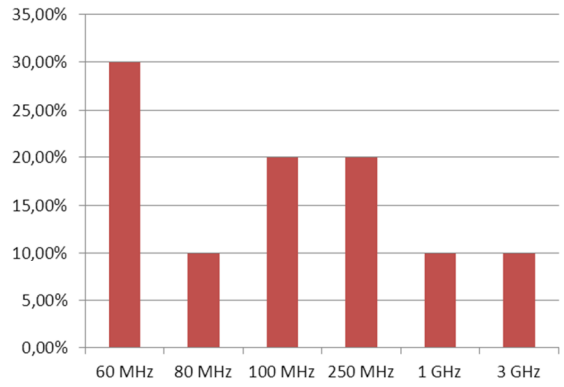

Figure 11: Expected toggle rate.

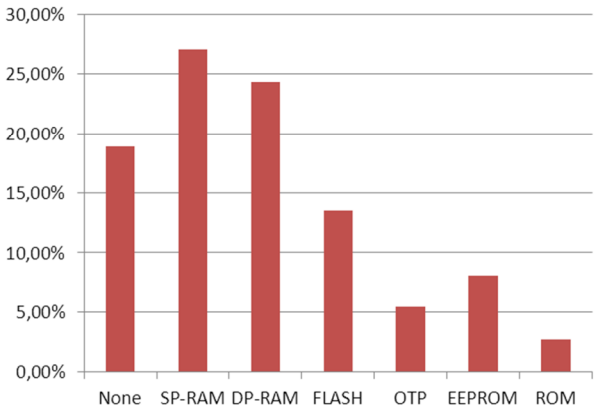

Figure 12: Expected memories type need.

From Figure 13 to Figure 18 the expected performances and features requested to the preferred mixed signal technologies for the analogue devices is shown, such as the analogue core power supply, high voltage needs, the primitive devices availability, the F_{MAX}, F_T and beta (for bipolar primitives) expected and the preferred analogue IP cores availability.

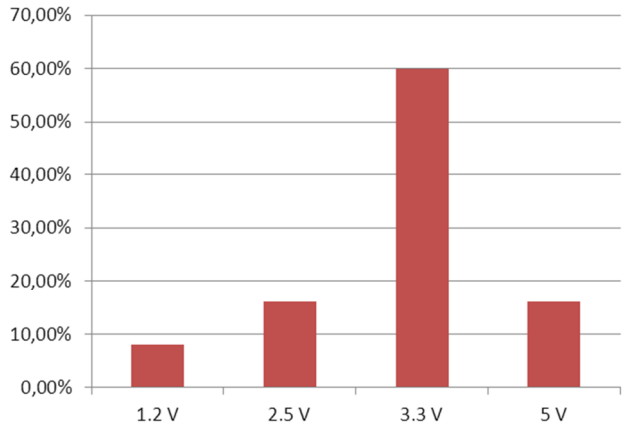

Figure 13: Expected analogue core power supply.

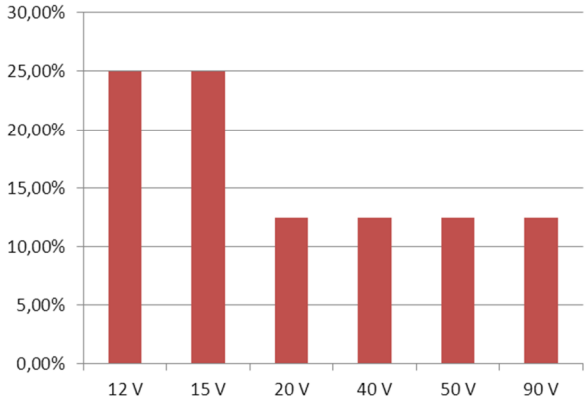

Figure 14: Expected High Voltage capability.

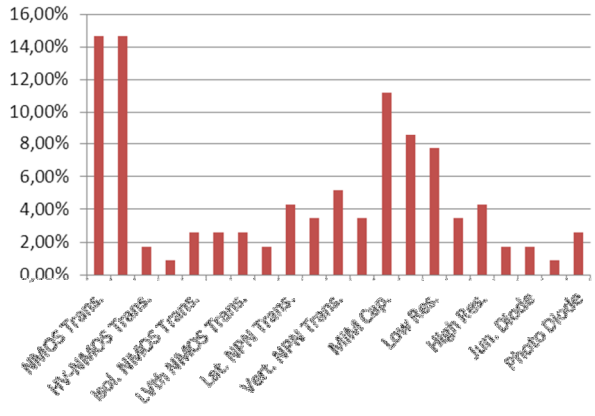

Figure 15: Expected primitives availability.

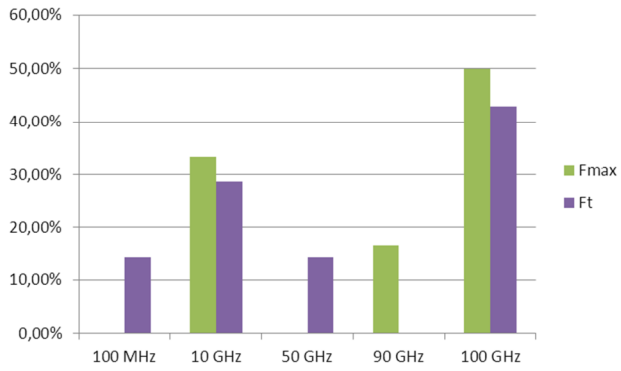

Figure 16: Expected F_{MAX} and F_T.

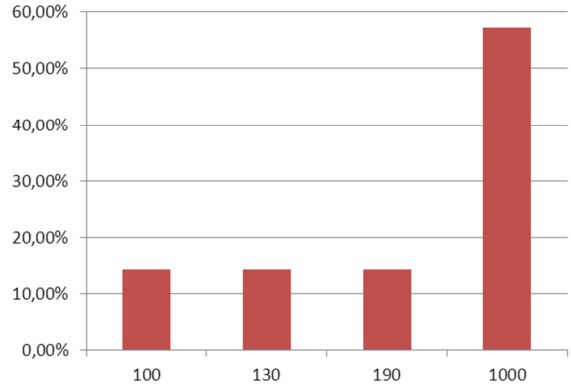

Figure 17: Expected beta values for bipolar transistor.

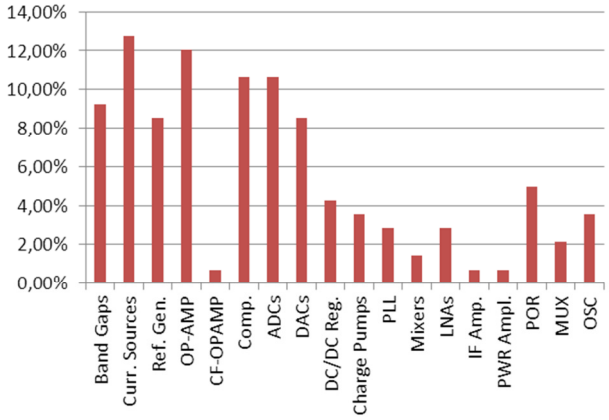

Figure 18: Expected analogue IP cores availability.

Analysing the data shown in the previous figures has been deduced that the features requested are mainly:

- Gate length of 0.35um or 0.18um (they can cover almost the 50% of need)
- CMOS technology with bipolar and high voltage option and with 15 year of lifetime
- Operational temperature range from -55°C to +125°C
- A 100Krad of TID limit can cover more than 50% of needs as well as a LET of 60MeV/mg/cm^2 it is enough for 60% of applications
- The 1.2 V, 1.8 V and 3.3 V of digital core power supply cover the most applications whereas the 3.3 V is the most requested for the I/O pads
- Technologies with up to 5 metal layers, with output pad with 4 mA of current capability and toggle rate below 250 MHz can cover the main applications
- Beside the static RAM (single or dual port) considerable importance is the availability of nonvolatile memory availability such as Flash.
- For analogue domain a technology with a 3.3 V of core power supply and up to 50 V of high voltage capability appears to cover the needs of most applications

The figures below summarize the conclusions reported above giving a grade of coverage of the needs against the features of technologies process analyzed; the values have been calculated by a weight average, taking into account the requirements, the grade of needs and the process features. Parameters like cost, qualification, MPW runs per year, … have not been taken into account.

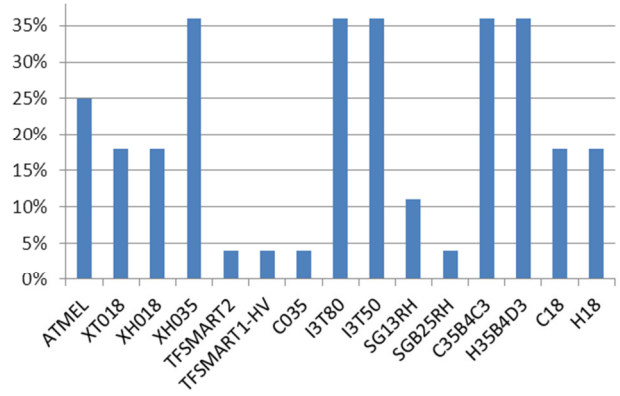

Figure 19: Coverage of the required process gate lengths.

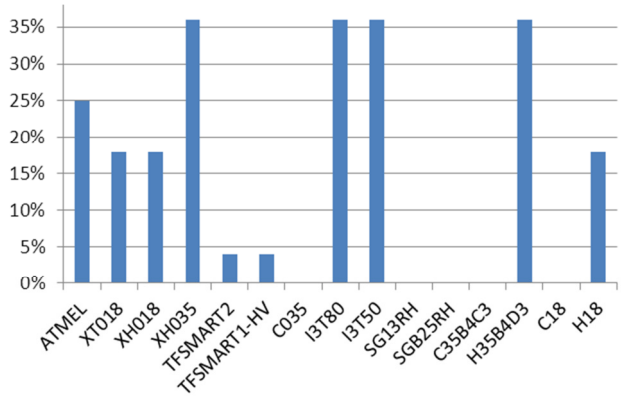

Figure 20: Coverage of gate lengths and HV requirements.

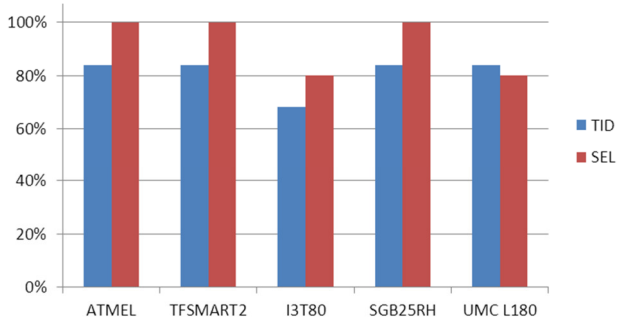

Figure 21: Coverage of the TID and SEL performances (the UMC L180 process has been introduced as reference).

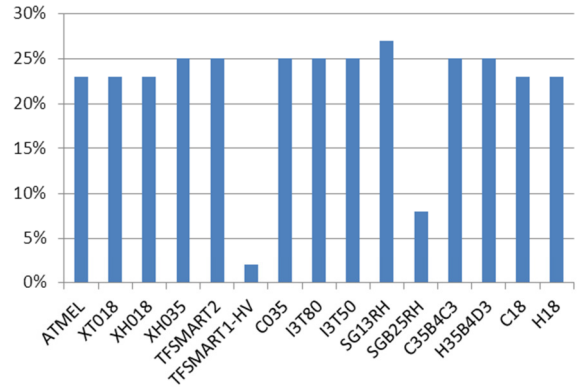

Figure 22: Coverage of the required core digital power supply.

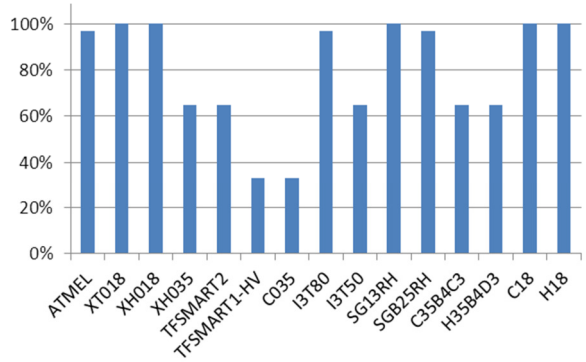

Figure 23: Coverage of the number of requested metal layers.

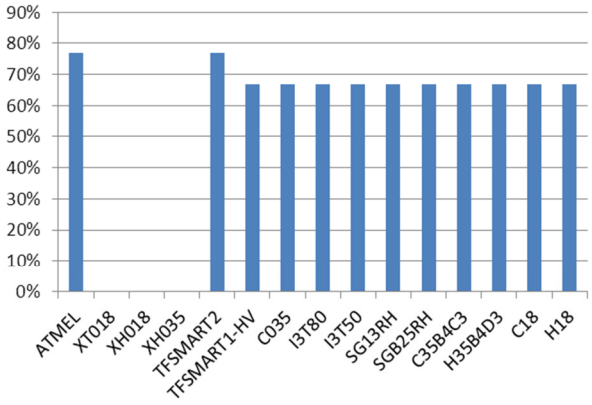

Figure 24: Coverage of required speeds.

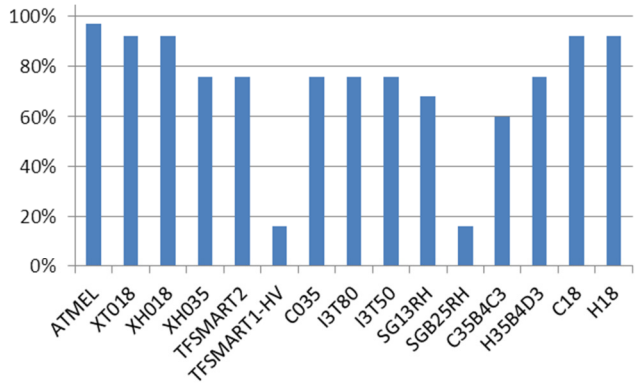

Figure 25: Coverage of the required analogue core low-range power supplies.

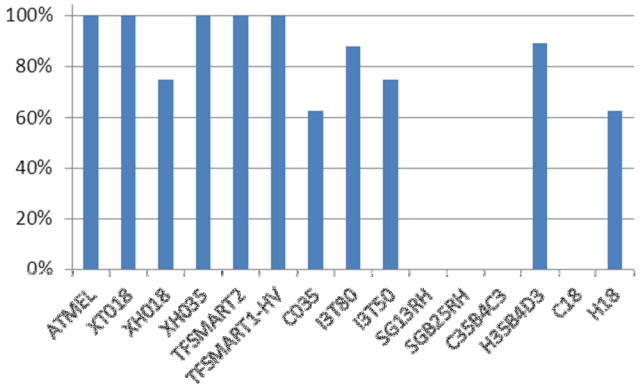

Figure 26: Coverage of the required analogue high voltage-range power supplies.

The availability of a process with High Voltage (HV) capability was a key requirement in order to meet the growing demand for HV power devices. Up to now no HV process has been submitted to a complete space qualification campaign, even if, for some technologies, this activity is planned for future or it is in development status.

Another important aspect to take into account for the process technology selection is the availability of Non Volatile Memory (mainly FLASH memories but also EEPROM). The status of NVM availability for mixed signal technology selected is reported in Table 2:

Table 2: NVM availability status.

Foundry	Process	NVM
Austria Micro System	C35B4C3	EEPROM FLASH
	H35B4D3	EEPROM
	C18	N/A
	H18	N/A
ATMEL	AT77.9K	EEPROM
	AT58K85	EEPROM
ON-Semi	C05	EEPROM
	I3T50	EEPROM
	I3T80	EEPROM
Telefunken	TFSMART1-HV	N/A
	TFSMART2	N/A
XFAB	XH035	EEPROM
	XH018	EEPROM FLASH
	XT018	N/A

By taking the conclusions from above, following main technology requirements for a mixed signal ASIC technology has been concluded:

- HV analog core capability
- NVM capability
- RH digital libraries, or analog/mixed signal RH IP, or analog PDK already developed or in development status or planned for future work

Based on the review of the data collected by the questionnaires and by consideration that several ESA and national Space Agencies activities are currently on-going or

have been completed on various technologies (e.g. ATMEL mixed signal processes are being characterised in the frame of a different project) the following candidate short list for the execution of the characterisation work planned in the phase 2 of this ECI activity has been concluded.

Table 3: Foundry process short list for phase 2

Foundry	Process	NVM
Austria Micro System	H35B4D3	EEPROM
ON-Semi	I3T80	EEPROM
XFAB	XH018	EEPROM FLASH

As mentioned above, due to the higher digital density capability, a 0.18µm process is expected to cover more application needs as compared to a 0.35µm process, XH018 has been chosen for the characterization activities planned in the second phase of this ECI contract.

IV. Description of Test Vehicle

As mentioned above, the second phase of this activity will focus on the characterisation of the selected process. The technology characterization test vehicle is currently being designed and will contain primitive devices and simple analogue circuits. For each devices type, the evaluation will focus on I-V and C-V curves extraction, noise characterization, end of life (EOL) test and Total Ionization Dose (TID) test. The Single Event Transient (SET) will be characterized in term of pulse width and charge injected by a test session based on pulsed laser. At the end of test campaign analogue models for simulations will be extracted in different condition (EOL, TID, SET,….) and they will be incorporated into the design-kit to allowing to designer a more accurate design and verification under critical conditions.

Since it is difficult to correlate the laser energy with the equivalent LET, heavy ion beam test for the selected technology devices are foreseen and are in preparation.

Currently heavy ion beam test for the selected technology devices are foreseen and are in preparation and it will be useful because the laser tests do not give indication whether the HV transistors survive the heavy ions. Moreover the heavy ion beam test will allow to know what charge injection is to be expected with LET because this information is not easily achievable with laser test.

V. Conclusions

In this paper foundry process appropriate for the manufacturing of mixed signal ASICs for space applications have been assessed.

The investigation has been driven by three (3) different surveys addresses respectively to European foundries, space community and companies and design centre involved in similar activities.

A candidate short list for the execution of the characterisation work planned in the phase 2 of this ECI activity has been concluded based on the results and analysis that was performed. Finally a brief description of the test vehicle for the technology characterization has been presented.

Of course different requirements and emphasis might affect the outcome.

VI. Acknowledgements

The authors wish to thank the companies and research laboratories for their precious contribution on the data collection.

VII. References

[1] Proceeding of 4th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA) August 26 – 28 ESTEC - Noordwijk - The Netherlands

[2] Analogue & Mixed-signal ASIC Technology Requirements and Priorities of Space Industry Users: round table of 4th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications (AMICSA) August 26 – 28 ESTEC - Noordwijk - The Netherlands

[3] Proceeding of European Space Components Conference ESCCON 2013 March 12 – 14 ESTEC - Noordwijk - The Netherlands