Radiation Hardness Tests of the CLARO-CMOS Chip: a Fast and Low Power Front-end ASIC for Single-Photon Counting in 0.35 μm AMS CMOS Technology

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Abstract

The CLARO-CMOS is a prototype ASIC primarily designed for single-photon counting with multi-anode photomultipliers tubes (Ma-PMTs). The chip features 5 ns peaking time, a recovery time to baseline smaller than 25 ns, and a power consumption at the order of 1 mW per channel. It was developed in the framework of the LHCb RICH detectors upgrade at CERN, but also found application in the readout of Silicon Photo-Multipliers (SiPMs) and microchannel plates. The prototype, realized in AMS 0.35 µm CMOS technology, has four channels, each made of a charge amplifier with settable gain (3 bits) and a comparator with settable threshold (5 bits) that allow tuning the response of the chip to the gain spread of the Ma-PMT pixels. The threshold can be set just above noise to allow an efficient single-photon counting with vacuum photomultipliers. In the readout of SiPMs, the threshold can be set above the single photon signals, allowing to count events with two or more photoelectrons with high efficiency and good separation of the photoelectron peaks. The CLARO-CMOS chip was fully characterized on the test bench. The chip was coupled to a Hamamatsu R11265 Ma-PMT, the baseline photon detector for the LHCb RICH upgrade, and was found able to read-out single-photon signals up to the maximum average rate expected in the LHCb RICH (~10 MHz) with a low power consumption (~1 mW) and a negligible crosstalk between pixels. In the LHCb RICH environment, over ten years of operation at the nominal luminosity expected after the upgrade in Long Shutdown 2, the ASIC must withstand a total fluence of about $6 \cdot 10^{12}$ 1 MeV n_{eq}/cm^2 and a total ionizing dose of 400 krad. A systematic evaluation of the radiation effects on the CLARO-CMOS performance is therefore crucial to ensure long-term stability of the electronics front-end. We present results of multi-step irradiation tests with neutrons up to the fluence of 10^{14} 1 MeV n_{eq}/cm^2, with protons up to the dose of 8 Mrad and with X-rays up to the dose of 8 Mrad. During irradiation, cumulative effects on the performance of the analog parts of the chip and single event effects (SEE) were evaluated. The chips were biased continuously and the chip threshold voltages were measured regularly, in order to detect possible single event upsets (SEUs) affecting the threshold DAC settings. Power consumption was also monitored online, and an additional circuit provided protection against Single Event Latchup (SEL). S-curves were measured before and after each irradiation step, to follow the evolution of counting efficiency, threshold shifts and noise during the irradiation.

I. Introduction

The capability to detect single photon signals is a requirement shared between several different applications. For instance, the Ring Imagining Cherenkov (RICH) detectors exploit the light emitted by relativistic charge particles crossing a suitable medium to provide their identification over a wide momentum range. Such detectors are extensively used in high energy physics experiments and, particularly, in the LHCb experiment at CERN.

An update of the whole LHCb detector is foreseen in 2018 in order to make it able to run at higher luminosity and sustain a proton-proton collision rate of 40 MHz [1]. Also the RICH detector will be updated and the currently used Hybrid Photon Detectors (HPDs) will be replaced by Multi-anode PhotoMultiplier Tubes (Ma-PMTs) coupled with an external wide-bandwidth read-out electronics [2]. The baseline photon sensor for the LHCb RICH Upgrade is the R11265 Ma-PMT, produced by Hamamatsu, which ensures an adequate spatial resolution thanks to the small pixel size (3×3 mm^2) [3][4]. The photon detector planes will consists of several thousands R11265 Ma-PMTs located side-by-side to minimize the dead area. This results in a high channel density which forces the read-out electronics to operate at very low power consumption. Indeed, the front-end electronics must be placed as near as possible to the photon sensors in order to minimize the stray capacitance between neighbouring channels or from the input node to ground which can lead to an increase of the cross-talk and noise, respectively.

The CLARO chip [5] is a custom designed ASIC realized in the 0.35 µm CMOS technology from Austria Micro Systems (AMS). The CLARO is able to read-out the R11265 Ma-PMTs fulfilling the LHCb RICH Upgrade requirements. Although a new improved 8-channels version of the chip has recently been designed (not described in this proceeding), the first versions of the chip are equipped with 4 channels with a 8-bits digital register each. The good chip performance led the LHCb collaboration to choose it as the baseline front-end device for the Ma-PMT read-out [2]. As the CLARO is supposed to be used in the LHCb environment, radiation hardness tests are needed to verify the radiation tolerance of the technology. Thus, some chips were irradiated with

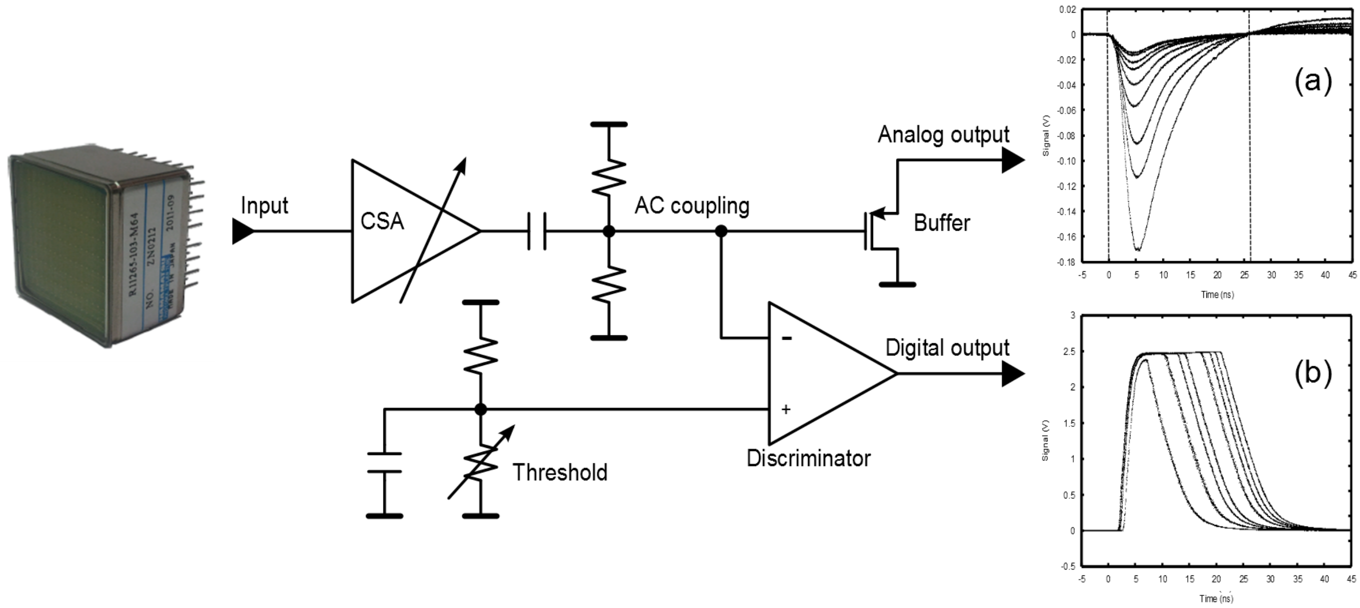

Figure 1: The block diagram of a CLARO CMOS channel. The typical analog and digital output signals are shown in figure 1.a and 1.b respectively.

neutrons, X-rays and protons so that the radiation hardness properties of several CLAROs could be studied in terms of both total ionizing dose (TID) and single event effects (SEE) [6].

A brief overview of the main chip features and of its performance is provided in Section II. The results of the radiation hardness tests are described in Section III.

II. THE CLARO CHIP

As shown in the block schematic (Fig. 1), the CLARO chip is essentially composed of an input Charge Sensitive Amplifier (CSA) and a Discriminator.

When a photon hits the Ma-PMT surface, a photoelectron is emitted from the photocathode starting the charge multiplication over the 12 dynodes. The collection time of the photon detector is very small, of the order of 1 ns. Thus, the typical signal at the anode consists of a $\sim 1\ \mathrm{Me^-}$ current pulse which is injected at the input node of the CLARO.

The CSA provides the amplification and the shaping of the input current giving a proportional exponential shaped voltage signal at its output. The rise time constant (τ_R) of the CSA is of the order of 1 ns and is proportional to the input capacitance, while the fall time constant (τ_F) amounts to ~ 5 ns, large enough for an effective integration of the fast pulses but short enough to sustain high rates without pile-up. The CSA is AC-coupled with a PMOS follower buffer and with a discriminator stage which provide the auxiliary analog output and the main digital output respectively.

Fig. 1.a shows the superposition of the signals read from the auxiliary analog output (input charge ranging from $330\ \mathrm{ke^-}$ to $3.3\ \mathrm{Me^-}$). The PMOS follower buffer, which allows to read the CSA output signal without adding capacitance at this node, was externally biased with a 1 kΩ resistance. Note that this output is not meant to be used for single photon counting but only for debugging purposes. As observable, the baseline is not well restored since an undershoot occurs after the pulses. Such behaviour is due to the AC coupling between the CSA and the buffer (~ 55 ns) and can lead to a threshold shift at photon counting rate higher than ~ 10 MHz. This is the main reason why in the new version of the chip the AC capacitance was removed and a DC-coupled approach was chosen.

The analog signal coming from the CSA is also read by a discriminator stage which provides a digital pulse in case it crosses a programmable threshold level (32 values available). Fig. 1.b shows the superposition of the signals acquired from the main digital output with a threshold level of $800\ \mathrm{ke^-}$ and for an input charge ranging from $810\ \mathrm{ke^-}$ to $5.6\ \mathrm{Me^-}$. As observable, the width of the pulses is proportional to the input charge, a feature which allows to adopt the technique based on the time-over-threshold to compensate the time walk in case the CLARO is used for precise time measurements. However, even for input signals ten times larger than the threshold the FWHM of the digital output signals is lower than 25 ns so that rates of 40 MHz can be sustained avoiding pile-up. As mentioned, each channel is equipped with a 8-bit register, similar to a SPI interface, which permits to select the CSA gain (3 bits, 8 values available) and the threshold level (5 bits, threshold step $150\ \mathrm{ke^-}$).

Another requirement that the CLARO CMOS has to fulfill is the low power consumption. Despite its wide bandwidth, the power consumption in idle mode amounts to about 1 mW per channel and it stays below 2 mW per channel even at a photon counting rate of 10 MHz. This ensures a low heat injection in the most illuminated areas of the RICH detector, avoiding the need for front-end cooling.

As mentioned, in order to ensure a suitable rise time (few ns), the input capacitance should not exceed few pF. Moreover, the series noise of the preamplifier is proportional to the input to ground capacitance, as shown in fig. 2, where the equivalent noise charge is plotted as a function of the input capacitance. With the CLARO CMOS mounted in a small QFN48 package, the total input capacitance was measured to be ~3.3 pF, mainly due to the input bonding pad, the bonding wire, the package and the interconnects (the contribution of the photon sensor is not included). In this best case condition, the ENC turns out to be $\sim 7.7\ \mathrm{ke^-}$. Note that also the stray capacitance between the input nodes of neighbouring pixels has to be minimized since it would result in an increase of cross-talk. In particular, the stray capacitance between the input nodes of neighbouring channels has to be negligible with respect to that due to the Ma-PMT alone (~ 0.5 pF). The minimization of the input capacitance guides the design of the CLARO PCBs and it is one of the main reasons to keep low the number of channels per chip, so that

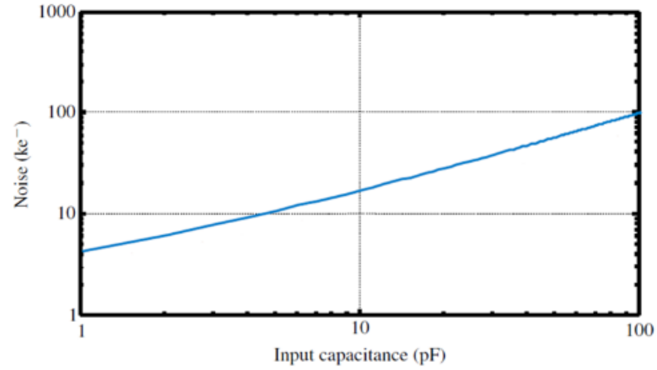

Figure 2: the input referred noise as a function of the input capacitance

the length of the traces connecting the pixels to the CLARO can be minimized.

In agreement with the LHCb Technical Design Review [2], the CLARO CMOS was chosen as the baseline front-end device for the read-out of the R11265 Ma-PMT for the LHCb RICH Upgrade. In addition to a deep characterization on the test benches, the CLARO CMOS performance was studied while reading the current signal coming from a R11265 Ma-PMT operating in single photon regime. Fig. 3 shows the superposition of single photon spectra acquired at different Ma-PMT biasing voltages. They are measured by illuminating the Ma-PMT with a LED and by counting the signal rates during a CLARO threshold scan. As it can be seen, the spectra look good and the signal to noise ratio is more than adequate since the single photon peak is clearly resolved. Moreover, the gain adjustment behaves as expected. Indeed, for analogous threshold step, setting a gain of 0.5 (points with a circular marker) the spectra are sampled with a double resolution with respect to the ones acquired using a gain of 0.25 (points with a x-cross marker). Anyway, in the last improved version of the CLARO CMOS, a finer threshold step is available in order to reach even higher resolution.

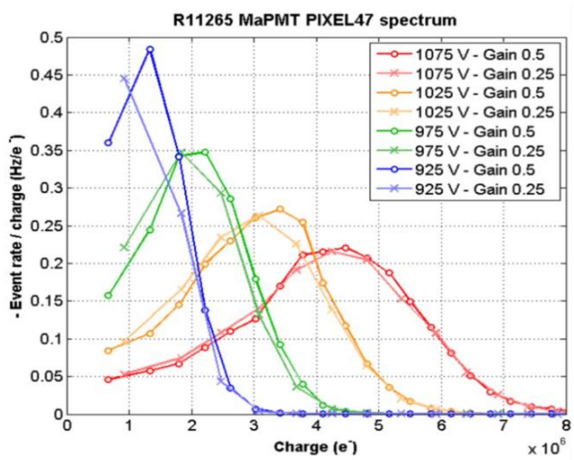

Figure 3: single photon spectra acquired by a R11265 Ma-PMT coupled with a CLARO CMOS chip.

III. Radiation Hardness Tests

All the electronic components which are supposed to be used in the LHCb environment have to pass the radiation hardness tests. Indeed, the radiation levels reached in the LHCb experiment could deteriorate the component performance in terms of Total Ionizing Dose (TID) and Single Event Effects (SEE). In order to ensure stable operation of the upgraded RICH detector over 10 years in the LHCb upgrade environment, a dedicated test of the CLARO performance under high radiation fields has been done.

Table 1 summarizes the radiation level expected in the LHCb Upgrade environment. The estimates are based on the worst case radiation level for a single proton-proton collision provided by M. Karacson [7] and assuming one year of LHCb operation (10^7 s), at a luminosity of $L=2\cdot10^{33}\ s^{-1}cm^{-2}$, with a proton-proton collision cross section of σ=84 mbarn. Note that the values shown in Table 1 do not include any safety factor and they could be affected by statistical fluctuations by a factor ~10-30 %. Furthermore, neither the final geometrical configuration nor the materials to be adopted are still completely defined and so they are not implemented in the current estimates.

Table 1: Radiation level expected per year in the LHCb RICH-1 and RICH-2 detectors

	Neutrons 1 MeV n_{eq}/cm^2	Hadrons E_H>20 MeV [cm^{-2}]	TID [krad]
RICH-1	$6.1\cdot10^{11}$	$2.3\cdot10^{11}$	39.6
RICH-2	$3.1\cdot10^{11}$	$1\cdot10^{11}$	15.9

In a very conservative approach, several CLAROs were irradiated up to a factor 10 times larger than the radiation level expected in 10 years of LHCb. The radiation hardness tests were performed irradiating the chip with neutrons, X-rays and protons.

A. *Neutron irradiation*

The neutron irradiation measurements were performed at the Université Catholique de Louvain-la-Neuve (Belgium) in May 2013. A cyclotron (T2 Hall) accelerates a deuteron beam on a beryllium target producing a high flux neutron beam (average energy ~23 MeV) with a very low gamma (2 %), proton and electron (0.02 %) contamination. Three CLARO PCBs were placed in a cascade configuration, powered and irradiated in three steps that correspond to 4, 40 and 160 equivalent years in LHCb (final cumulative fluence of ~ 10^{14} 1 MeV n_{eq}/cm^2). During the irradiation process the threshold level and the supply current were continuously monitored so that Single Event Upset or variation in the supply could be detected. Before and after each irradiation step bursts of 1000 identical test pulses was sent to all the CLARO inputs simultaneously and the number of discriminated output signals was measured for different input signal amplitudes. This process permits to acquire the “S-curves”, such as the one shown in Fig. 4. The position of the edge of the curve allows to evaluate any variation in the threshold level, while an increase of the noise would result in a smoother transition. As it can be seen, no significant increase of the noise was observed and also the variation of the threshold level turned out to be of the order of few percentage points. Furthermore, neither Single Event Upset nor Single Event Latch-up occurred.

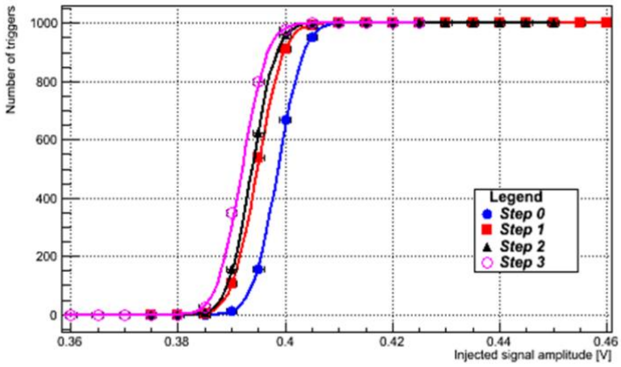

Figure 4: S-curve acquired during the neutron irradiation.

B. *X-rays irradiation*

In order to test the CLARO CMOS chip tolerance to the total ionizing dose (TID), a X-rays irradiation measurement was performed at the INFN National Laboratory in Legnaro (Italy) in September 2013. The X-rays were produced using tube with a tungsten anode biased at 50 kV. Two bare CLAROs (the lid which covered the ASIC was removed) were biased and irradiated in three steps that correspond to about 1, 10 and 110 years of LHCb operation (the final cumulative dose amounts to 4 Mrad).

The measurements performed are similar to those described in the previous section. Again, no Single Event Upset nor Single Event Latch-up occurred, while the supply current decreased by a factor 10-15 %. From the S-curves (see Fig. 5) a variation in the threshold level by a factor 10-15 % can be evaluated, while the noise did not change significantly.

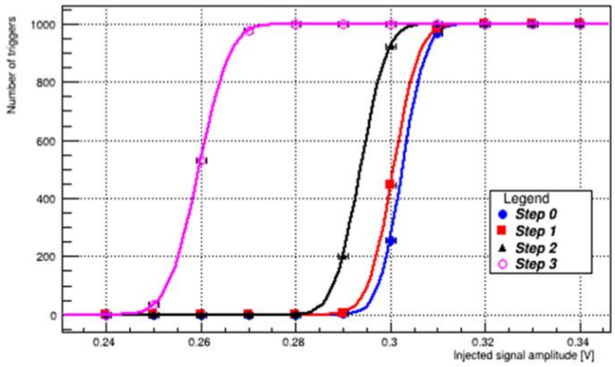

Figure 5: S-curve acquired during the X-rays irradiation.

C. *Proton irradiation*

Finally, the proton irradiation tests were performed at the Institute of Nuclear Physics, Polish Academy of Sciences in Krakow (Poland) in February 2014. The proton beam had an average energy of about 60 MeV and ensured a good uniformity over the CLARO CMOS area (beam diameter ~ 1 cm). Three bare CLARO were biased and irradiated in four steps that are equivalent to 1, 10, 100 and 190 years in the LHCb environment (final cumulative dose of 7.6 Mrad). Performing the usual measurements, no Single Event Latch-up was observed, a decrease by a factor 10-15 % in the supply current was recorded, while the threshold level reduced by a factor 15-20 %. Furthermore, a Single Event Upset occurred (see Fig. 6) which made the DAC output move abruptly from ~ 1.13 V to ~ 1.1 V. This event suggests to equip the new version of the CLARO with a register protected with triple modular redundancy and a SEU internal counter in order to monitor and correct such events.

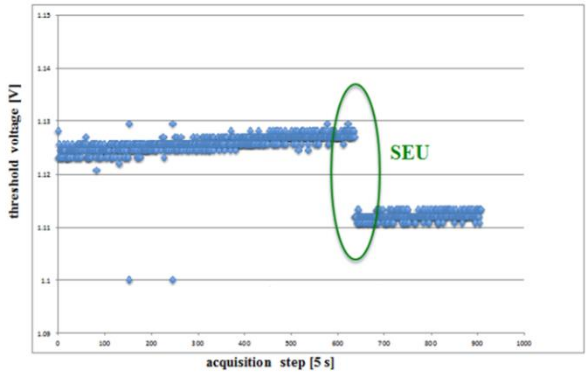

Figure 6: Single Event Upset observed during the proton irradiation.

IV. Conclusions

The CLARO CMOS chip has been described. It is an ASIC designed in 0.35 µm AMS CMOS technology for the readout of Ma-PMTs. The CLARO was chosen as the baseline front-end device to be used in the upgraded RICH detectors in the LHCb experiment. The main features of the chip are the capability to sustain high photon counting rate (up to 40 MHz) with a low power consumption (~ 1 mW per channel). The relative old technology also meets the requirements of minimizing the costs, enhancing the yield. The performance of the chip have been briefly described also when coupled with the R11265 Ma-PMT, produced by Hamamatsu. The results of the radiation hardness tests have been presented. The CLARO turned out to be tolerant to neutrons, X-rays or proton irradiation up to levels 10 times larger than those expected in 10 years of LHCb operation.

V. Acknowledgments

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