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# Radiation hardness tests of the CLARO-CMOS chip: a fast and low power front-end ASIC for single-photon counting in AMS 0.35 micron CMOS technology

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The CLARO-CMOS is a prototype ASIC primarily designed for single-photon counting with multi-anode photomultipliers (Ma-PMTs). The chip features 5 ns peaking time, a recovery time to baseline smaller than 25 ns, and a power consumption in the order of 1 mW per channel. It was developed in the framework of the LHCb RICH detectors upgrade at CERN, but also found application in the readout of Silicon Photo-Multipliers (SiPMs) and microchannel plates.

The prototype, realized in AMS 0.35 micron CMOS technology, has four channels, each made of a charge amplifier with settable gain (3 bits) and a comparator with settable threshold (5 bits) that allow tuning the response of the chip to the gain spread of the Ma-PMT pixels. The threshold can be set just above noise to allow an efficient single-photon counting with vacuum photomultipliers. In the readout of SiPMs, the threshold can be set above the single photon signals, allowing to count events with two or more photoelectrons with high efficiency and good separation of the photoelectron peaks.

The CLARO-CMOS chip was fully characterized on the test bench. The chip was coupled to a Hamamatsu R11265 Ma-PMT, the baseline photon detector for the LHCb RICH upgrade, and was found able to read-out single-photon signals up to the maximum average rate expected in the LHCb RICH (˜10 MHz) with a low power consumption (˜1 mW) and a negligible crosstalk between pixels.

In the LHCb RICH environment, over ten years of operation at the nominal luminosity expected after the upgrade in Long Shutdown 2, the ASIC must withstand a total fluence of about 6x10ˆ12 1 MeV n_eq/cmˆ2 and a total ionizing dose of 400 krad. A systematic evaluation of the radiation effects on the CLARO-CMOS performance is therefore crucial to ensure long-term stability of the electronics front-end.

We present results of multi-step irradiation tests with neutrons up to the fluence of 10ˆ14 1 MeV n_eq/cmˆ2, with protons up to the dose of 8 Mrad and with X-rays up to the dose of 8 Mrad. During irradiation, cumulative effects on the performance of the analog parts of the chip and single event effects (SEE) were evaluated. The chips were biased continuously and the chip threshold voltages were measured regularly, in order to detect possible single event upsets (SEUs) affecting the threshold DAC settings. Power consumption was also monitored online, and an additional circuit provided protection against Single Event Latchup (SEL). S-curves were measured before and after each irradiation step, to follow the evolution of counting efficiency, threshold shifts and noise during the irradiation.

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