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A Complete Space Based CCD Biasing Solution in a 0.35µm High Voltage CMOS ASIC

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Outline

- History
- Motivation
- Architecture
- Circuit design & layout
- Experimental results
- Future work & conclusions

History

- ASIC Design Group at RAL, original background in design for Particle Physics detectors (extensive work on CMS detector in LHC @ CERN).
- Experience in design for high radiation environments.
- Now operate across many scientific areas (Space, Nuclear Physics, Synchrotrons/XFELs).
- Established record of chip design for space applications.
- Chips flown or designed into many missions:

  - Polar(CEPPAD), Cluster(RAPID), Rosetta(Ptolemy), MINISAT-01(LEGRI), TopSat, STEREO(SECCHI), SDO(AIA & HMI), GOES(SUVI), IRIS(IRIS), Bepi-Columbo(SIXS)

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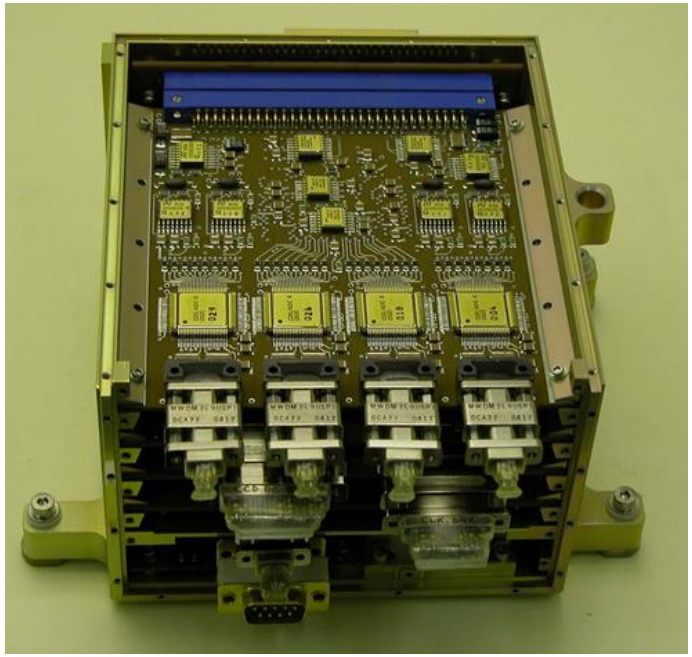
Motivation

- CCD bias generation uses 1 of 4 PCBs in SDO camera electronics box.
- Uses custom LV ASIC for control with HV discrete op-amps for buffering.
- High power & area. Space qualified component issues.
- **Integrate entire biasing PCB into a single device, save on area, power, mass.**



SDO camera electronics box
(152mm x 131mm x 95mm)

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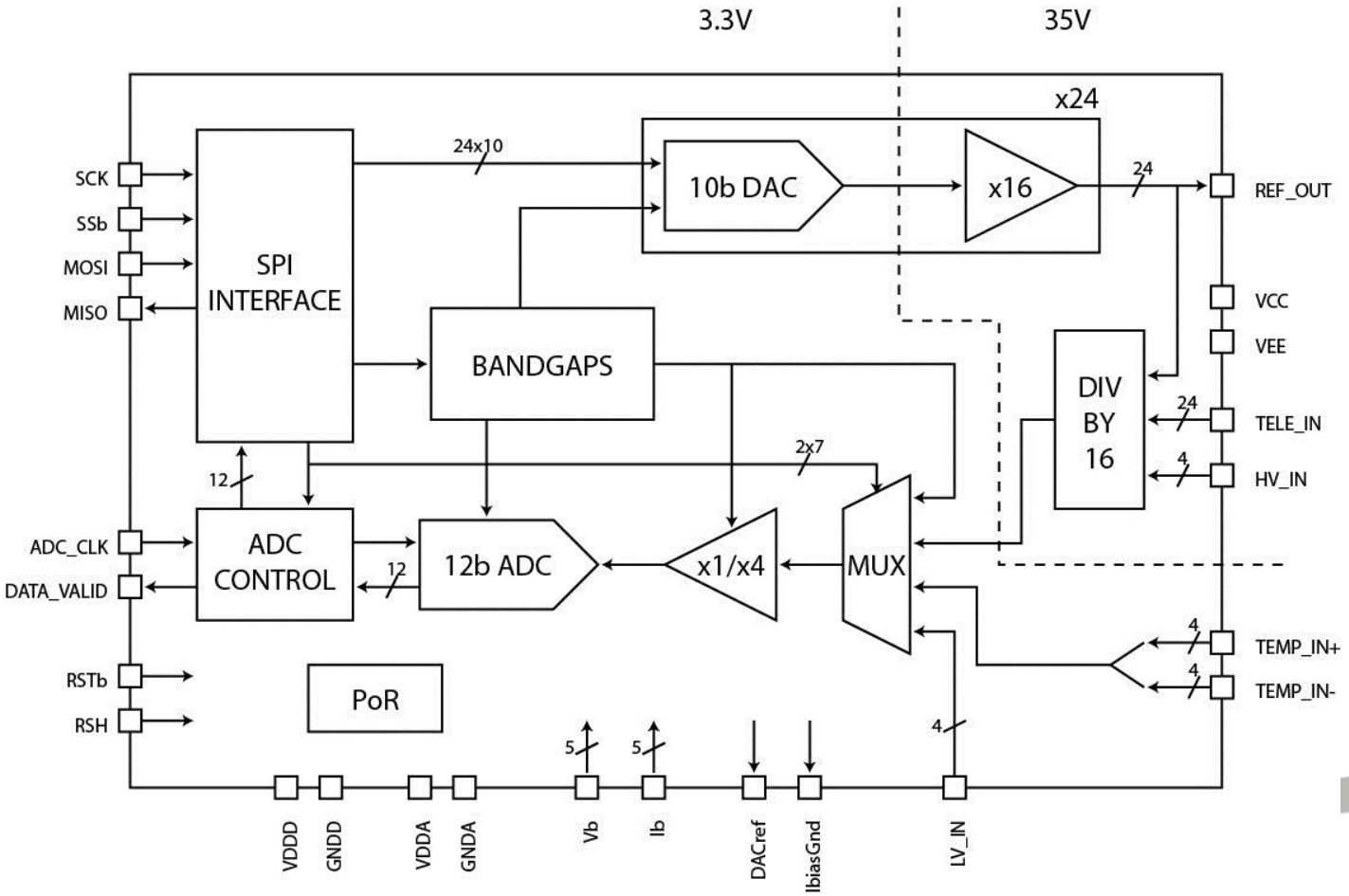
Requirements

- Single chip solution – no extra active components.
- Sufficient outputs to independently bias 4 quadrants of a scientific CCD.
- Internally generated voltage & current references.
- 0-32V output range, +/-20mA drive capability.
- Low bandwidth for low noise outputs (<100µV RMS).
- Stable for capacitive loads of 10pF - 10µF.
- Integrated telemetry system.
- Digital control over LV serial interface.
- >100KRad TID hardness, SEU & SEL resistant.
- -40°C - +125°C operation.

STAR ASIC Architecture



Space Telemetry And Reference ASIC

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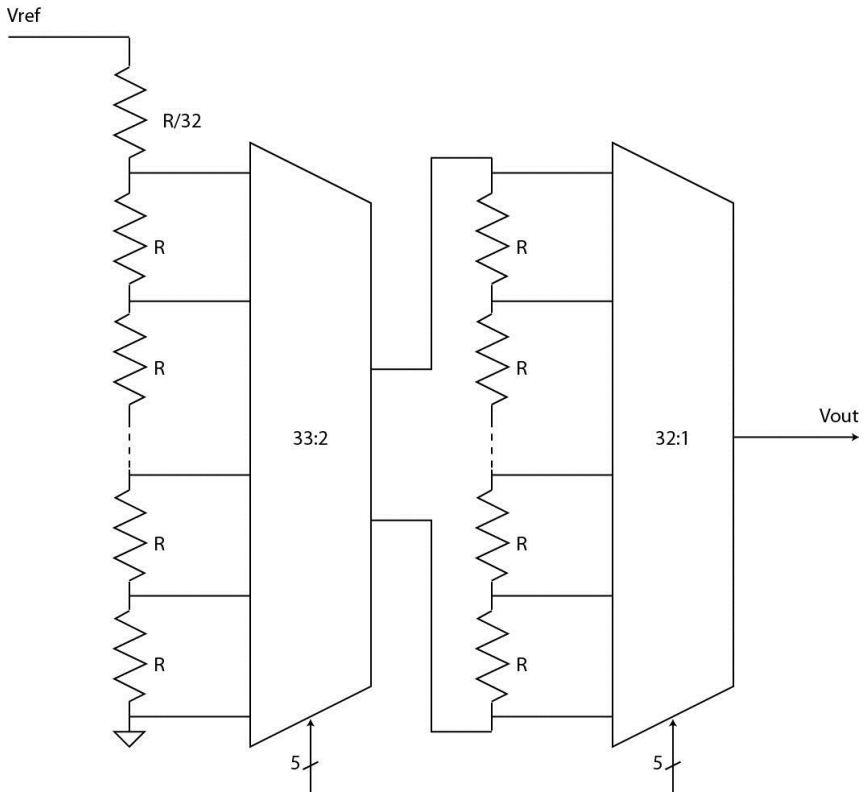
10b Voltage DAC

- Segmented resistor string design.
- Uses two 5 bit strings (64 resistors) plus correction resistor.
- Individually buffered 2.048V reference, 160µA current.
- Monotonic **if** switches are designed carefully (resistance/leakage).



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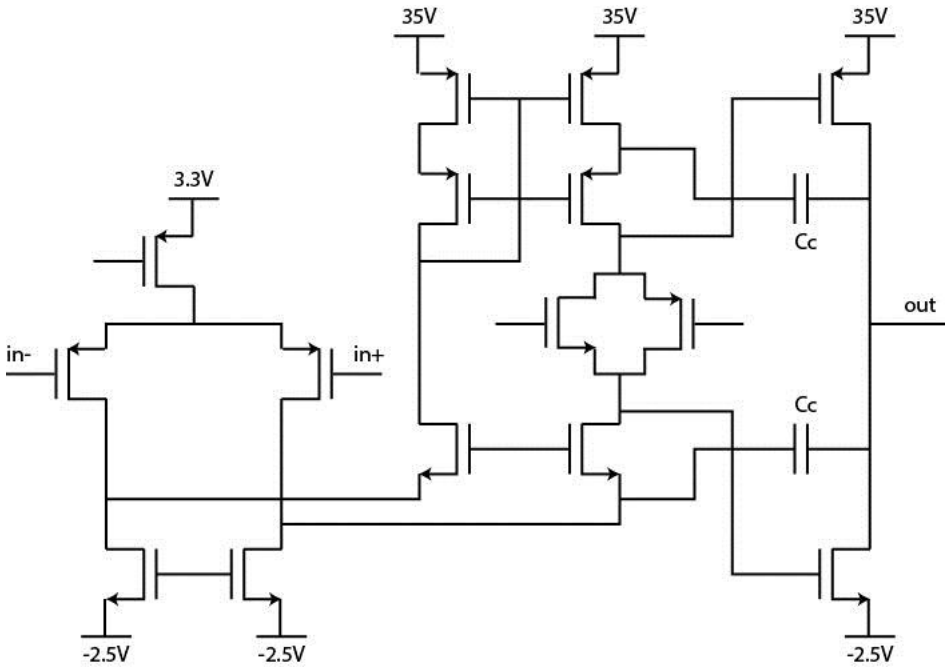
HV buffer amplifier

- Differential input class AB op-amp (Hogervorst, 1994).
- LV input stage to save power.
- Output limited to 25mA – short circuit protection.
- Resistive feedback for gain of +16.
- 25Ω series resistor for stability with high cap.
- Compensated for low bandwidth – low noise.
- Large capacitor area.



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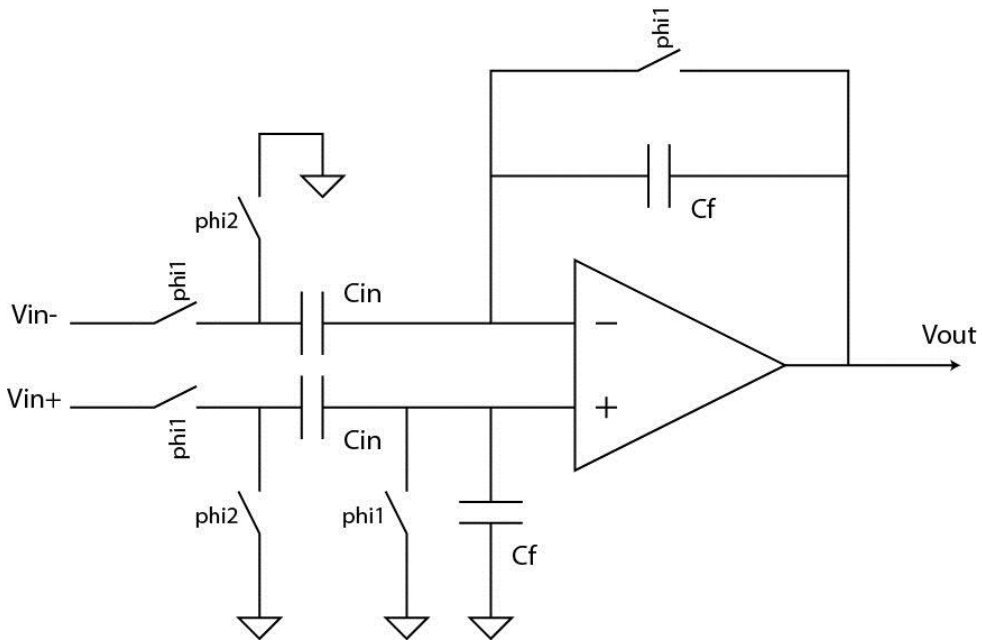
Telemetry mux & Gain amp

- Dual channel mux allows measurement of differential signals, or a single ended signal against choice of references.
- Amp provides level shifting to match ADC input range.
- Differential to single ended conversion with gain of 1 or 4.



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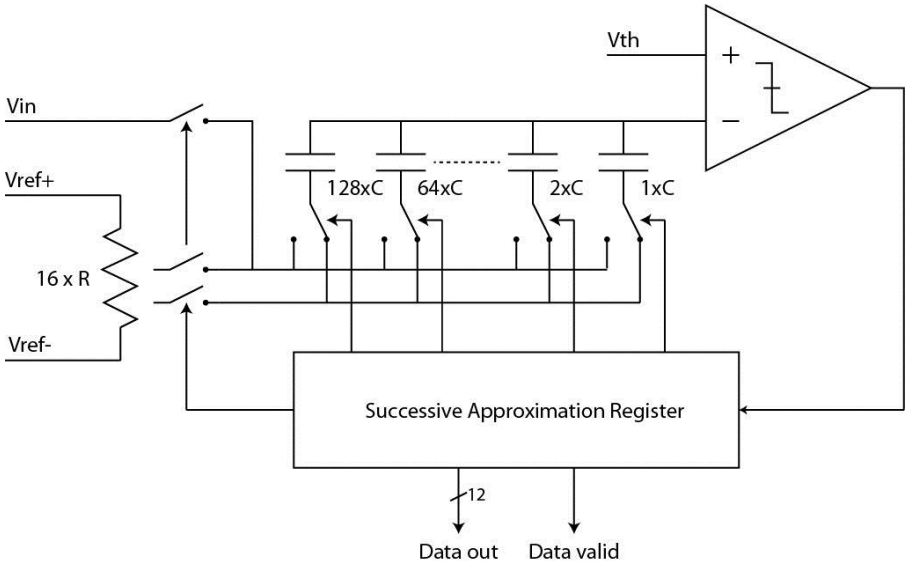
Telemetry ADC

- Single ended 12b SAR ADC.
- Pre-existing IP block.
- 0.512V – 2.560V input range.
- 4b resistor/ 8b capacitor architecture.
- 667kHz conversion rate from 10MHz clock.
- Data read back via SPI interface.



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Power

- Operates from 3.3V, 35V and -2.5V supplies.
- 35V rail can be reduced if full output swing not required.
- Each circuit & channel has power down option – only channels being used are powered.

Circuit	Current by supply			Power
	3.3V	35V	-2.5V	
Biasing	2.9mA	0.72mA	0.72mA	**36.57mW**
ADC	6.6mA			**21.78mW**
DAC (each)	0.61mA			**2.01mW**
HV output (each)	0.21mA	0.67mA	0.83mA	**26.22mW**
HV feedback resistors (each)		15.63µA/V		**546.9 µW/V**
Full 24 channels driving 32.736V, no load current	29.18mA	29.08mA	20.64mA	**1.17W**

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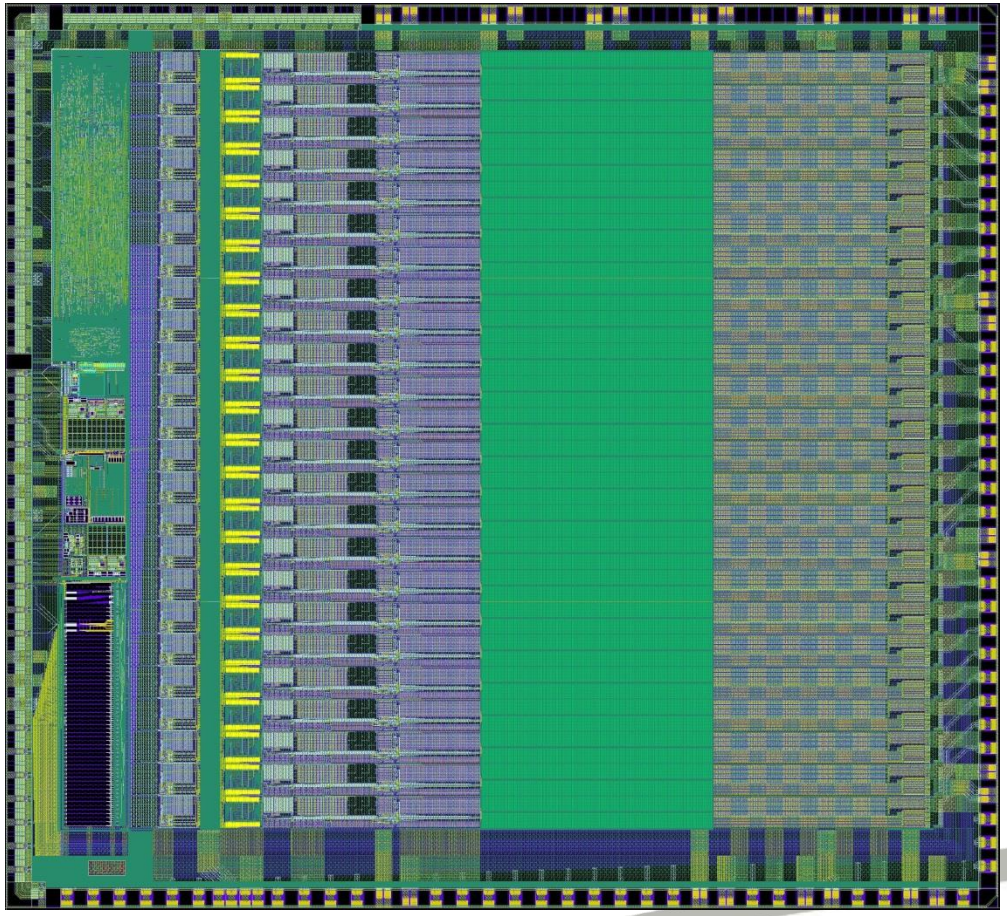
Other features

- Trimmable bandgap circuits produce all required references, only 1 external filtering capacitor needed plus supply decoupling.
- Control via SPI interface with TMR registers for SEU resistance (register refresh feature included).
- Designed with guard ringed layouts for enhanced SEL resistance.
- Implemented on AMS H35 50V 0.35µm CMOS technology, C35 variant TID tolerant to >100kRad.
- Designed for 144 pin CQFP package.

STAR Layout



13.955mm

15.125mm

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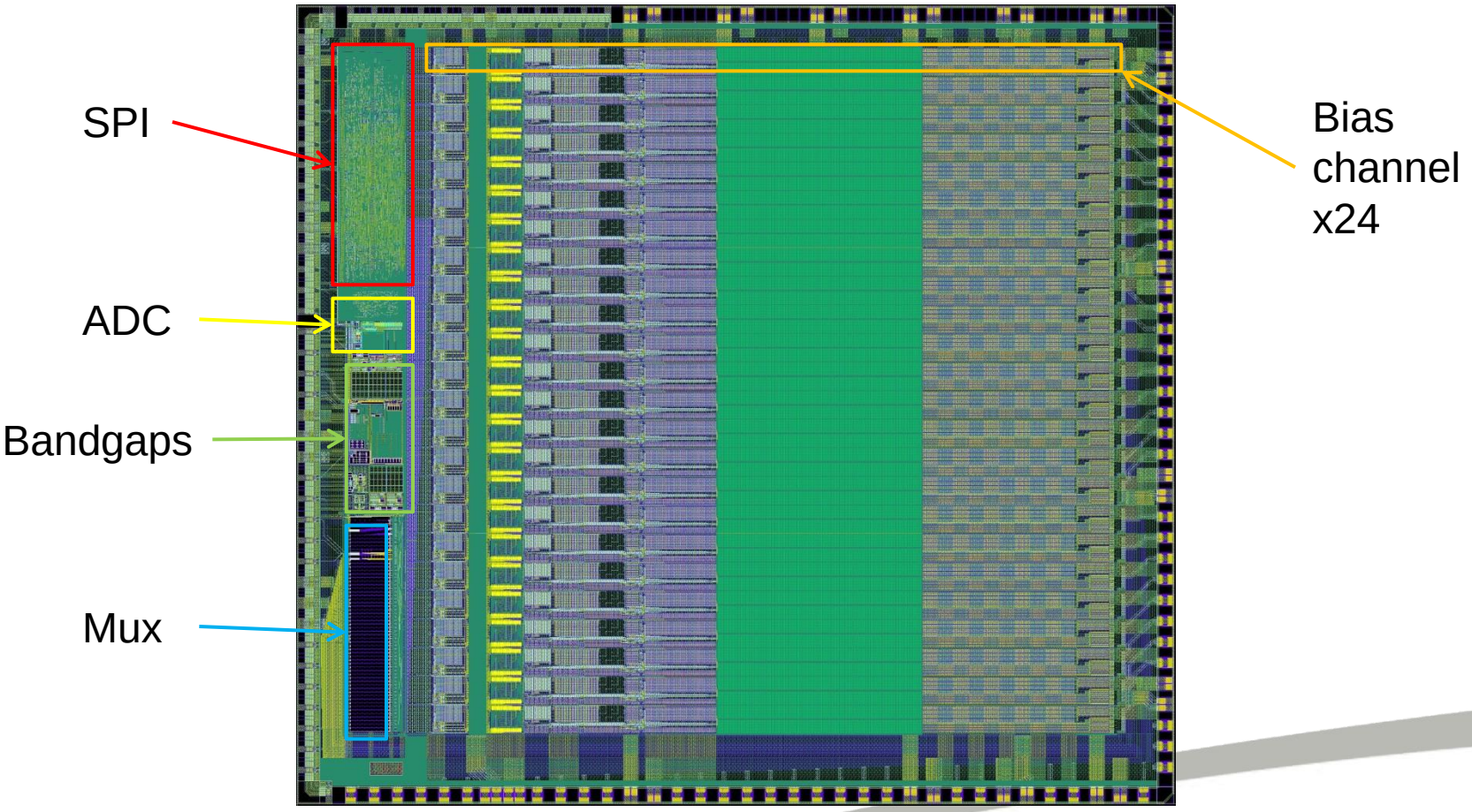
STAR Layout



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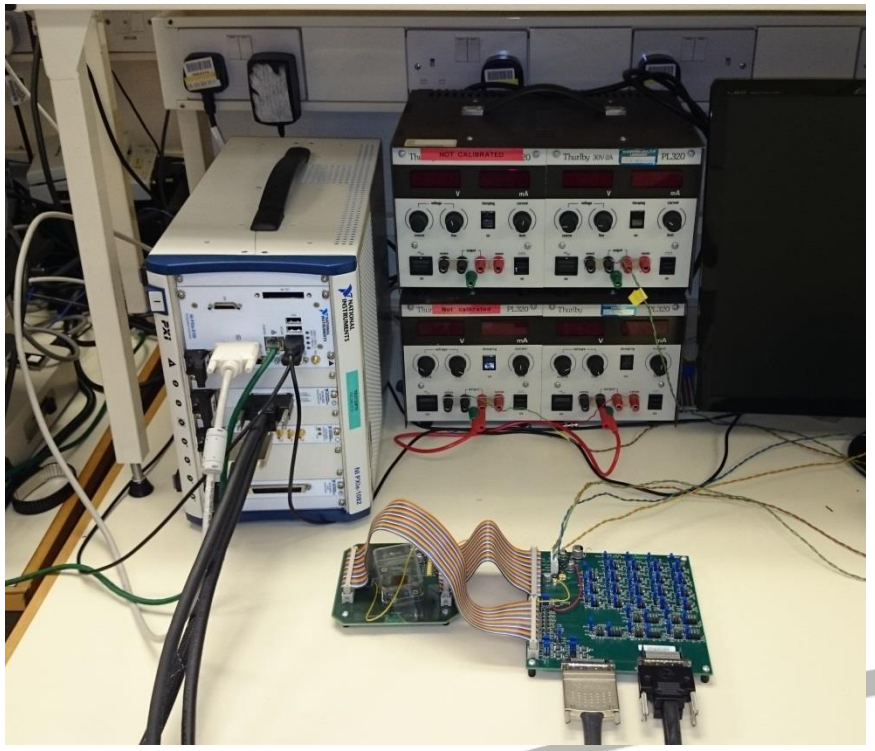
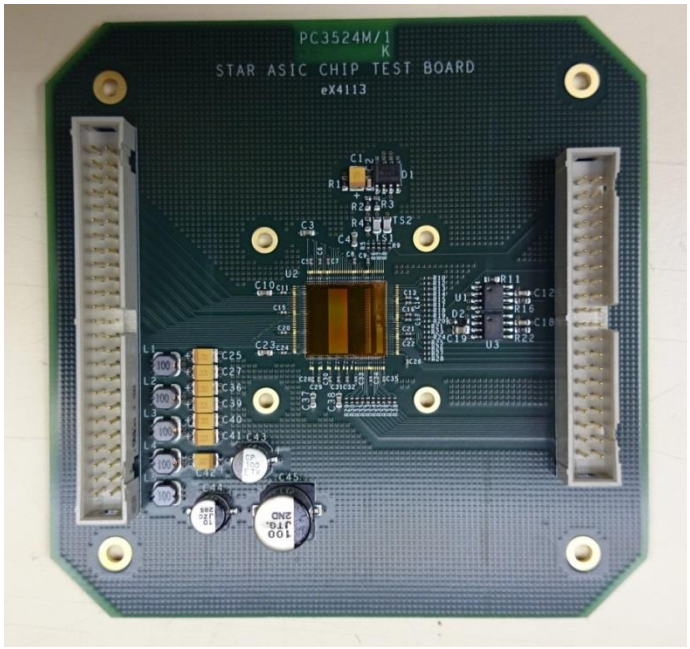
Test system

- Based on NI PXI crate with custom interface cards.





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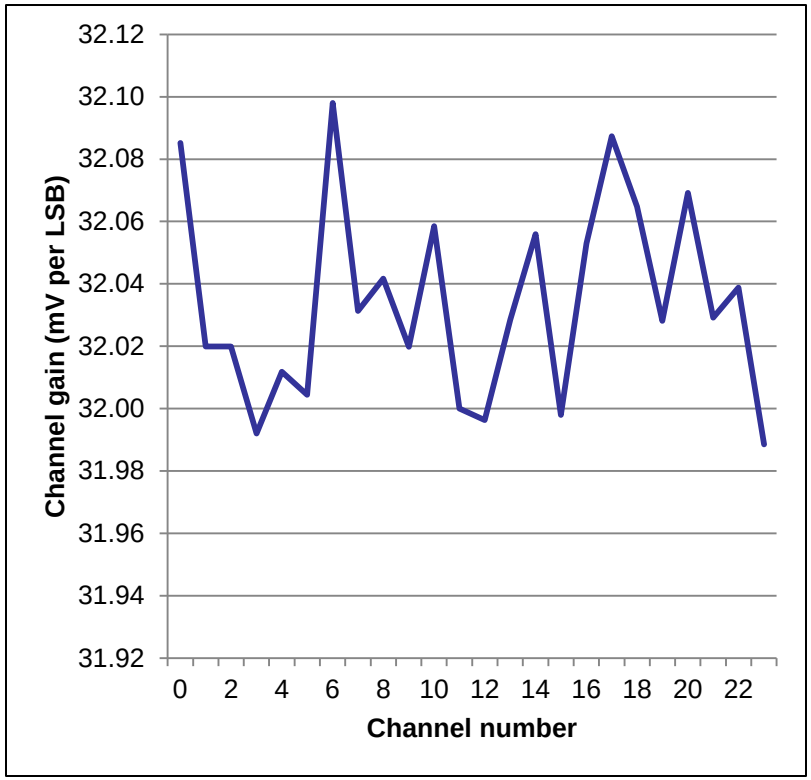
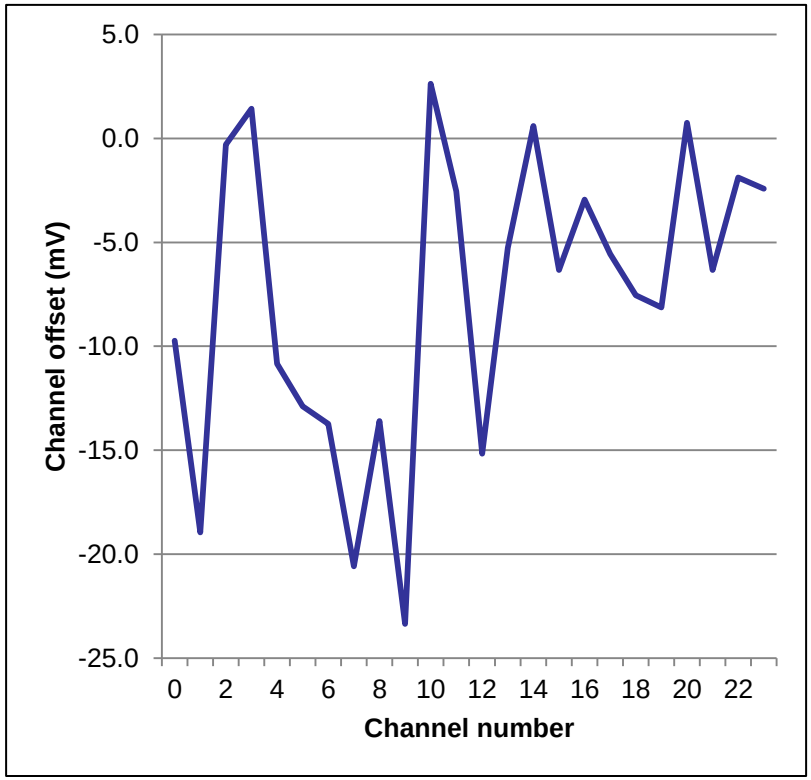
Bias output gain & offset





Worst case gain error +0.3%

Worst case offset -23mV (-0.74LSB)

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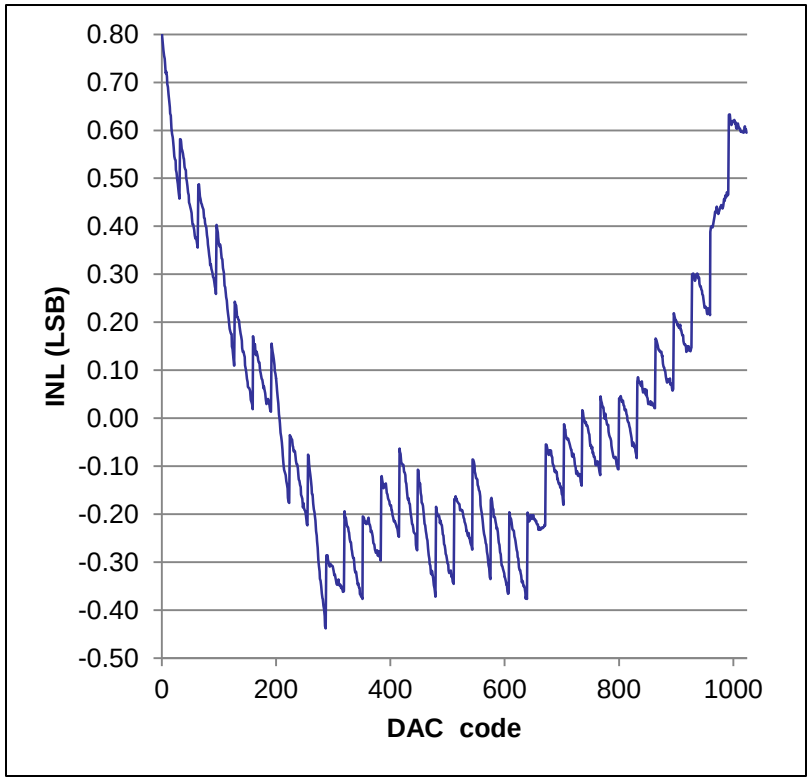
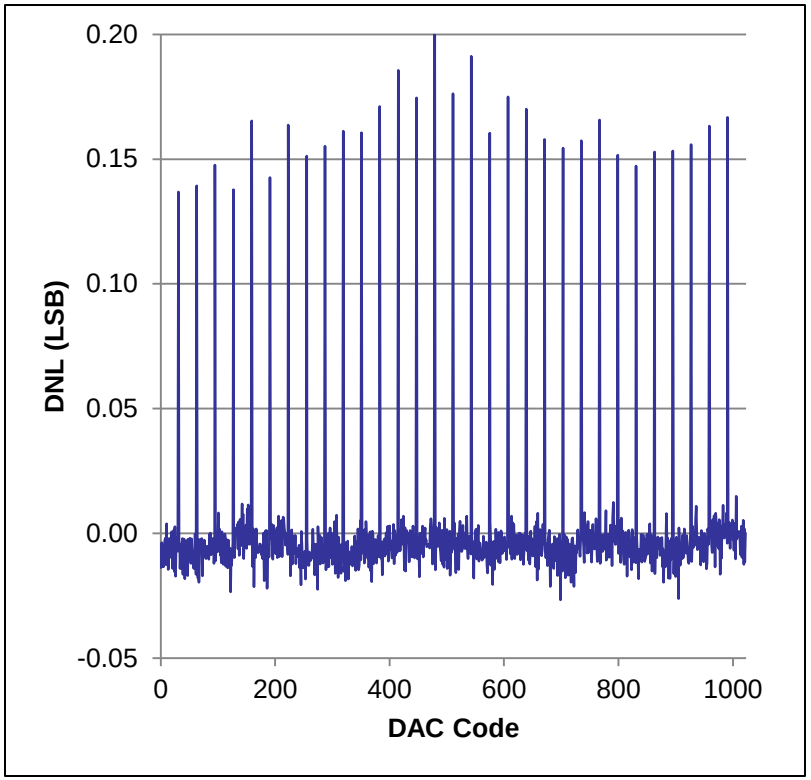
Bias output INL & DNL



Worst case INL 0.80LSB



Worst case DNL 0.20LSB

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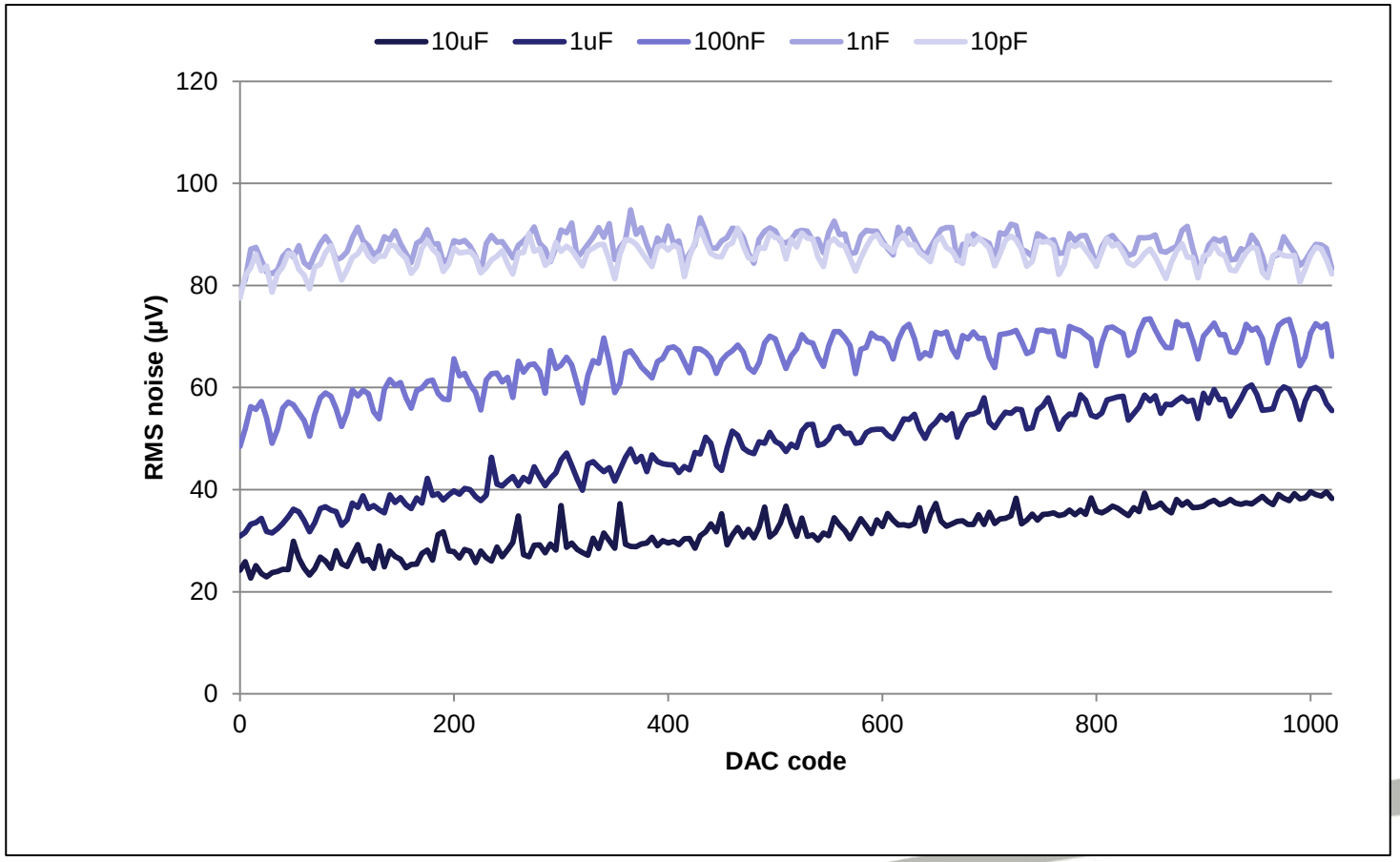
Bias output noise



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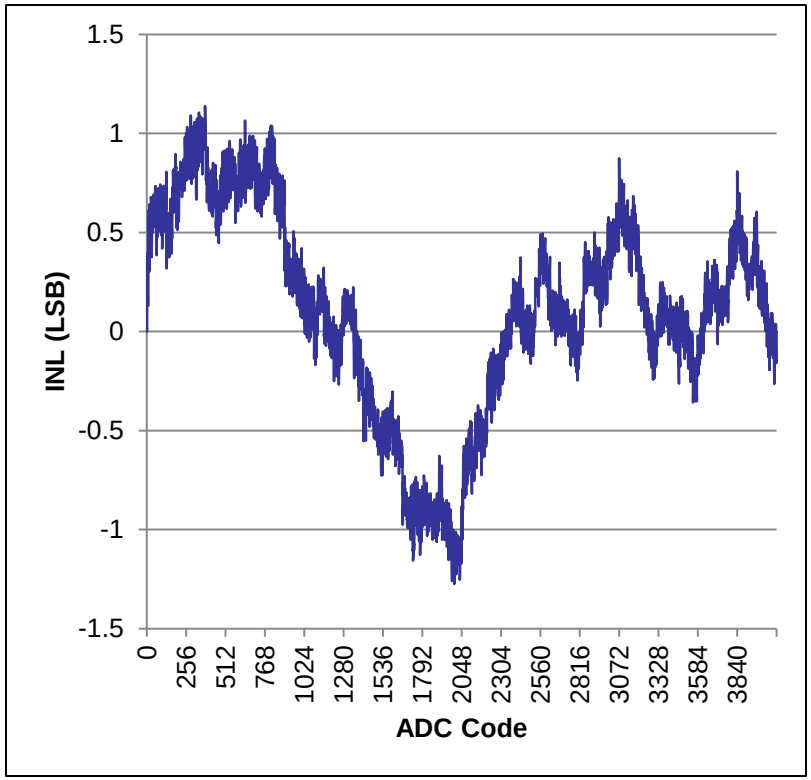
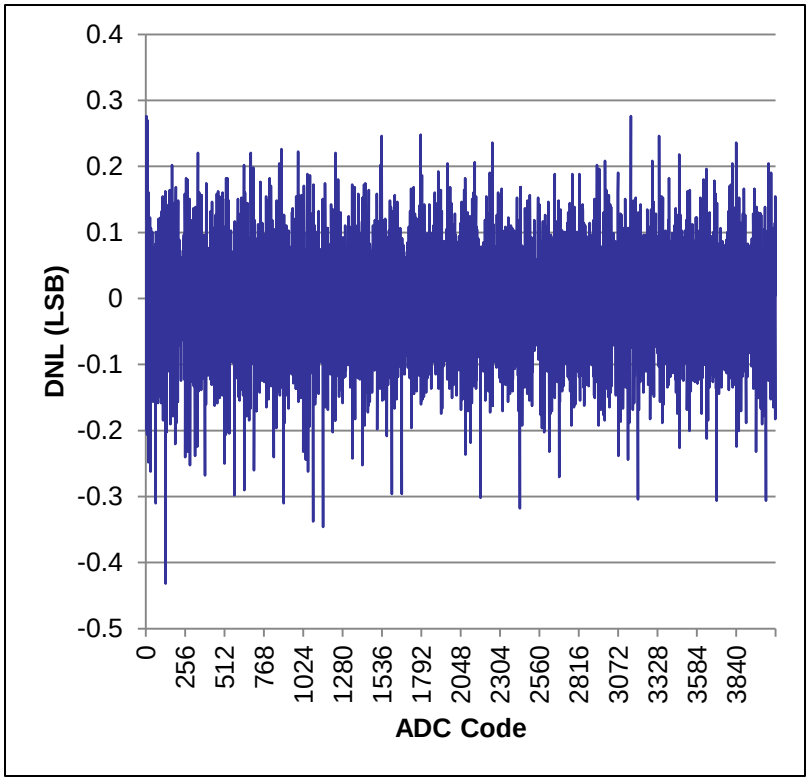
Telemetry ADC INL & DNL





Worst case INL -1.26LSB

Worst case DNL -0.43LSB

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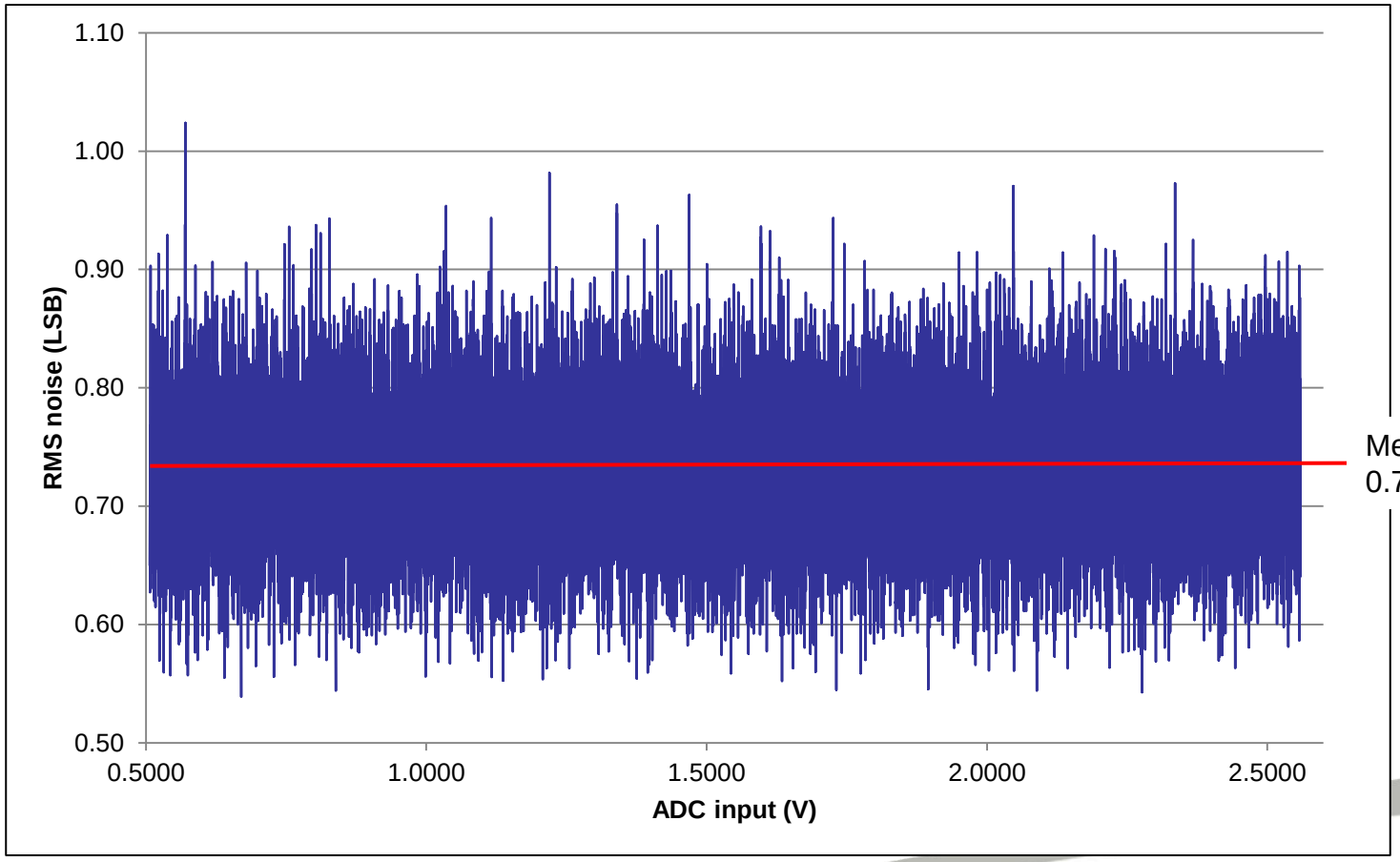
Telemetry ADC noise



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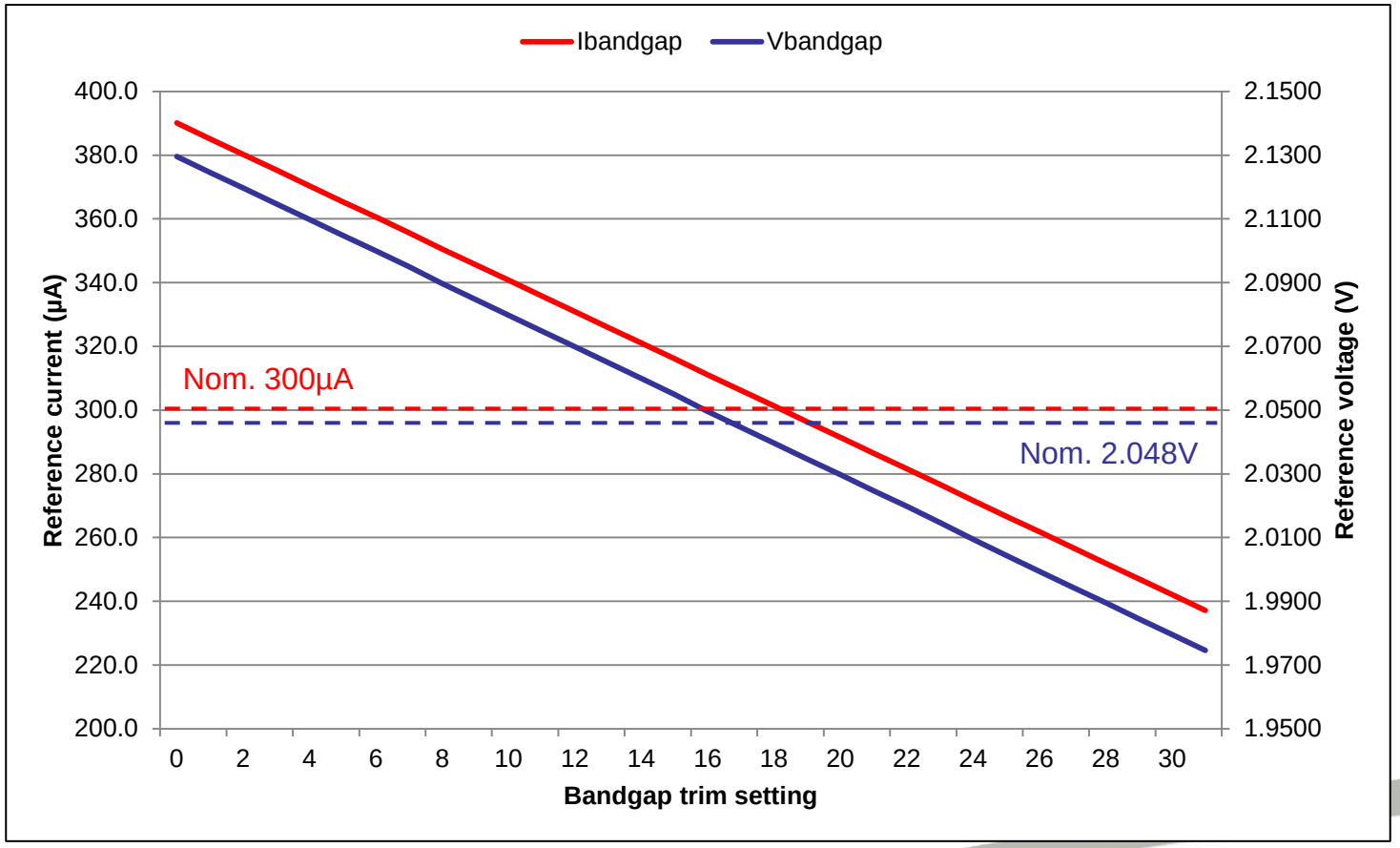
Bandgap trimming range



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Conclusions

- Complete single-chip solution for providing CCD bias voltages has been presented – the STAR ASIC.
- The STAR ASIC provides 24 independent biases of up to 32.736V with <100µV noise.
- All features working well at room temperature.
- Evaluation continuing, testing over -40°C to +125°C temperature range now underway. Radiation TID and heavy ion testing to follow.

Thank you for your attention