A Complete Space Based CCD Biasing Solution in a 0.35µm High Voltage CMOS ASIC

Q. Morrissey[a], N. Waltham[a], S. Bell[a], M. Prydderch[a], M. Torbet[a], M. Clapp[a]

[a]STFC Rutherford Appleton Laboratory, Harwell Oxford, Dicot, OX11 0QX, United Kingdom

Quentin.Morrissey@stfc.ac.uk

Abstract

An ASIC designed to fulfil the role of a general purpose bias voltage generator for CCDs in space based camera systems is presented. The STAR (Space Telemetry And Reference) chip has been developed to reduce both the size and power consumption of the circuitry required to bias a science grade CCD. Implemented in a 0.35µm 50V tolerant CMOS process, STAR provides 24 independent voltage outputs with a 32V range and noise of <100µV. Each output channel features a 10-bit DAC and a high voltage output buffer to provide current drive of up to 20mA. The output buffer can drive loads of 1KΩ / 10µF, and also includes output current limiting for short circuit protection.

An on-board telemetry system featuring a 12-bit ADC and programmable gain buffer allows measurement of the output voltages from the chip as well as up to 32 single ended and 4 differential external voltages. Control of the ASIC is via an SPI interface and all required voltages and currents are generated from internal bandgap circuits. Layout of the circuits uses established radiation hardening techniques with the intent that the circuit be SEL (Single Event Latchup) immune by design. Designed for encapsulation in a 144 pin package the STAR ASIC replaces an entire PCB of discrete electronics in current camera electronic systems.

Details of the chip architecture and circuit design will be presented, along with simulated performance and test results.

I. Introduction

At present the vast majority of space based optical wavelength camera systems use CCDs at their focal plane, particularly for scientific instruments requiring high quality images with minimal noise. These devices often operate at higher voltages falling outside the range of standard ASICs or FPGAs. Discrete drive circuits are therefore needed to reach the required signal levels. However these circuits bring with them associated issues of increased power consumption, PCB area and instrument mass. Finding suitable space qualified parts for these circuits is also an ever-present problem for the designer. Figure 1 shows the camera electronics box supplied by STFC Rutherford Appleton Laboratory for the HMI and AIA instruments on NASA's Solar Dynamics Observatory [1]. In this already compact system one of four PCBs used for operating the attached CCD (the second card from the top in figure 1) is entirely devoted to discrete circuits generating bias voltages.

In this paper a high voltage mixed signal ASIC is described which has been developed to address this problem. The STAR (Space Telemetry And Reference) ASIC integrates all the circuitry required for generating programmable biases of up to 32V with on-chip references and a housekeeping telemetry system in a single die. The device requires only appropriate power supplies with decoupling, a single noise filtering capacitor, and a digital serial interface to operate, making it a simple and highly compact alternative to traditional discrete biasing solutions. The device is designed to replace the entire biasing PCB required for systems such as the electronics box in figure 1.

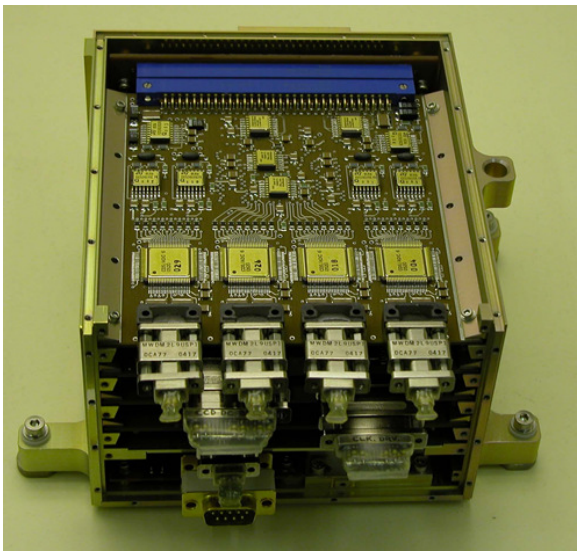

Figure 1: Camera electronics box from the HMI & AIA instruments on NASA Solar Dynamics Observatory. The CCD biasing circuitry occupies one of the lower circuit boards.

The paper will be arranged as follows: section II will describe the architecture of the STAR ASIC and provide details of its sub-blocks, section III contains test results from the prototype devices, and section IV discusses conclusions and future work.

II. ASIC Architecture

The STAR ASIC provides 24 independently controllable, low noise bias voltages with an output range of 0-32.736V and a current drive capability of +/-20mA, plus a short circuit current limit of +/-25mA. Each output can drive resistive loads as low as 1kΩ and provide stable operation with load capacitances from 10pF up to 10µF to allow for loading from the CCD and cable harness plus noise filtering. The telemetry system allows monitoring of the generated voltages, plus point-of-load external connections, differential temperature monitors, and general purpose uncommitted inputs. Control of the system is via a simple digital SPI interface operating at standard 3.3V CMOS logic levels. All required bias voltages and currents are generated on-chip, and no additional active

circuitry should be required to operate the chip. The low voltage portions of the chip operate on a 3.3V supply while the output buffers in each channel require high voltage supplies, nominally 35V and -2.5V. The device is designed to operate across a military temperature range (-40°C to 125°C) and be resistant to radiation Total Ionising Dose (TID) up to at least 100kRad and Single Event Effects (SEE) such as upset or latchup. A functional block diagram of the circuit is shown in figure 2.

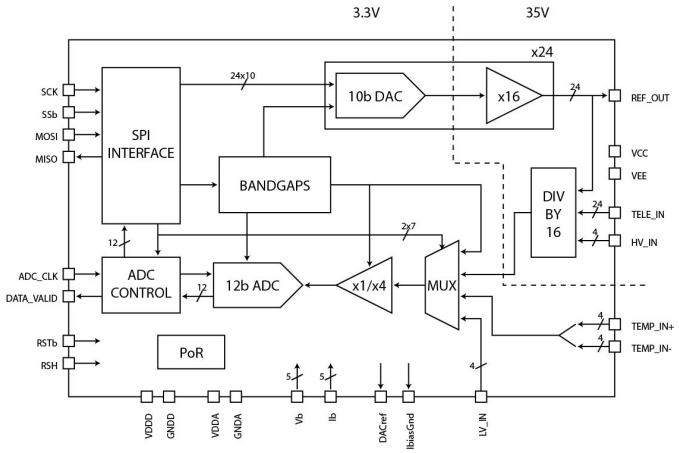

Figure 2**:** Functional block diagram of the STAR ASIC.

A. High voltage output channels

Control of the output bias voltages is achieved using 10 bit segmented resistor string DACs [2] in each channel. Each DAC is provided with an individually buffered 2.048V reference voltage taken from a master DAC reference produced by the voltage bandgap circuit. This gives an output range of 0-2.046V in 2mV steps. The structure of the DAC using two 5-bit stages is shown in figure 3.

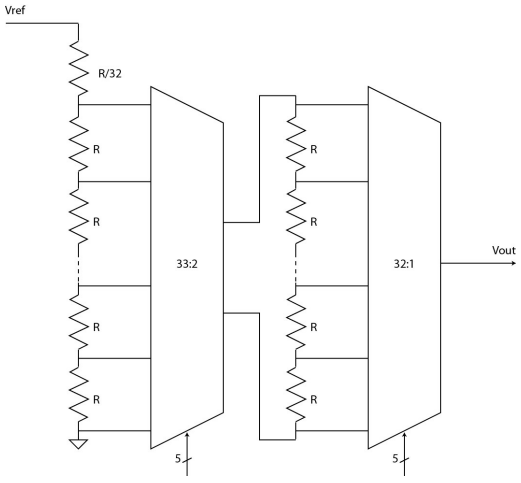

Figure 3**:** Schematic showing the segmented resistor string DAC.

An amplifier with a gain of 16, realised with a high voltage class AB differential input op-amp, is then used to boost the output voltage to the required 32V output level. The amplifier (shown in figure 4) is constructed using a PMOS input folded cascade first stage and a class AB second stage with cascoded compensation and floating control cell [3]. To save power the input tail current source is run on the low voltage 3.3V power supplies, while the rest of the circuit runs on the high voltage supplies. The amplifier power consumption is 22.7mW running on 35V and -2.5V supplies and can source or sink up to 20mA into a 1kΩ while maintaining amplifier accuracy to 10b. Current mirrors inserted in series with the op-amp output stage (not shown in figure 4) limit the output current to +/-25mA, to prevent damage to the chip in case of a short circuit in one of the load components. Since the amplifier is designed to provide DC bias voltages it is compensated to provide a low small signal bandwidth of approximately 60kHz for noise reduction. The amplifier has an output slew rate of 0.55V/µs giving a full power bandwidth of 5.3kHz.

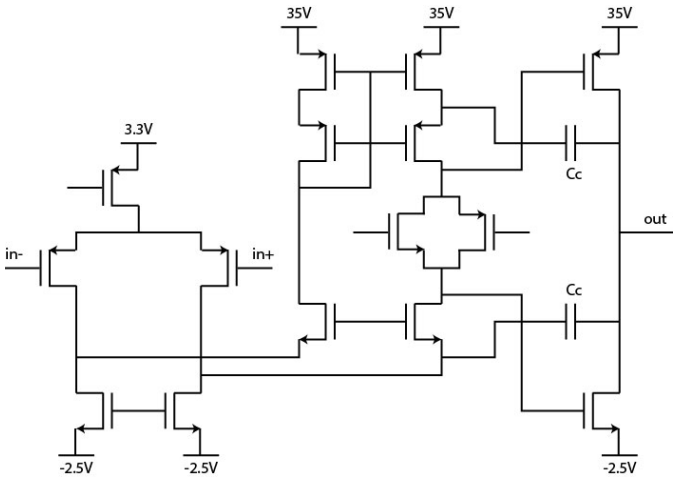

Figure 4: Schematic of the high voltage buffer amplifier.

The op-amp is used in a resistive feedback non-inverting configuration as shown in figure 5, with a gain set to 16 (Rg = 4kΩ, Rf = 60kΩ). A signal dependant current of up to 512µA therefore flows through Rf and Rg. The resulting circuit in conjunction with the DAC has an output range of 0 - 32.736V with a resolution of 32mV. To help ensure amplifier stability across the full 10pF – 10µF range of capacitive loads a series output resistor (Rs) of 25Ω is included to enhance the amplifier phase margin.

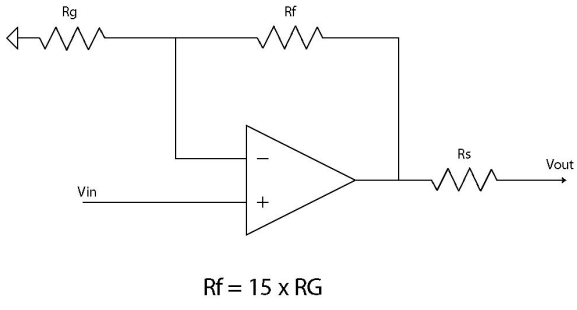

Figure 5**:** Feedback arrangement of the high voltage output buffer.

B. Telemetry system

The telemetry system incorporated into STAR is designed to allow monitoring of the 24 output bias voltages plus all voltages generated on-chip. External inputs for point-of-load monitoring of the biases are provided, or for measurement of other system voltages. An additional 8 uncommitted inputs

are also available for this purpose (four low voltage inputs and 4 high voltage inputs). Finally four pairs of differential inputs allow PRT bridge circuits to be connected for temperature monitoring.

The system is constructed from a twin channel analogue multiplexer, a differential input variable gain amplifier, and a 12 bit Successive Approximation Register (SAR) ADC. The multiplexer includes 16:1 resistive dividers on its inputs where appropriate for scaling high voltage signals to match the 2.048V input range of the ADC. The two independently controllable paths through the multiplexer facilitate either differential inputs, or measurement of an input against a selectable internal or externally provided reference.

The variable gain amplifier is used to buffer the multiplexer signals and drive the ADC input capacitance. It is implemented as a switched capacitor amplifier circuit with a selectable gain of 1 or 4 to allow amplification of smaller signals, and also performs the necessary level shifting to match the single ended output to the input range of the ADC. The architecture is shown in figure 6. Operation of the buffer is tied to that of the ADC, with switches phi1 being closed while the ADC is idle or converting, and switches phi2 only being closed when the ADC samples an input. This means the inputs are sampled during the reset phase of the amplifier and allows the voltages on Cin a longer period settle, reducing the bandwidth requirements through the multiplexer.

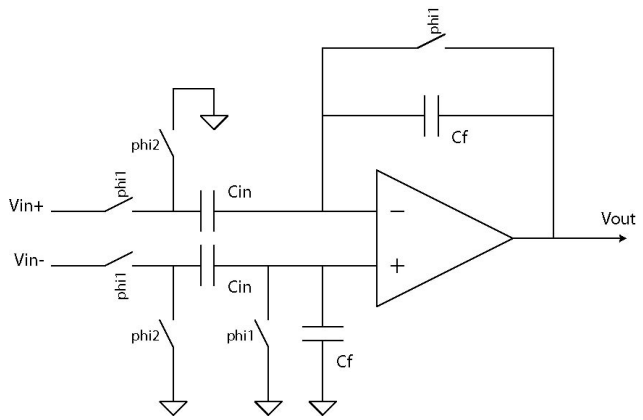

Figure 6: Variable gain multiplexer buffer architecture

The ADC itself uses a single ended 4 bit resistor string / 8 bit capacitor array architecture with a 2.048V input range between 0.512V and 2.560V, operating at up to 667kSPS with a 10MHz clock. Control of the ADC is via dedicated clock and sample signals taken from external inputs, with an external data valid signal indicating when data is available for retrieval via the SPI interface.

C. Digital interface

Control of all the ASICs remaining functions and setting is via a 3 or 4 wire SPI serial interface operating on standard 3.3V CMOS logic levels. This is used to access an internal register bank controlling chip functions, which is implemented with Triple Module Redundancy (TMR) to provide protection from Single Event Upsets (SEU). A dedicated 'refresh' signal is included in the design to update any registers affected by a Single Event Upset (SEU) with corrected data from its TMR voting circuit when the SPI clock is not running. ADC conversion data is also accessed from a read only location in the memory map of the SPI interface. The SPI interface uses a 16 bit word length and supports burst mode read and write operations.

D. Reference voltages and currents

The required reference voltage and currents on the STAR ASIC are generated from a pair of on-chip bandgap reference circuits based on the low voltage architecture detailed in [4]. Each bandgap includes a 5 bit current mirror DAC at its output to allow for trimming out of errors due to process variations. The voltage bandgap circuit provides a range of voltages used in the telemetry system and the master DAC reference voltage. The current bandgap produces a single reference used to set bias currents in all the circuit amplifiers and output current limiters. A power-on reset circuit is also included to ensure correct known operating conditions after power-up.

E. Process and layout

Due to its intended application the STAR ASIC will be exposed to the radiation environment of space. For this reason the H35 2 poly 4 metal 50V 0.35µm CMOS process from AMS was chosen for the fabrication of the STAR ASIC due to the availability of 50V tolerant transistors and the suitability of the process for use in radiation environments with relevant layout techniques [5, 6]. Guard banding was applied to all elements of the layout to provide enhanced protection from SEL. The completed STAR die size is 15.125mm x 13.955mm, the layout is shown in figure 7.

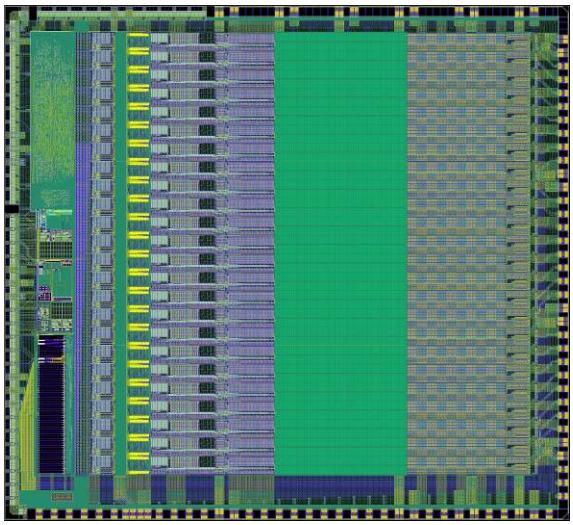

Figure 7: Layout of the STAR ASIC

F. Power dissipation

Each circuit on the ASIC (with the exception of the bandgaps, some biasing circuits, and the power on reset) has a power down mode to enable unused circuits and channels to be disabled if not required and save power. The ASIC powers up in the minimum power state with only the bandgaps and basic biasing circuitry active. The telemetry circuits and ADC, channel DACs, and HV output buffers can then be enabled individually. The minimum power dissipation of the circuit at power on is 36.57mW, and maximum with all circuits activate and outputs driving 32.736V is 1.17W. A

breakdown of current and power consumption by power supply and circuit element is shown in table 1.

Table 1: Current and power consumption by circuit element and power supply.

Circuit	Current by supply (A)			Power (W)
	3.3V	35V	-2.5V	
Biasing	2.9m	0.72m	0.72m	36.57m
ADC	6.6m			21.78m
DAC (each)	0.61m			2.01m
HV output (each)	0.21m	0.67m	0.83m	26.22m
HV feedback resistors (each)		15.63µ/V		546.9 µ/V
Full 24 channels driving 32.736V, no load current	29.18m	29.08m	20.64m	1.17

III. Results

A. *Test system*

The completed design of the STAR ASIC has been fabricated and the unpackaged die mounted on a carrier PCB for evaluation (shown in figure 8). Testing was carried out using a National Instruments PXI crate to provide analogue and digital stimulus and measure the analogue outputs from the ASIC. An interface PCB was used for signal multiplexing, cable connections, and to implement load circuits for the bias outputs. Each output was connected to selectable load resistors of 680Ω, 1.5kΩ or 15kΩ connected to the positive or negative high voltage supplies to control load current. A 4MΩ resistive divider to ground, feeding the output to the NI ADC card, was present on all outputs. All but five of the outputs were connected to a fixed 1nF capacitor. The five remaining channels (0, 5, 11, 17, and 23) had selectable capacitive loads of 10pF, 1nF, 100nF, 1µF or 10µF to investigate output stability and noise filtering. A high pass RC filter on these channels was used to remove the DC component of the outputs before high resolution noise measurement. Tests were carried at 22°C with a low voltage supply at 3.3V and high voltage supplies of +35V and either -2.5V or -5V.

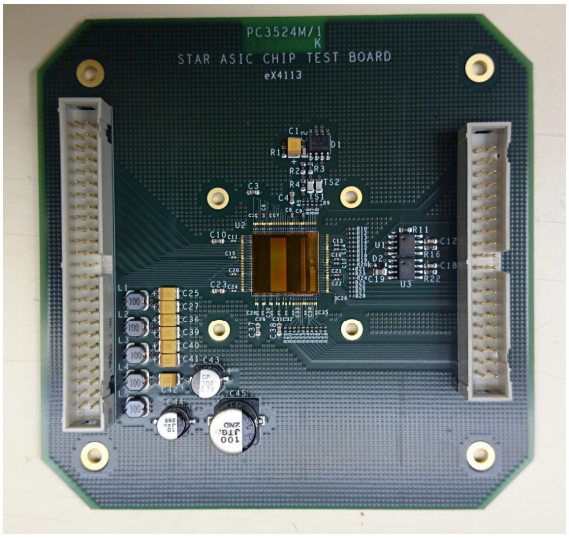

Figure 8: Prototype STAR ASIC bonded to a carrier PCB.

B. *HV outputs*

Testing of the high voltage bias outputs was conducted for the full range of resistive and capacitive loads on each output, representing the range of likely operating conditions for the device. The outputs were found to be stable for all capacitive loads up to 10µF. Gain and offset measurements were taken for all channels in an unloaded state (only the 4MΩ resistive divider to ground connected), the results being shown in figures 9 and 10. In all cases it can be seen that the gain is accurate to <0.3% and the zero offset measured is less than 1LSB (32mV). All channels were demonstrated to be monotonic with the worst case channel DNL and INL measurements shown in figure 11 and figure 12 respectively. The transitions between sub-ranges in the DACs give rise to the saw-tooth pattern in the INL plot and spikes in the DNL plot.

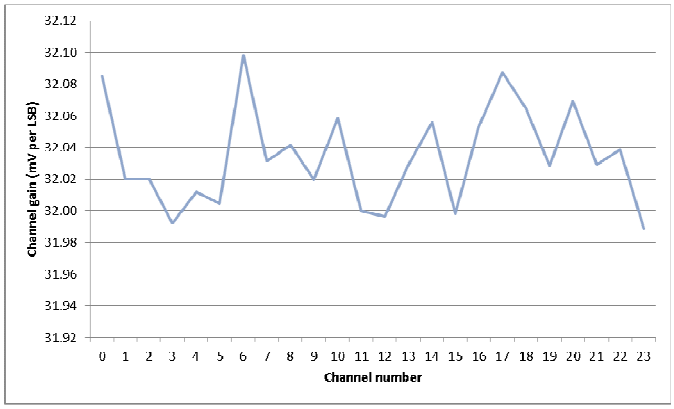

Figure 9: High voltage output gain by channel calculated from least-square straight line fit, nominally 32mV/LSB (4MΩ load to ground).

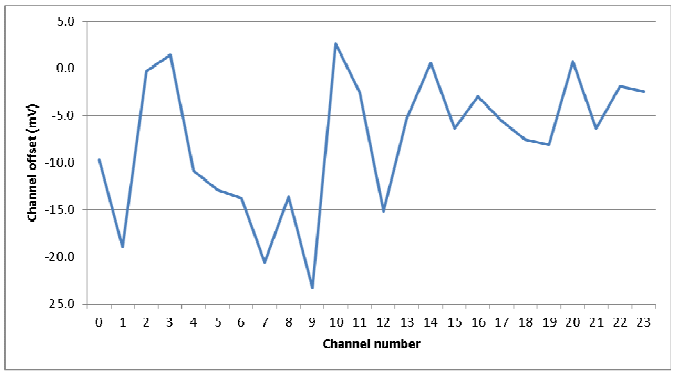

Figure 10: High voltage output offset by channel, calculated from least-square straight line fit (4MΩ load to ground).

Measurements of noise were carried out as a function of output voltage and load capacitance for each of the 5 channels with selectable capacitors. The results from a representative channel are shown in figure 13. At low load capacitances the noise is dominated by thermal noise from the output amplifier and feedback resistors. At higher loads noise from the DAC reference buffer and DAC resistance become significant giving a slope proportional to DAC code. The ripple seen in the plots is the result of the changing equivalent resistance of the channel DAC as it moves through sub-ranges.

Short circuit current limits for all channels were tested and confirmed to be 25mA +/- 5% in all cases.

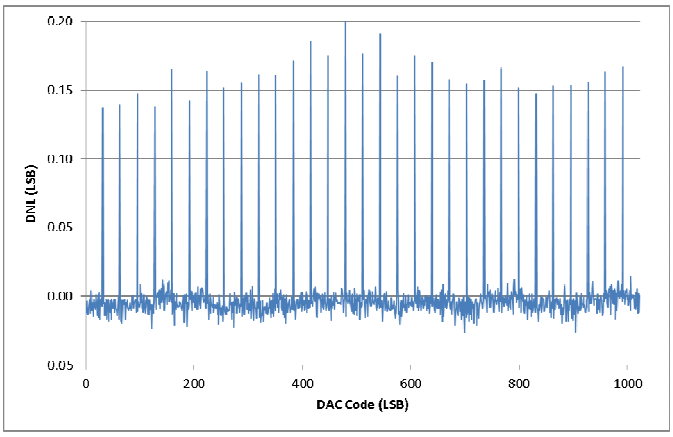

Figure 11: High voltage output DNL measurement of worst case high voltage channel output (channel 9, 4MΩ load to ground).

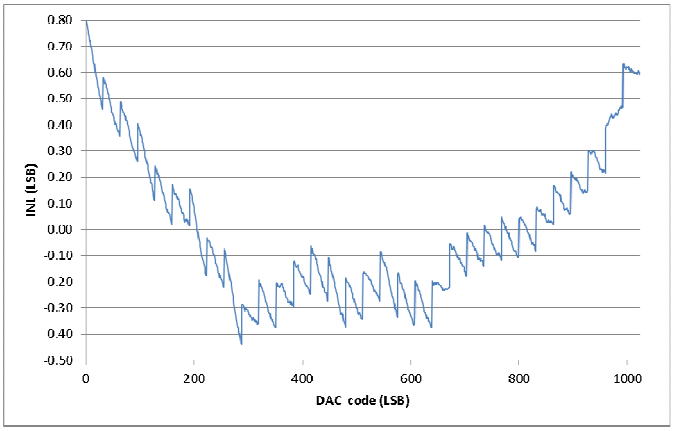

Figure 12: High voltage output INL measurement of worst case high voltage channel output (channel 8, 15kΩ load to -2.5V).

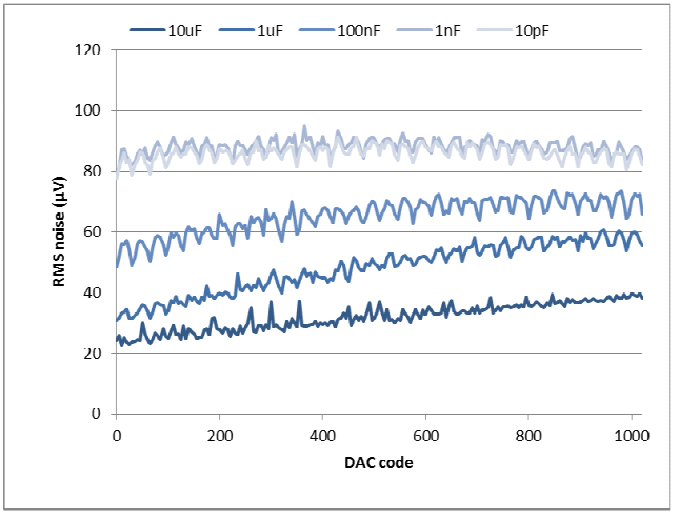

Figure 13: High voltage output noise as a function of DAC setting for a variety of load capacitances, (channel 11, 15kΩ load to +35V).

C. *ADC & Telemetry system*

The telemetry system and ADC were tested using a DAC outputs from the NI crate via one of the uncommitted inputs to the telemetry system. The test signal was then swept across the native 0.512V – 2.560V range of the ADC against the internal ADC mid-range reference voltage of 1.536V. The multiplexer gain buffer was set to 1 for these tests. The DNL and INL of the telemetry ADC are shown in figures 14 and 15 respectively. The telemetry system as a whole showed an INL of -1.26 LSB and a DNL of -0.43 LSB. The measured noise of the telemetry system as a function of input voltage is shown in figure 16. The mean measured noise was 0.73 LSB.

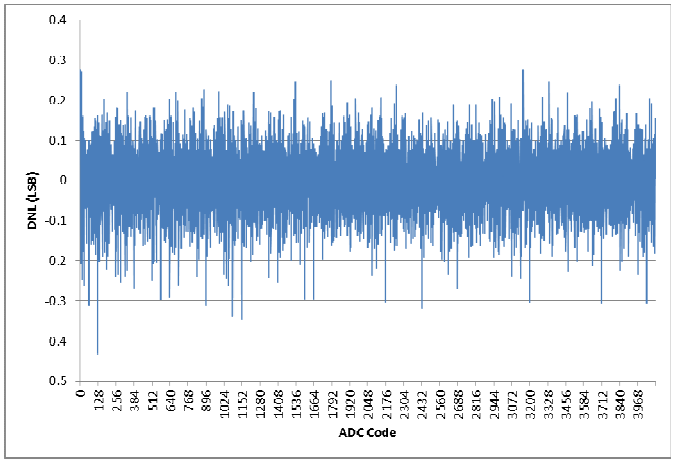

Figure 14: Telemetry ADC DNL measurement for a mux buffer gain of 1.

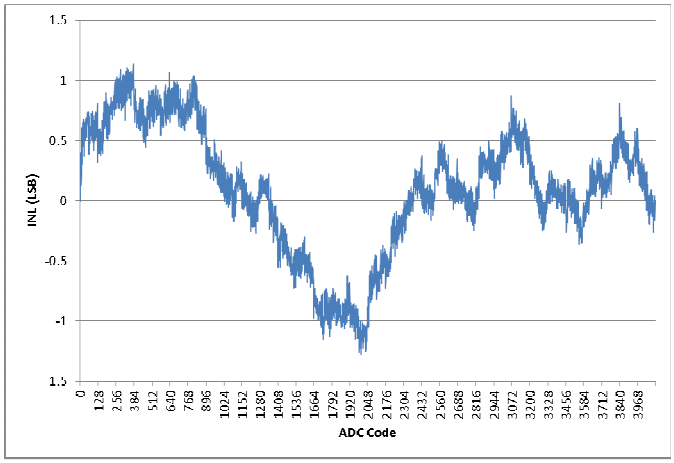

Figure 15: Telemetry ADC INL measurement for a mux buffer gain of 1.

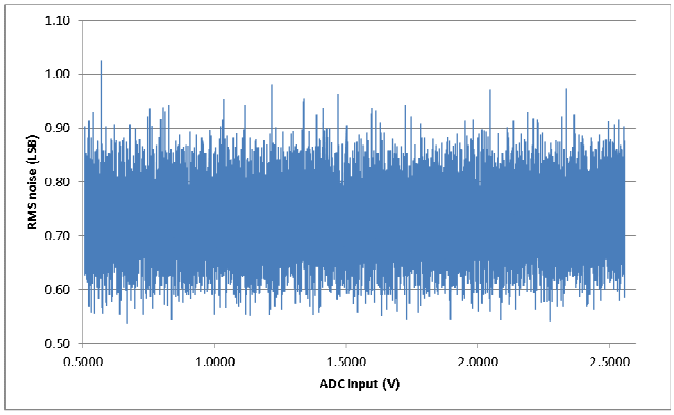

Figure 16: Telemetry ADC noise as a function of input voltage for a mux buffer gain of 1.

D. *Reference voltage and current*

The bandgap circuit output voltages and currents were measured at a fixed temperature of 22°C. The current and voltage references were tested across the range of possible trim settings for each, the results being shown in figure 17. For both circuits the range of trimming adjustment was found to be sufficient to reach the nominal outputs for each circuit, being 2.048V and 300µA.

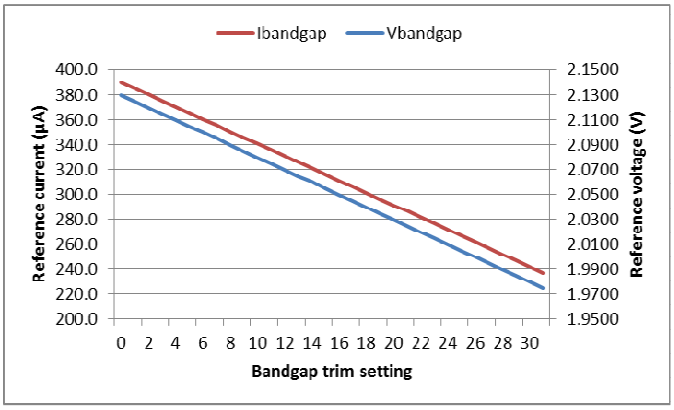

Figure 17: Bandgap outputs as a function of trim settings, showing the nominal settings of 300µA and 2.048V are within the trim range of both circuits.

E. *SPI Interface*

The SPI serial interface and register bank were tested at a range of speeds and were found to be error free up to bit rates of 50MHz, the maximum speed of the digital I/O card being used.

F. *Power*

Power dissipation for the main circuits was measured from the power supplies as the individual elements were enabled. Due to other test circuitry sharing the supplies it was not possible to accurately determine the current drawn by the ASIC at power up. However the current draw from other circuit elements was measured and the results are shown in table 2. These can be seen to be in broad agreement with the predicted values listed in table 1.

Table 2: Measured current and power consumption by circuit element and power supply.

Circuit	Current by supply (A)			Power (W)
	3.3V	35V	-2.5V	
ADC	7m			21.78m
DAC (each)	0.6m			2.01m
HV output (each)	0.2m	0.7m	0.8m	26.22m

IV. Conclusions

A high voltage mixed signal ASIC for the generation of CCD bias voltages has been presented. The device has been fabricated in a commercial 50V 0.35µm CMOS technology and prototype die tested. Results show the device performs well, providing low bandwidth output biases on a 0 – 32.736V range with less than 100µV of noise which can be reduced further through the use of filtering capacitors. The controlling DACs are monotonic showing good INL and DNL performance. The telemetry function was also assessed and found to have good characteristics with monotonic behaviour and DNL, INL and noise measurements of 0.43LSB, 1.26 LSB and 0.73LSB respectively. Testing across the full temperature range of -40°C to 125°C will now proceed, followed by TID and SEL radiation testing in the future.

V. References

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