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A complete space based CCD biasing solution in a 0.35µm high voltage CMOS ASIC

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An ASIC designed to fulfil the role of a general purpose bias voltage generator for CCDs in space based camera systems is presented. The STAR (Space Telemetry And Reference) chip has been developed to reduce both the size and power consumption of the circuitry required to bias a science grade CCD. Implemented in a 0.35µm 50V tolerant CMOS process, STAR provides 24 independent voltage outputs with a 32V range and a SNR of up to 120dB. Each output channel features a 10-bit DAC and a high voltage output buffer to provide current drive of up to 20mA. The output buffer can drive loads of 1KΩ / 10µF, and also includes output current limiting for short circuit protection.
An on-board telemetry system featuring a 12-bit ADC and programmable gain buffer allows measurement of the output voltages from the chip as well as up to 32 single ended and 4 differential external voltages. Control of the ASIC is via an SPI interface and all required voltages and currents are generated from internal bandgap circuits. Layout of the circuits uses established radiation hardening techniques with the intent that the circuit be SEL (Single Event Latchup) immune by design. Designed for encapsulation in a 144 pin package the STAR ASIC replaces an entire PCB of discrete electronics in current camera electronic systems.
Details of the chip architecture and circuit design will be presented, along with simulated performance and test results.

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