

# Analogue and **M**ixed-Signal **I**ntegrated **C**ircuits for **S**pace **A**pplications

AMICSA 2006

AMICSA 2008

AMICSA 2010

AMICSA 2012

**AMICSA 2014**

**Wrap – Up**

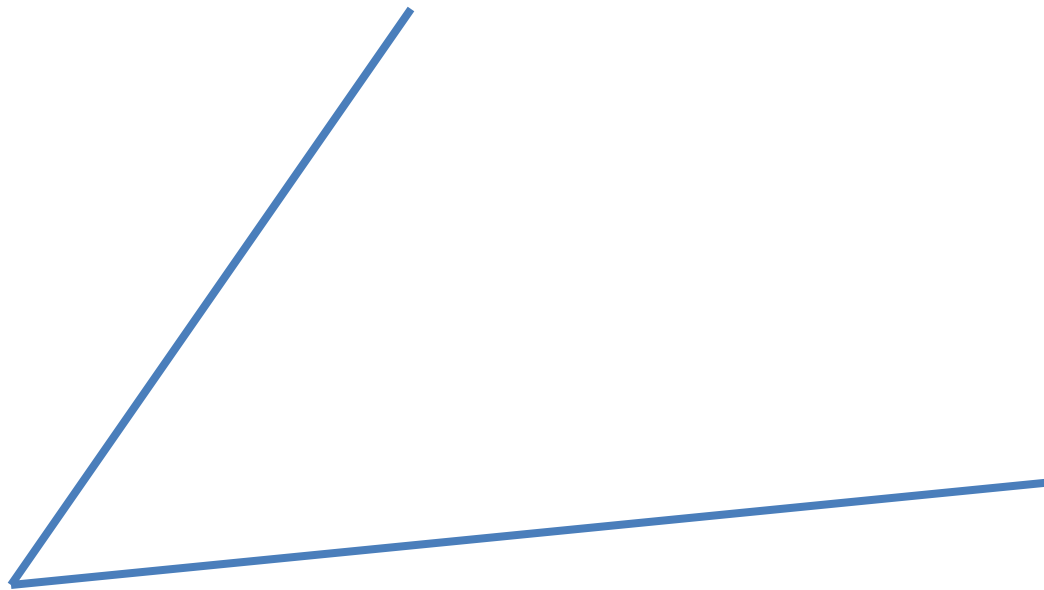
# Outline:

- intriguing discovery about AMICSA venues
- after AMICSA 2012
  - A-MS Users Round Table
  - EAMAS Working Group
- AMICSA 2014 statistics
- some conclusions
- some pictures

# AMICSA venues

**2010, 2012**  
ESTEC, Noordwijk, Netherlands

**2008**  
Sintra/Cascais  
Portugal



**2006**  
U. Thrace  
Ξάνθη (Xanthi)  
Greece

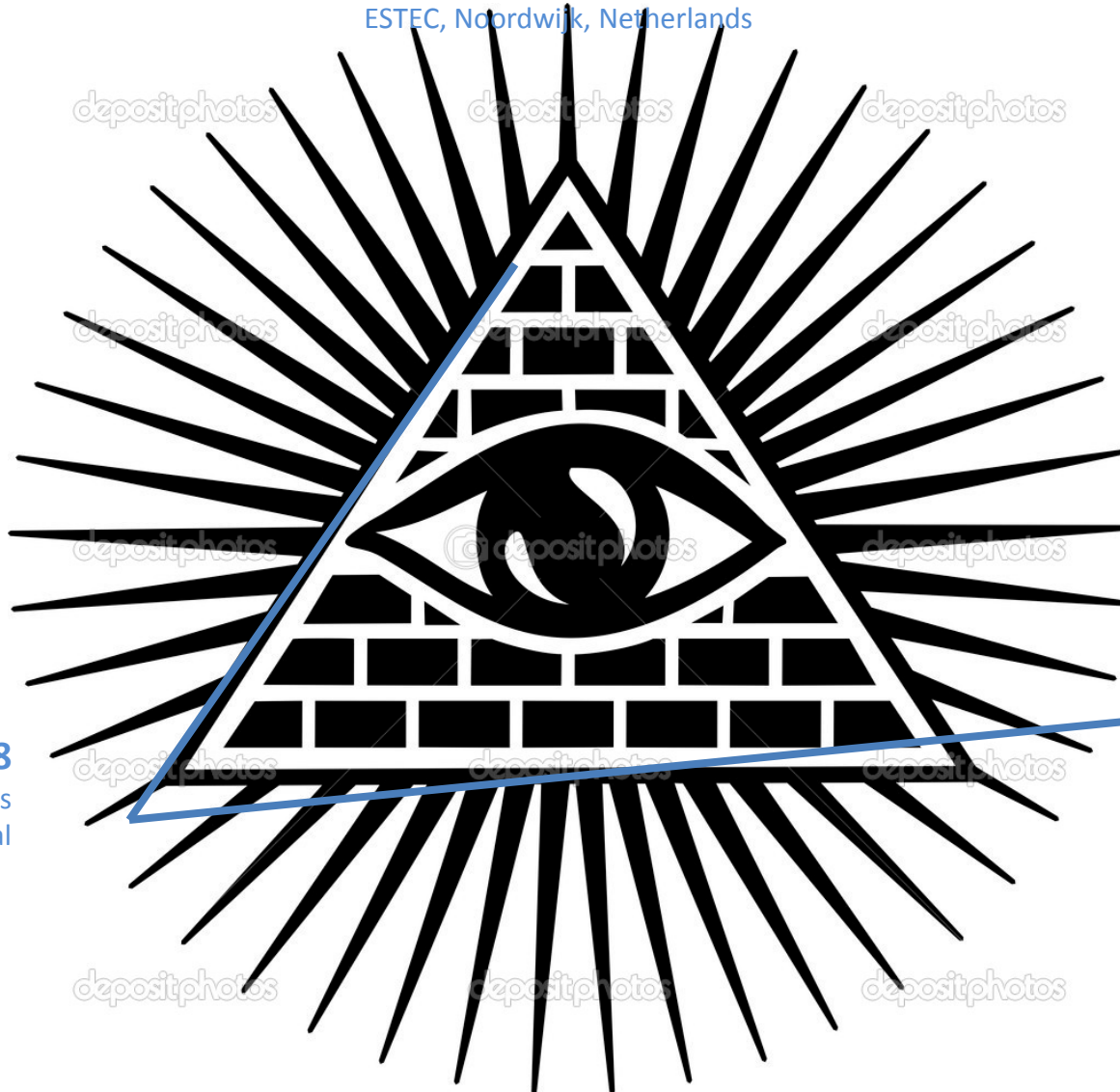


# HIGGS BOSON OBSERVED

## July 2012

# AMICSAs in the map

2010, 2012  
ESTEC, Noordwijk, Netherlands

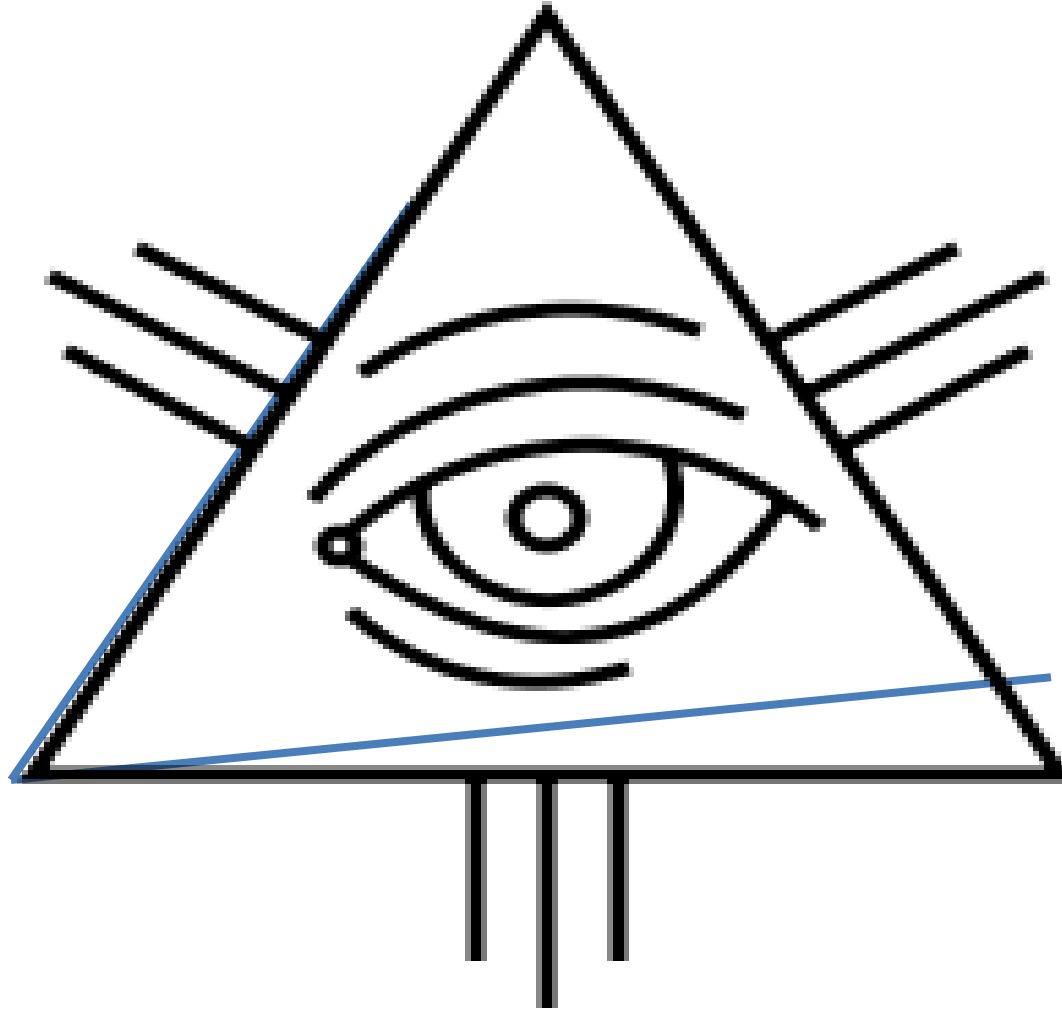


2008  
Sintra/Cascais  
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2006  
U. Thrace  
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Greece

# AMICSAs in the map

2010, 2012  
ESTEC, Noordwijk, Netherlands



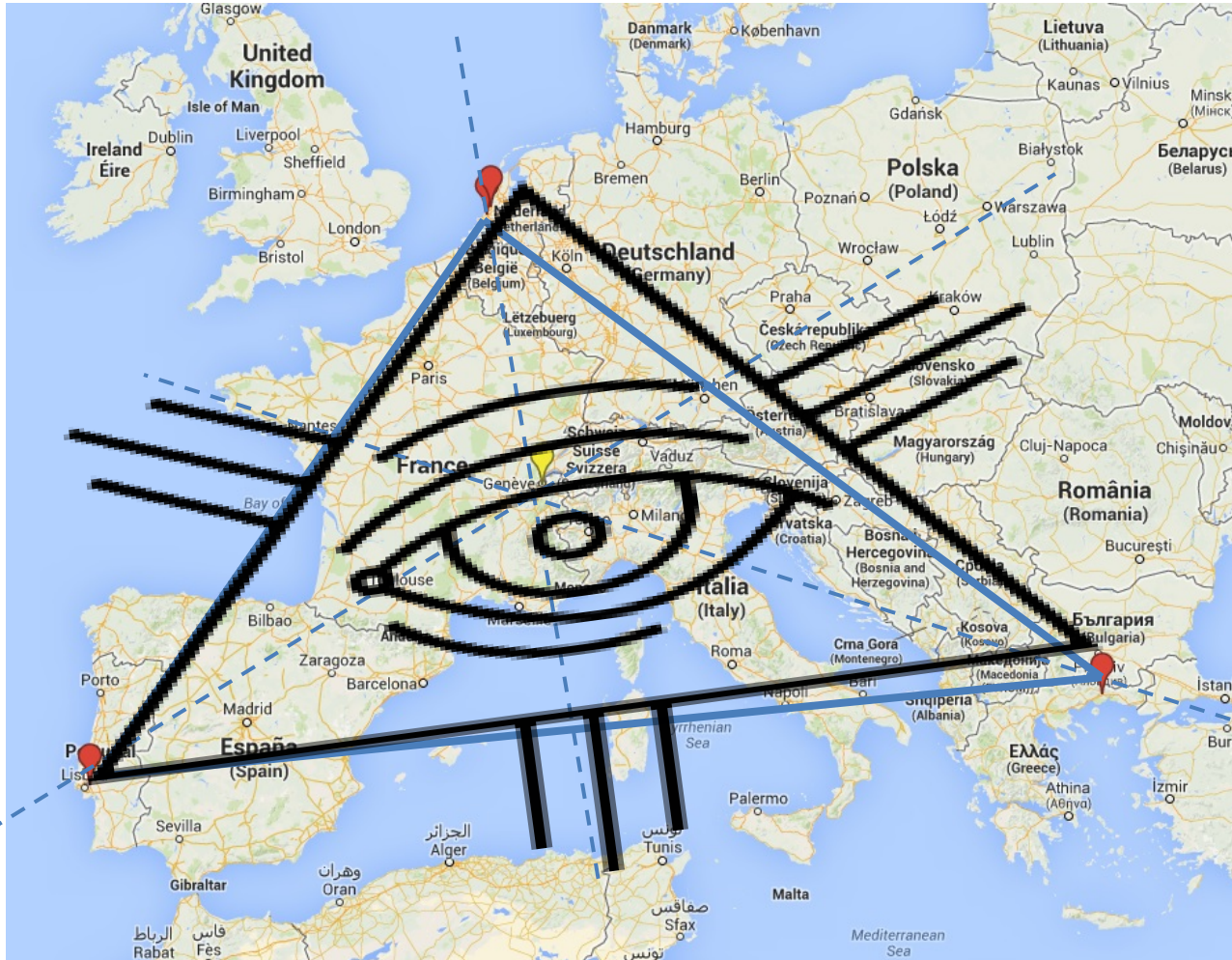
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Sintra/Cascais  
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# AMICSAs in the map

2010, 2012

ESTEC, Noordwijk, Netherlands



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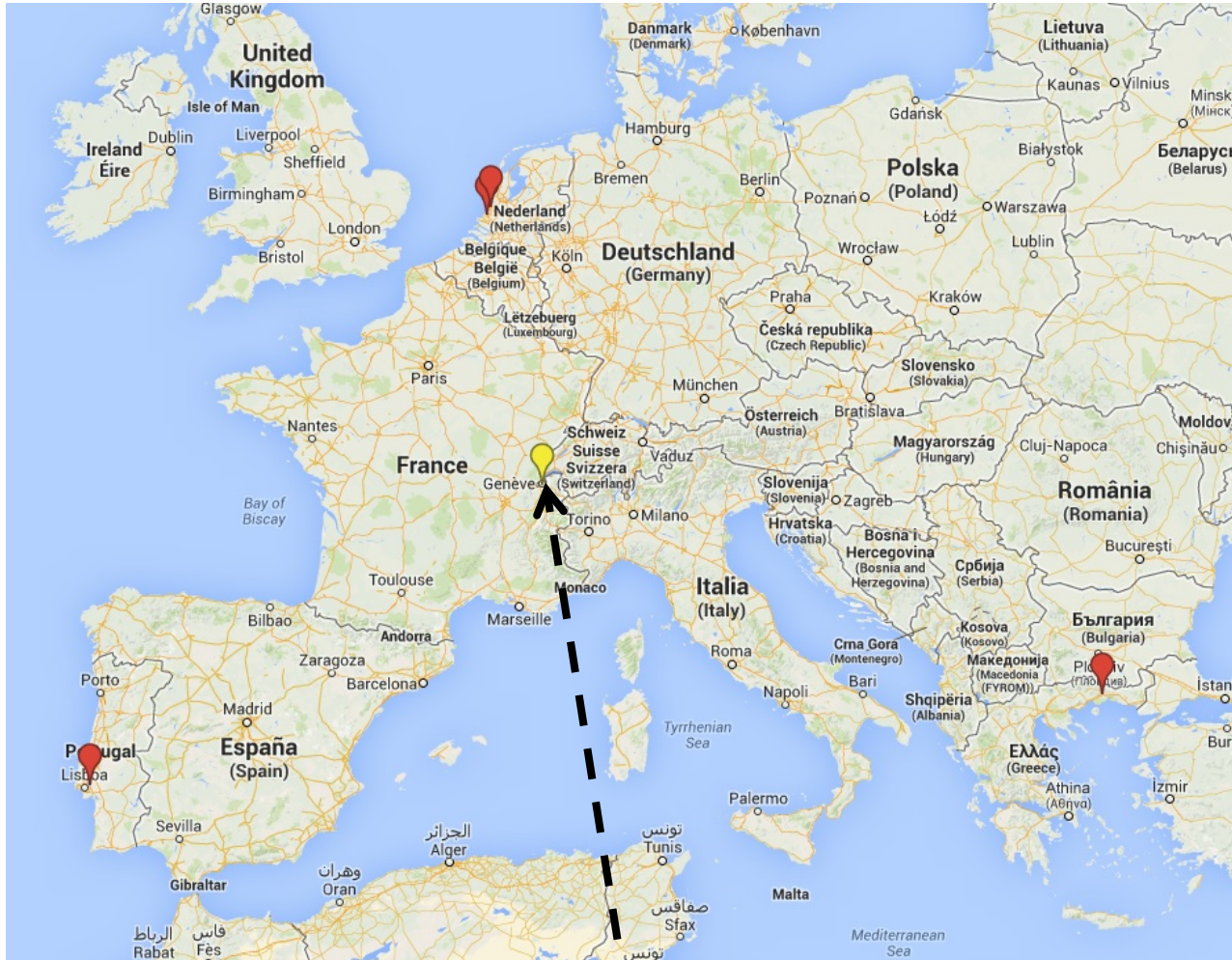
2014

CERN, Geneva, Switzerland

# AMICSAs in the map

2010, 2012

ESTEC, Noordwijk, Netherlands



2008  
Sintra/Cascais  
Portugal

2006  
U. Thrace  
Ξάνθη (Xanthi)  
Greece

2014  
CERN, Geneve, Switzerland



# AMICSA venues history

**2006**

U. Thrace, Ξάνθη (Xanthi)  
Greece



**2008**

Cascais/Sintra  
Portugal



**2010, 2012**

ESTEC, Noordwij  
Netherlands



**2014**

CERN, Genève  
Switzerland



# Between AMICSA 2012 and 2014...

- **ESA, CNES, DLR continued to support multiple A-MS IC technology developments with many companies in Europe**
- **A-MS “Users” Round Table - 29 August 2012**
- **“EAMAS WG” - ESA Analogue and Mixed-signal ASIC Working Group – created after the RT**

Short summary of

**ROUND TABLE :**

Analogue & Mixed-signal  
ASIC Technology **Requirements** and **Priorities** of  
Space Industry **Users**

Organised by [ESA](#), [ESTEC](#), [TEC-EDM/QTC](#), 29/08/2012

# RT OBJECTIVES and QUESTIONS

## OBJECTIVES:

identify space industry user's A/MS ASIC techno & application priorities to consider them in ESA's future technology improvement activities.

## The QUESTIONS: **WHAT...**

1. **company's experience** developing and/or using analogue and mixed ASICs for space applications?
2. **applications** where mixed/analogue ASICs have been and will be developed or used by your company?
3. **expected benefits** (performance, integration, cost) in using analogue and mixed-signal ASIC technology in those applications?
4. **technical requirements** do your applications need to meet: ranges of V, F, power, noise levels, integration levels, life time, rad hardness, etc.?
5. **main problems** that your company has in using the mixed-signal ASIC technology for those applications?
6. **existing mixed/analogue ASIC technology(ies)** will be used by your company, according to your experience and feasibility studies? (i.e. which ASIC fabs/vendors, manufacturing processes, PDK and libraries, assembly and test options)
7. **your priorities:** what European mixed/analogue ASIC technology(ies) should get **support from ESA** in order to facilitate its use for space applications?
8. **technology improvements** should be done for your preferred mixed/analogue ASIC technology (e.g. better transistor models, better PDK, etc.)?

# Who attended the RT (on invitation)

## presenting (17)

Arquimea (E)  
 AST (UK,F,E,D)  
 E2V (F)  
 GM-Ideas (N)  
 ID-MOS (F)  
 ISD (G)  
 Kayser-Threde (D)  
 RUAG (S,CH,A)  
 Saphyrion (Nemerix) (CH)  
 Sitael (Aurelia)(I)  
 SRON (NL)  
 TAS (F, I, E)  
 TESAT (D)  
 VTT (Fi)

CNES (F)  
 DLR (D)  
 ESA (NL)

ASI (I) – no answer

## not presenting, but attending (10)

Aeroflex (USA, UK)  
 ATMEL (F)  
 IHP (D)  
 ON-Semi (B)  
 Ramon Chips (Israel)  
 STMicroelectronics (F)  
 Telefunken (D)

CNM (E )  
 INTA ( E )  
 VH-S (D)

Wider ESA/ESTEC invitation

Aeroflex Gaisler (S) - declined  
 DUTH (G) – no answer  
 Omnisys (S) – no answer  
 S3 (ChipIdea, now Synopsys) (Portugal) – no answer  
 Syderal (CH) – no answer

# RT Agenda

- Short intro of the groups / people at ESA involved in A-MS technology
- Short overview of on-going A-MS ESA activities
- Sequence of Industry (users) 20' presentations, answering the same questions: techno/application preferences, priorities, future needs, etc.
- Open discussion, conclusions

# TEC EDM – Microelectronics Section

## A / MS on going activities

C10	<b>Low power, high speed DAC (10-12bits, 1.25Gbps, 0.5-1W):</b> DAC activity done by Kayser-Threde (D) with IHP(D) technology, 900€(+180K€CCN), TRP, close to its end. (this was A4 in previous 2007 roadmap)
C11	<b>Technology Study And Development Test Vehicles For Front End Readout ASICs:</b> design, prototype and test a set of configurable mf (100khz-10mhz) & hf (10mhz-100mhz) radiation tolerant analogue circuit blocks (adc, dac, filter, low-noise amplifier and linear output amplifier) that can constitute together the amplification, signal-condition and converter function of a selected cosmic vision instrumentation payload. Arquimea(e),trp-siuc, 625+725k€
C12	<b>Development &amp; Qualification of a 14-bit ADC ASIC for Pressure Sensors :</b> 14 bits 100KHz ADC to bias pressure sensor for launchers applications. Design, manufacture, test and qualification. 1M€, DUTH(G), to finish in Q3-2012. (this activity was E28 in 2007 RM)
C13	<b>Development of a Very High Resolution (24bit) ADC for Space Applications</b> Greek Task Force, ISD (G), 370K€
C14	<b>DAREplus (Design Against Radiation Effects) ASICs for extremely rad hard &amp; harsh environments:</b> fix memory compiler, new cells and design kit for analogue. New customer ASIC for Cosmic Vision. IMEC(B), TRP, 1.2M€

Support to several other A/MS activities in other sections (CAN transceiver, LDVS drivers, microcontroller, power management IC, etc.

=> Future update of the ESA Tech. Harmonisation Microelectronics Dossier coming in **2015**

## TEC-QTC -- Space Components on-going mixed signal Activities

- Assessment and characterisation of a mixed signal technology (Sitael - 250k€)
- Evaluation and characterisation of a harmonised mixed signal ASIC flow (ISD - 510k€)
- ESCC Evaluation of IHP 0.13 technology. DLR/ESA joint funding (~1.2M€)
- Other: Various product development, evaluation and qualification activities: DACs, ADCs, MosFET driver ASIC, PoL ASIC, etc.



## Summary of ROUND TABLE, outcome:

- 15 inputs/summaries from small, medium and large companies and CNES.
- Not an exhaustive view, but a good sample, together with AMICSAs
- Easy agreement on what the benefits are or maybe
- Good synthesis of what the main, some common **problems and gaps** seem to be.

ROUND TABLE conclusions:  
what are the priorities / gaps (1/3)

- lack of well characterized (electr and rad) T models
- no standardized suppliers for A/MS
- RHDB digital and analogue libs
- building blocks (IP, ASSP)
- EU std. development flow
- new license models for the expensive EDA tools
- analogue BIST
- std. for sensors and ROICs
- HV power devices
- some new devices needed for ADC, LO, optical and electrical sensor buses
- more std. for analogue i/f

ROUND TABLE conclusions:  
what are the priorities / gaps (2/3)

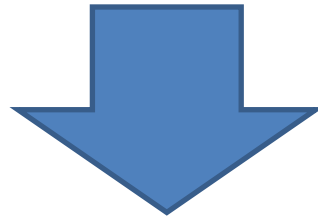
- second sources
- university support is unstable - maintaining know-how
- costs of qual lot for flight
- maximize dual-use, more than space
- maintain suppliers interest
- high NRE costs for wafers, Ips...
- lack of common stand. Packages, and test approach
- DK do not allow ELT (schematic, layout, DRC, LVS)
- maintaining DK / IP /lib support
- ESA list of test rad-hard technology
- time and cost of selecting and validating a technology

ROUND TABLE conclusions:  
what are the priorities / gaps (3/3)

- techno eval is not core business of designers / users.  
Not equipped
- **coordinating all elements in supply chain**
- ESA should help in making rad test assessments of technology available
- facilitating rad test stands and equipment to industry
- **duplication of activities**, efforts - more team work, joining forces to help sustain the service/techno offer
- Focus on European manufacturers
- Reduce # of actors, simplify # options in supply chain
- More frequent MWP runs?
- **No ESCC supply chain, no EPPL A/MS tech**
- Know-how confidentiality – difficulties to share

# A-MS “Users” Round Table

29 August 2012



## “EAMAS WG”

**E**SA **A**nalogue and **M**ixed-signal **A**SIC

Working Group

# ESA **A**nalogue and **M**ixed-signal **ASiC** Working Group

- Creation of **Foundry Space Users Groups (SUG)**:
  - anyone interested can join, participate at SUG meetings, and/or access the Foundry SUG Alfresco shared repositories
  - if they provide a presentation to be shared with the SUG answering the following questions:

- **Foundry Space Users Group questions to be answered and shared:**

- 1) What are ... the application domains for your ASICs?
- 2) your ASIC design tool flow?
- 3) your general experience with the “Foundry” technology and provider (process variation, yield, matching, reliability, ...)?
- 4) your specific experience with the “Foundry” technology models, devices, IOs, (model accuracy with temperature, frequency, ) and design kit (HIT-KIT)?
- 5) your general radiation tolerance experience with the technology?
- 6) any radiation data to share?
- 7) any radiation-tolerant transistor models (or other device) to share?
- 8) what radiation characterization data you think is still missing?
- 9) what radiation tolerant devices you think are still missing but needed on this technology?

# ESA **A**nalogue and **M**ixed-signal **AS**IC

## Working Group

Done Already

- **AustriaMicroSystems SUG** 1st webex – Feb 2014 -> Alfresco shared repository
- **XFAB SUG** – 1st webex -> Alfresco shared repository
- Survey / analysis of potential IC **package reuse** -> not easy
- negotiations with **CADENCE** in pursuit of **cheaper tool licenses** for small companies -> initial interest shown but nothing agreed, to be further pursued...



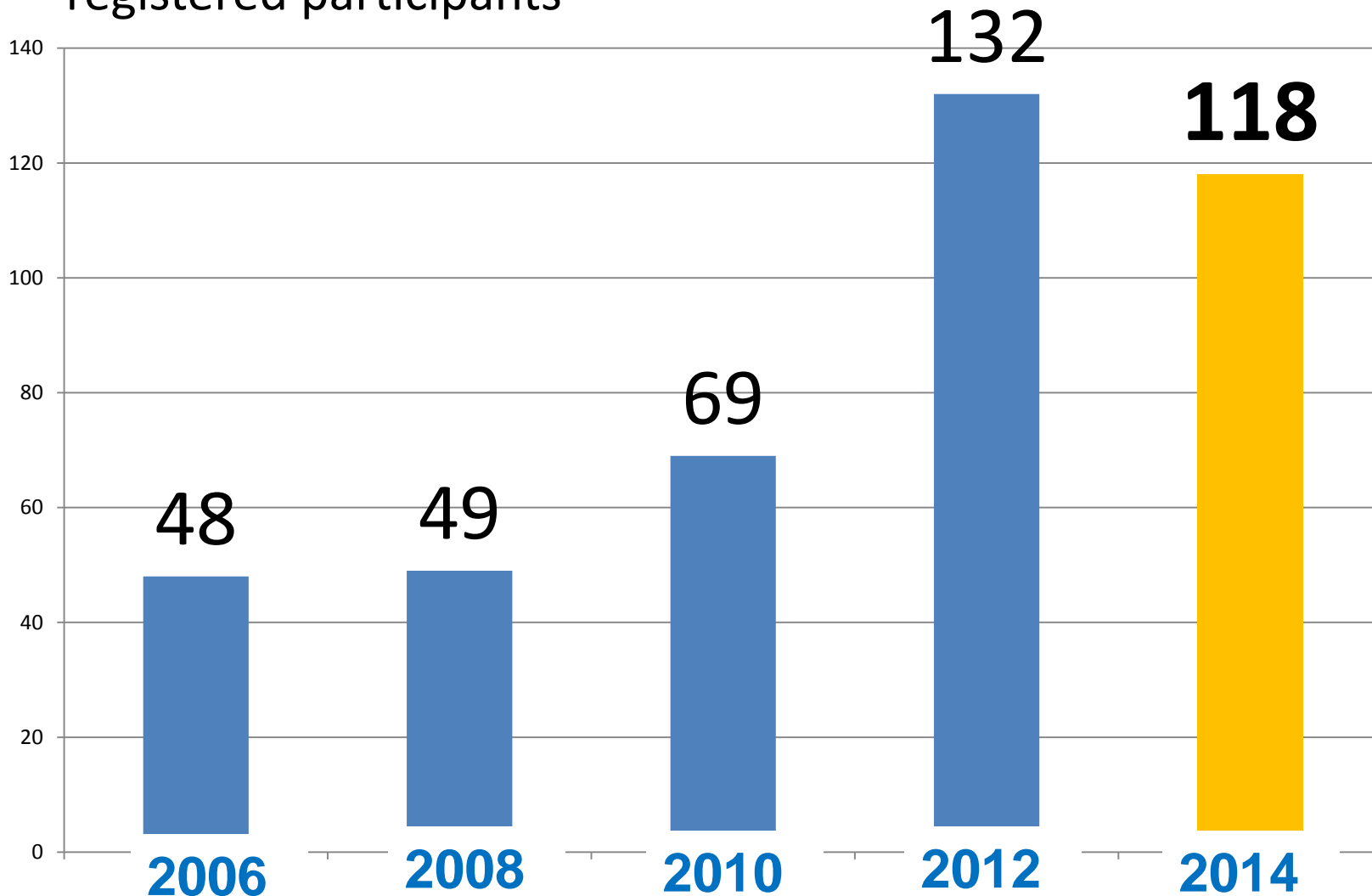
**Future Work**

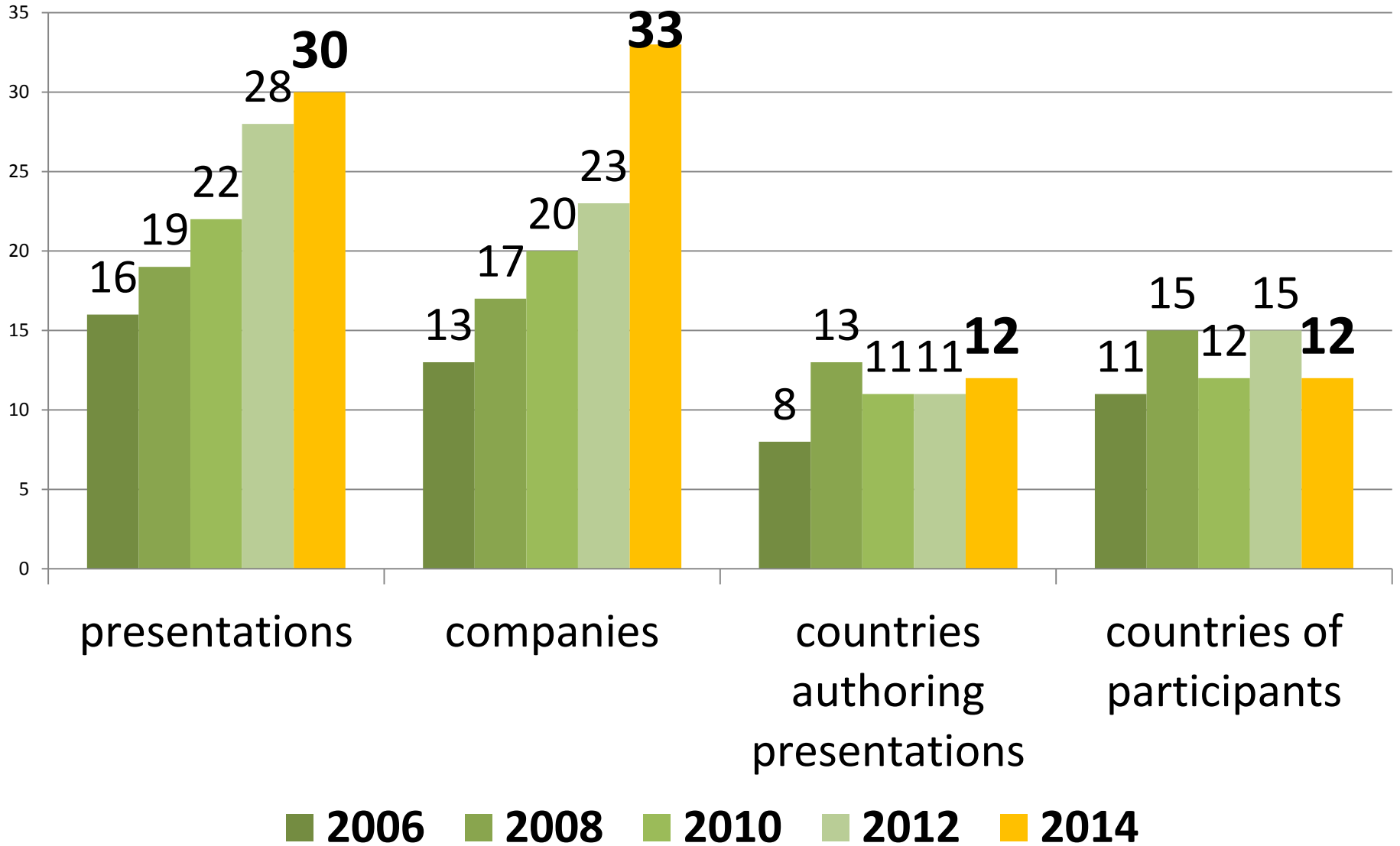
## ESA Analogue and Mixed-signal ASIC Working Group

- **IHP SUG** 1st webex – planned Q3 2014 -> Alfresco shared repository
- **2nd SUG webexes** : Xfab, AMS, IHP ?
- New **ON-semi, UMC, TSMC SUGs** ?
- **DARE Day** at ESTEC, Dec 8<sup>th</sup> 2014
- **Inventory** of A-MS ASIC Design Kit / Libraries / IP owners / providers

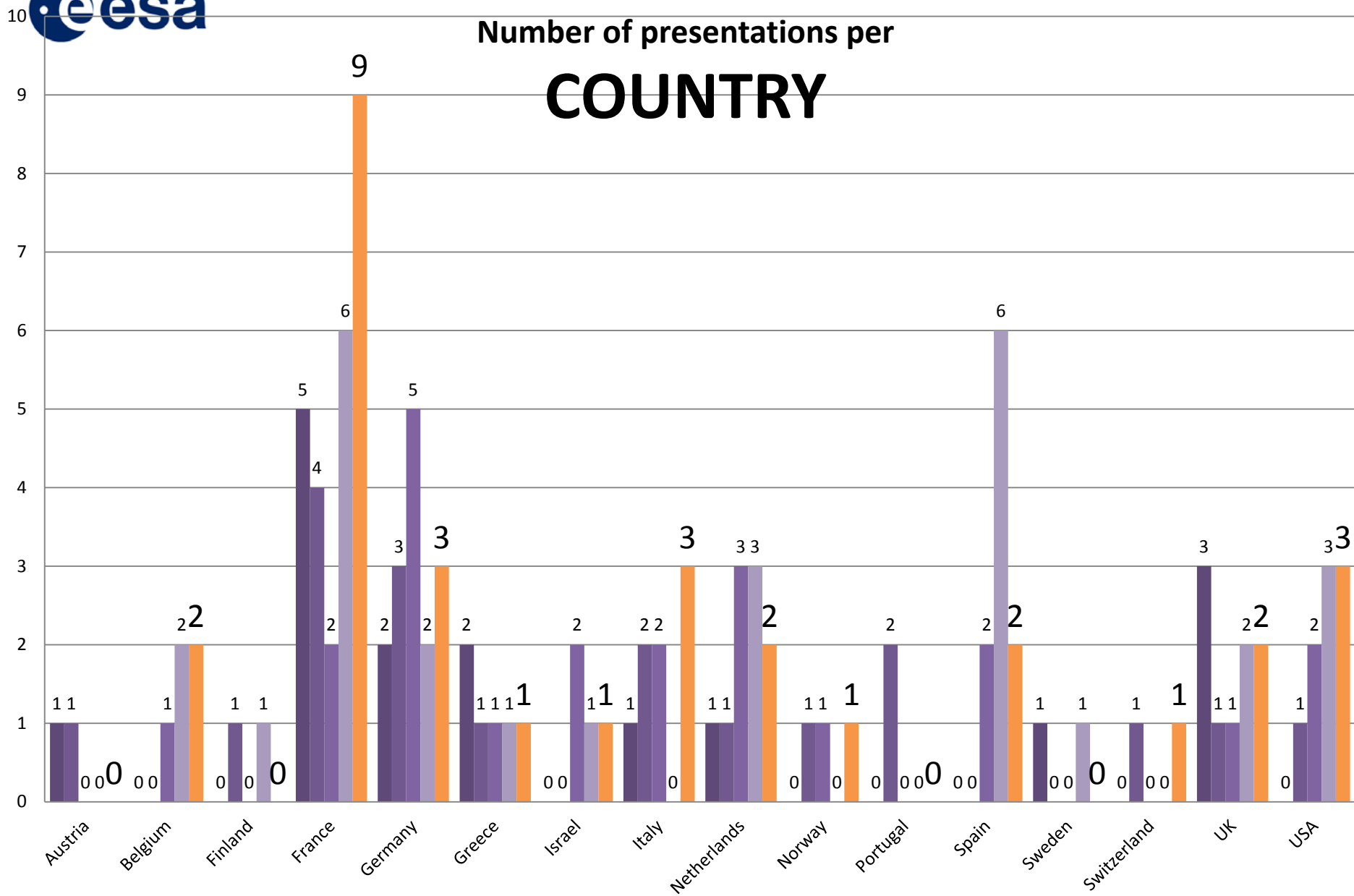
# AMICSA 2014: some statistics

registered participants



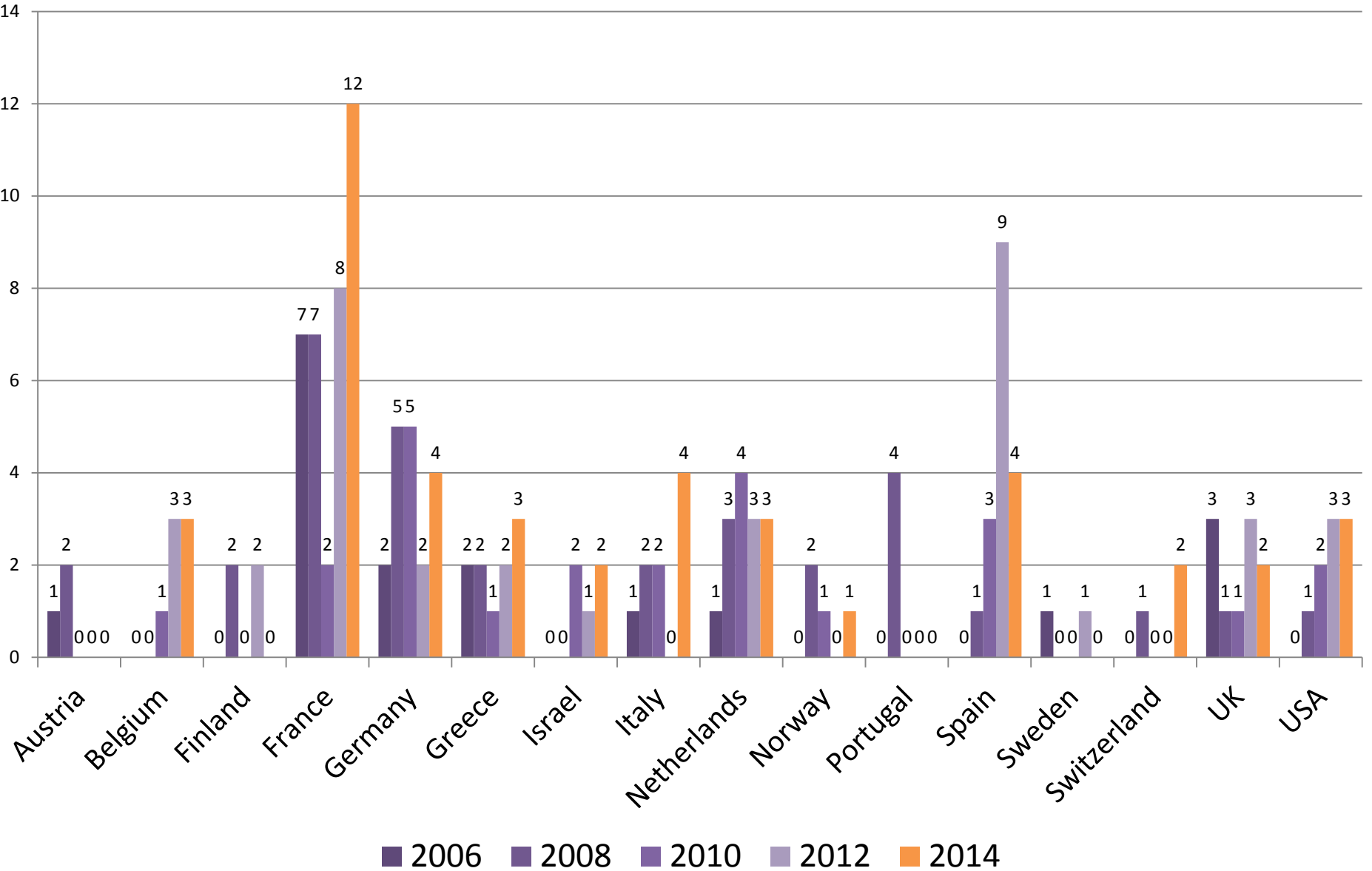


# Number of presentations per COUNTRY



2006
  2008
  2010
  2012
  2014

# number of presentations per COUNTRY + 2nd company



■ 2006  
 ■ 2008  
 ■ 2010  
 ■ 2012  
 ■ 2014

# AMICSA'2014

CMOS Image sensors (2) & CCD readouts  
Video processing chain  
ADC/DAC      high speed / high resolution

Low Power RX for Telecommand  
Magnetometer front end (2)

POL DC-DC and Power converters (2)

High energy particle accelerators  
Rad hard libs (2)

CCD biasing

low speed high resolution ADC

Design Kits with LV & HV transistors and NVM (4)

# Applications

Low power SRAM compilers for LHC  
IR/SWIR detectors FE

Radiation monitors, dosimetry

Silicon Drift Detectors analogue Front Ends

microcontroller

Charged particle / single-photon detection FE

LDVS drivers, receivers and repeaters (3)

Digital Step Attenuators for Microwave MS ICs  
Scalable Sensor Data Processor

# AMICSA'06-14

# More Applications

**CMOS Image sensors (2) & CCD readouts**

**Video processing chain**

**ADC/DAC/HSSL high speed / high resolution** low power telecom processors  
(mobile & broadband) & **direct down/up conversion from/to RF or IF**

**CAN 1553 transceivers**

**TM acquisition & data handling IO control**

**Low Power RX for Telecommand**

**Magnetometer front end (2)**

Slow sampling high resolution

**POL DC-DC and Power converters (2)**

**LASER interferometer**

**AOCS**

**Environmental (T, wind, humidity) monitoring**

**X, Gamma ray spectroscopy readout**

**GNSS receivers Front End**

**High energy particle accelerators**

**Rad hard libs (2) and DLLs for SoCs**

**Low speed regulated and CCD biasing**

**low speed high resolution ADC, and DAC for  
control and calibration**

**Design Kits with LV & HV transistors and NVM (4)**

**Low power SRAM compilers for LHC**

**IR/SWIR detectors FE**

low power telecom processors

**Radiation monitors, dosimetry**

**High Power commands management**

**ISM radar receivers Front ends**

**Local oscillator MMIC for Ka-band down conversion in  
satcom**

**Silicon Drift Detectors analogue Front Ends**

**Optical wireless links**

**microcontroller**

**Reconfigurable multi-instrument detector FE**

**Charged particle / single-photon detection FE**

**SAR RX / converter for L, C, X bands**

**Comparator for cross-correlator for SAR**

**Actuators drivers**

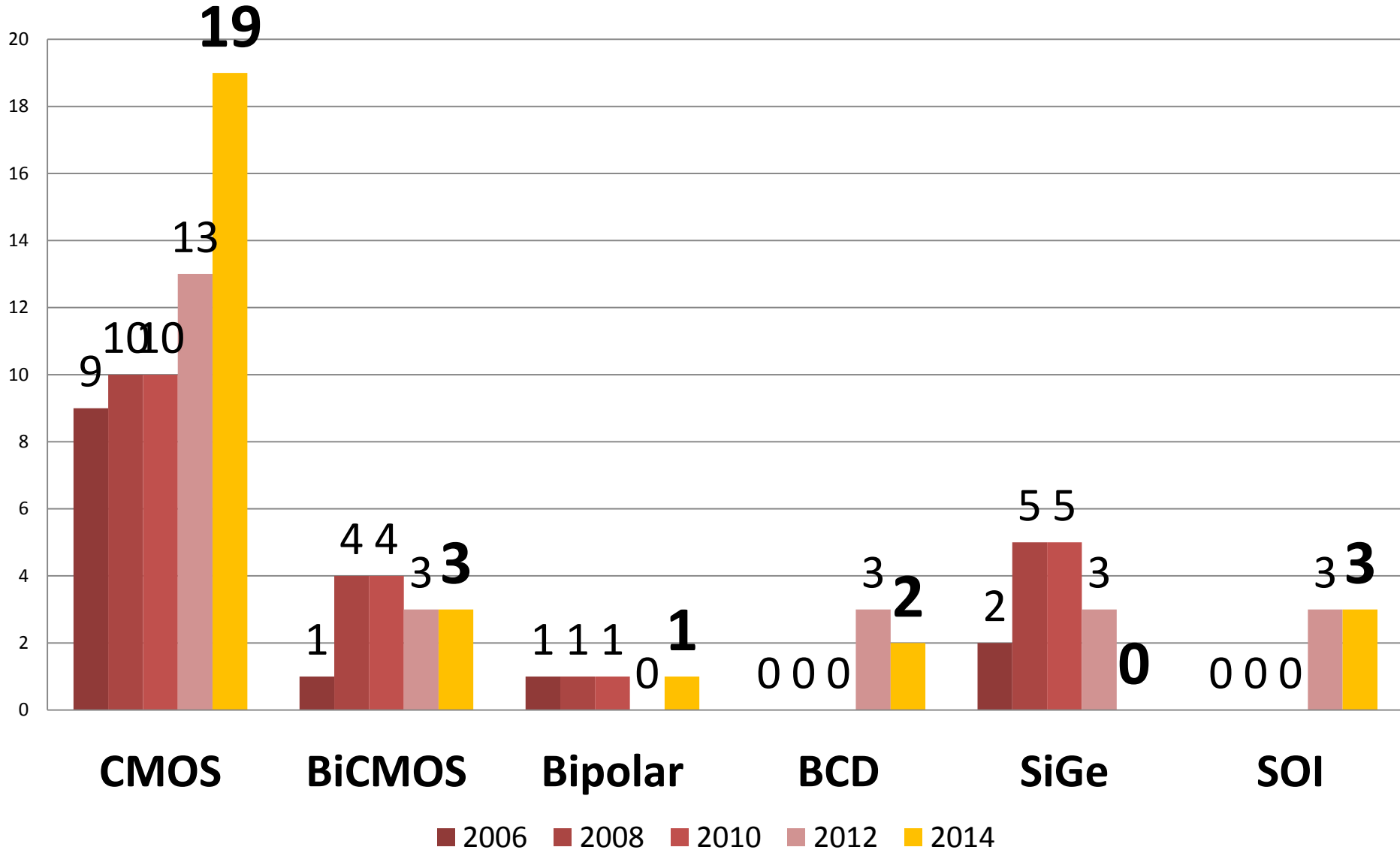
**LDVS drivers, receivers and repeaters (3)**

**Decentralised power & env. Management “micronodes”**

**Digital Step Attenuators for Microwave MS ICs**

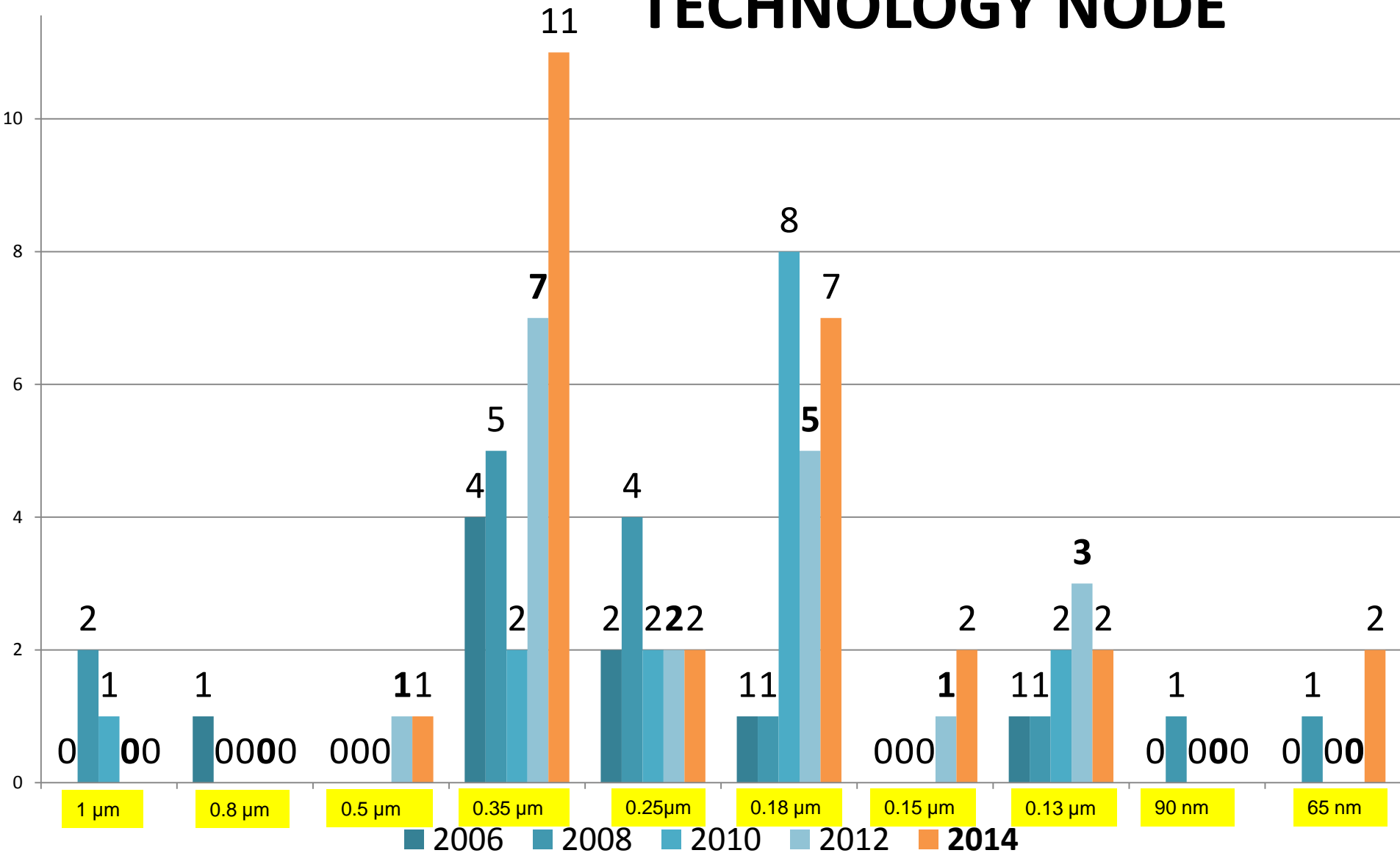
**Scalable Sensor Data Processor**

# number of presentations talking about TECHNOLOGY TYPES

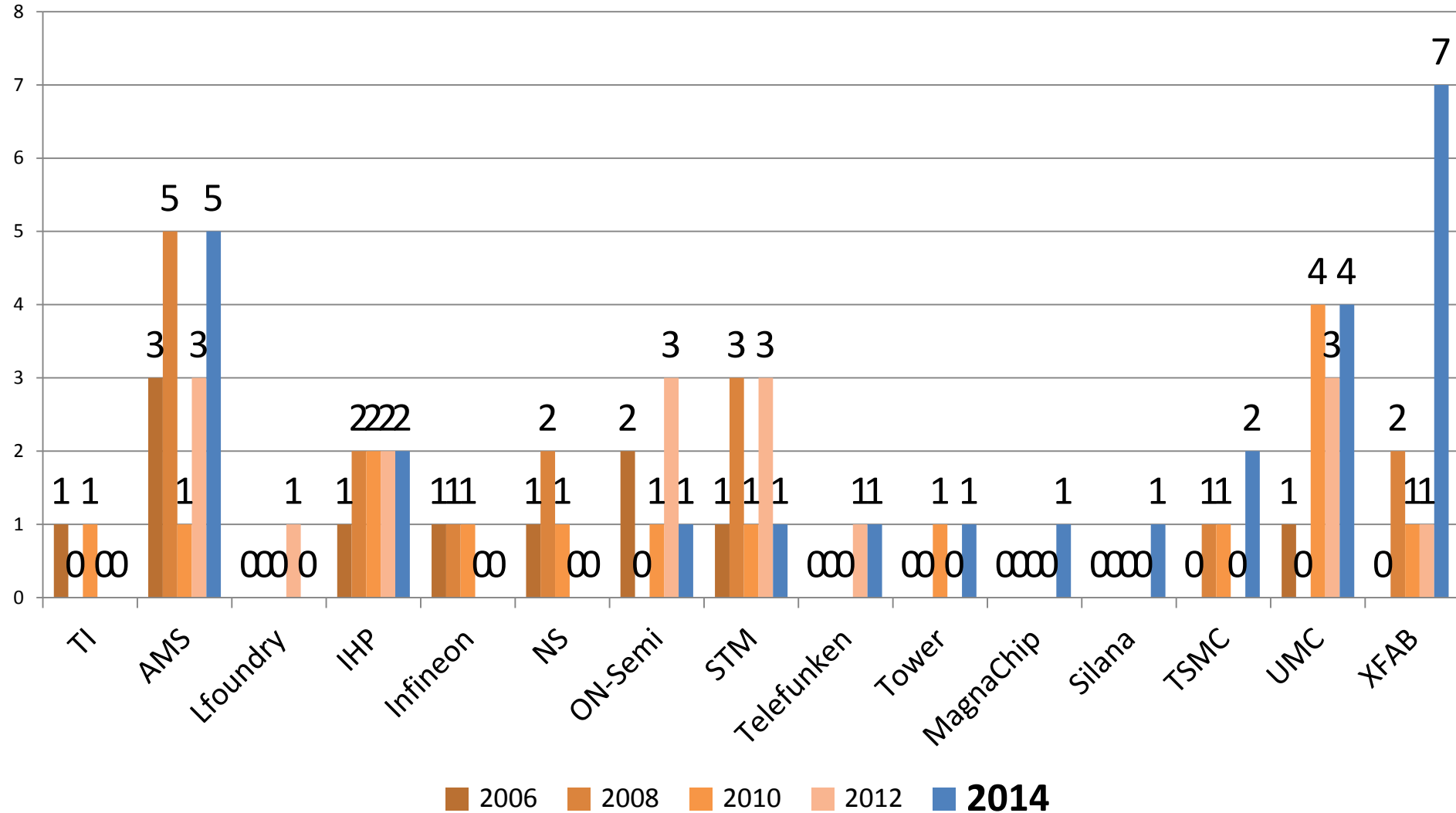




# TECHNOLOGY NODE



# FOUNDRY



**AMICSA 2012**



**Europractice + CMP**

**Foundries used for space mixed-signal ICs**

**TI (NS)**

**XFab**

**RHBD Digital  
Libs exist**

**ON**

**Infineon**

**IHP**

**TI**

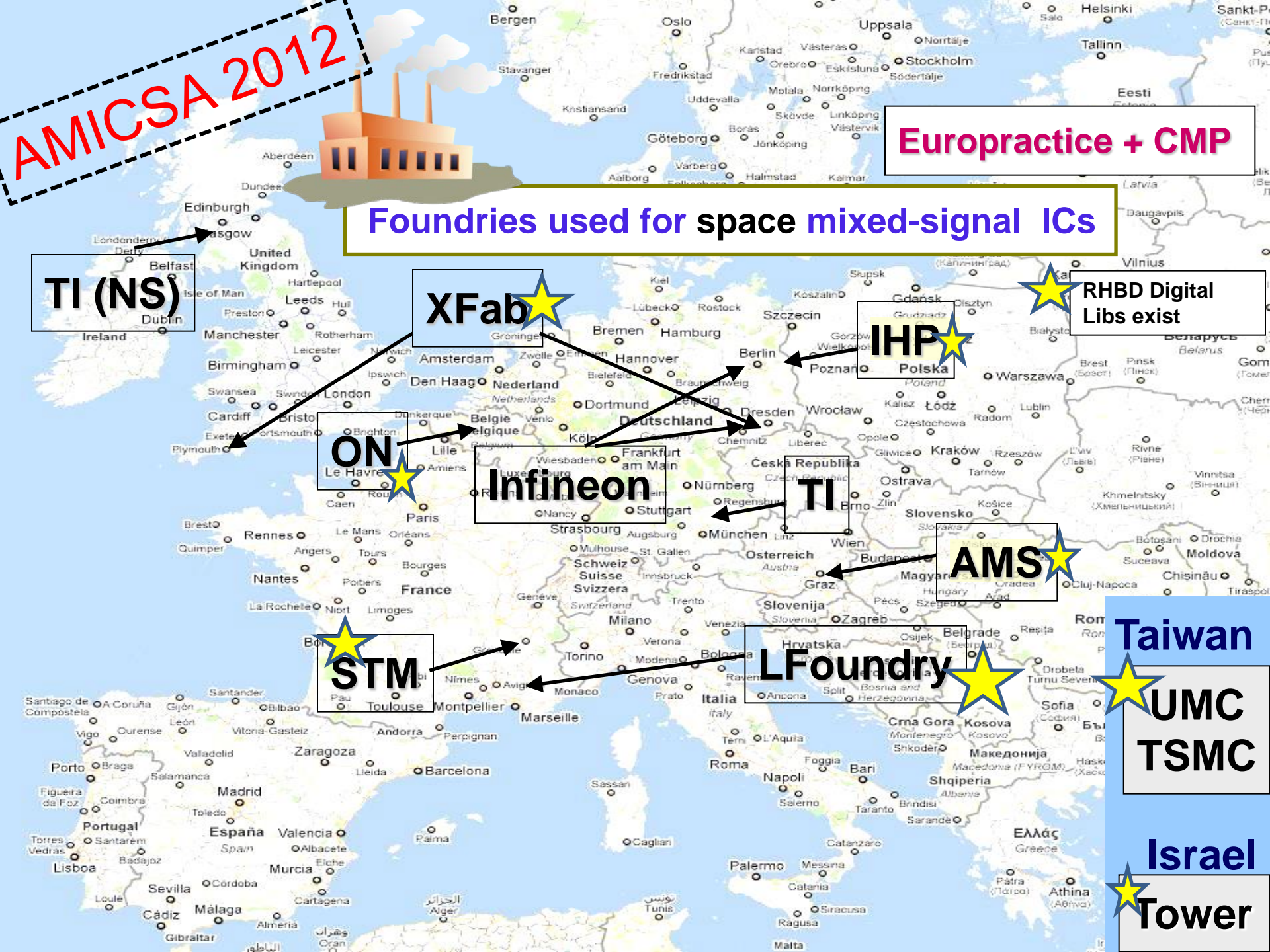
**AMS**

**STM**

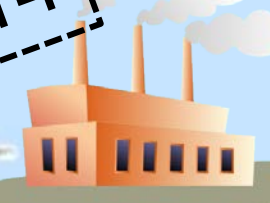
**LFoundry**

**Taiwan**  
**UMC**  
**TSMC**

**Israel**  
**Tower**



**AMICSA 2014**



**Europractice + CMP**

**Foundries used for space mixed-signal ASICs**

**TI (NS)**

**XFab**

**IHP**

**ON**

**Infineon**  
**Telefunken**  
**TI**

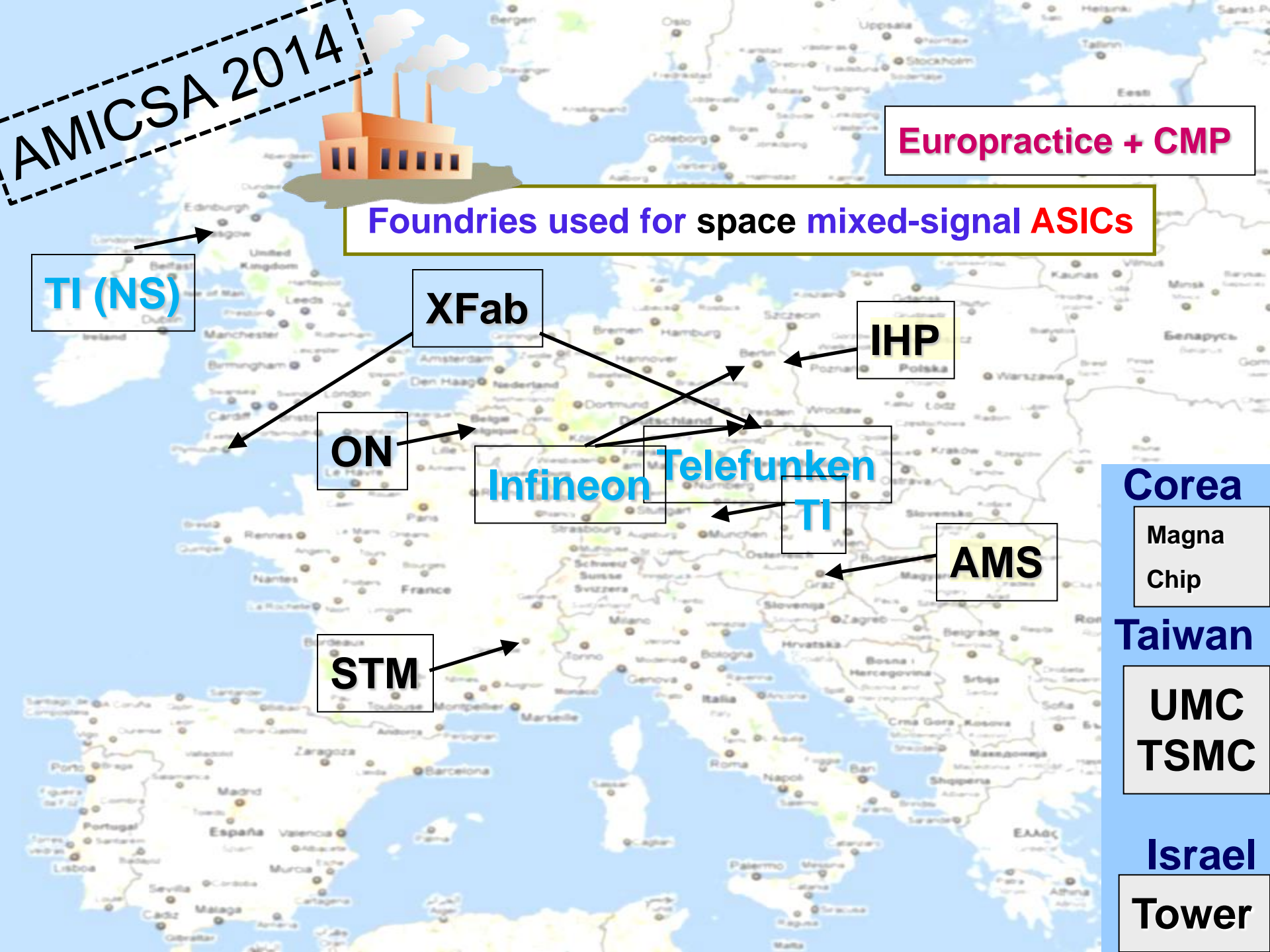
**AMS**

**STM**

**Corea**  
Magna  
Chip

**Taiwan**  
UMC  
TSMC

**Israel**  
Tower



Could we map A-MS space ASICs:

- **Design Kits – Libraries vendors?**
- **Re-usable IP Cores / large macro blocks vendors?**
- **One-stop-shops ?**
- **Supply chain actors with ESCC capability approval?**

# Some conclusions

- AMICSA 2014 was successful and there is (still) growing interest among A/MS for Space IC design community
- AMICSA 2014 growing numbers: similar number of participants and countries, more talks and companies
- The diversity of target technology types and fabs, supply chain combinations and qualification approaches continues, depending on application domain, previous experiences and funds.

# More conclusions

- Trend to have more Analogue and Mixed Signal ASICs in our satellites, despite the **challenges** (technical complexity, high costs, controlling end-to-end supply chain and space quality)
- Because there are **benefits!!** Lower mass, volume, power consumption; Higher speeds, potential for higher reliability and shorter lead-times (monolithic vs. several components + PCB)
- **In preparation / future:** High Voltage A-MS, NVM, High Frequency A-MS, A-MS in 65nm or below??







# THANKS !

See you at  
AMICSA 2016...

but ...where?