Power Matters

Microsemi

Analog Front End Integrated Circuits for Mixed Signal Spacecraft Applications

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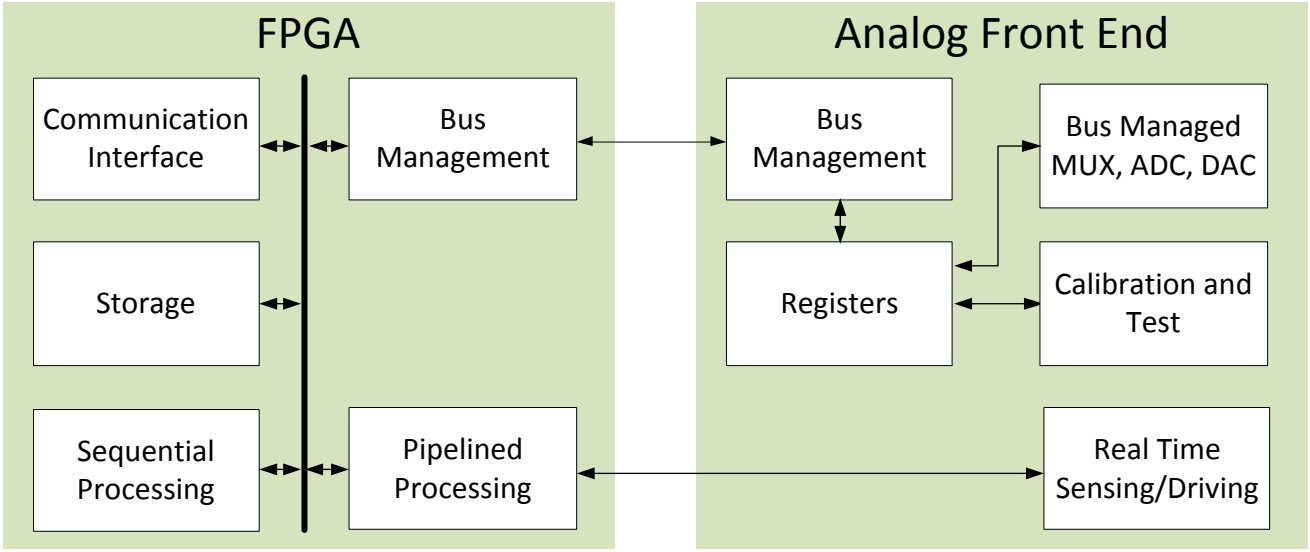
Abstract

- Mixed signal = Analog + Digital
- Partition to optimize performance and versatility.
- AFE = application targeted Analog Front End
- Use FPGA to personalize system
- Optimize AFE for interaction with FPGA.



Typical AFE Functions

- Differential Receiver
  - Common mode rejection
- Level Shifting
  - High side sensing
- ADC or DAC Converters
  - Analog to digital transitions
- Power Driver
  - Motors, actuators, relays, power converters
- Cold Sparing
  - Support redundancy
- Bi-level logic buffer
  - External logic levels too high for cores and fabrics.

AFE Approach Comparison

An AFE provides:

- High integration level
- Flexibility in target application set
- Minimal development
- Low power

Implementation Approach	Single Function ICs	AFE	Custom
NRE	Low	Low	High
Development Time	Months	Months	Years
Qualification	Fast	Fast	Long
Risk	Small	Small	High
Flexibility	High	High	None
Power	Worst	Good	Best
Reliability	Average	Excellent	Excellent
Size and Weight	Poor	Good	Best

Process Advantage

- Low voltage CMOS provides higher density, lower power consumption and supports digital hardening.
- Higher voltage DI processes with bipolar features have a wide voltage range, fault isolation and linear accuracy.

Process	Attribute	Advantage
Digital	Small geometry	High density
	Anti-fuse	High retention
	Triple redundancy	SEU immunity
Analog	Higher voltage	Wide range I/O
	DI process	Fault containment
	BCD process	High power and Precision linear

Programmable Digital

- Versatility is provided through the programming in the form of the FPGA HDL code.
- Hard coded logic in an AFE limits its versatility.
- Reducing the hard coded digital content in the AFE allows the companion FPGA to configure the basic capabilities of the AFE in different ways depending on the attributes of the application.
- Providing an AFE that is configurable for several applications allows the same flight proven component to be reused as the system requirements evolve.

FPGA Advantages

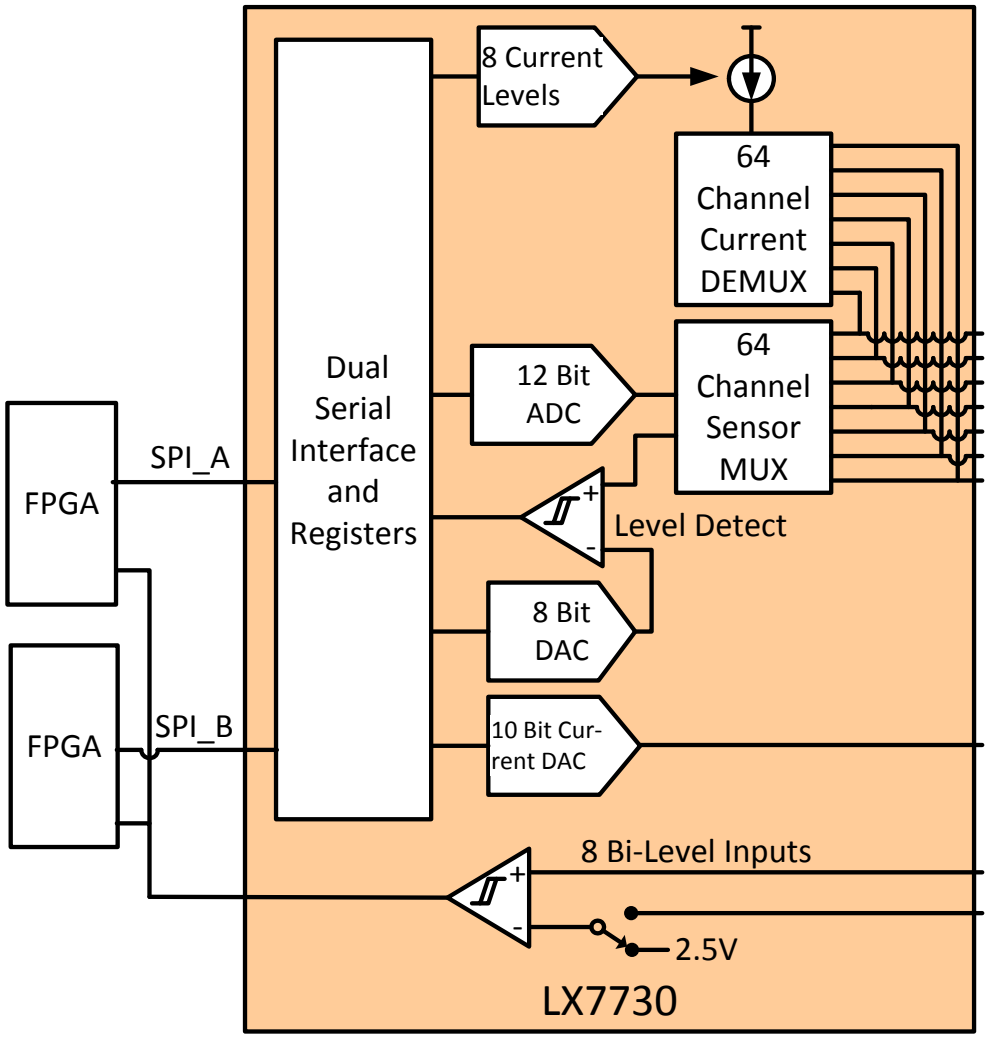
- Parallel signal processing
  - Multiple data paths can be processed simultaneously
- Complex math functions
  - Multipliers are implemented as hardware “math blocks” allowing fast processing in fabric
- Gate count and I/O can be scaled to the application needs
  - Wide range of gate counts available
- Single Event Immunity
  - Triple logic redundancy and voting

AFE Applications

- Telemetry Management
  - Monitoring a large number of sensors
- Motor Control
  - Power driver and position or speed feedback
- Power Control
  - Supervisor, reset, sequencing, margining

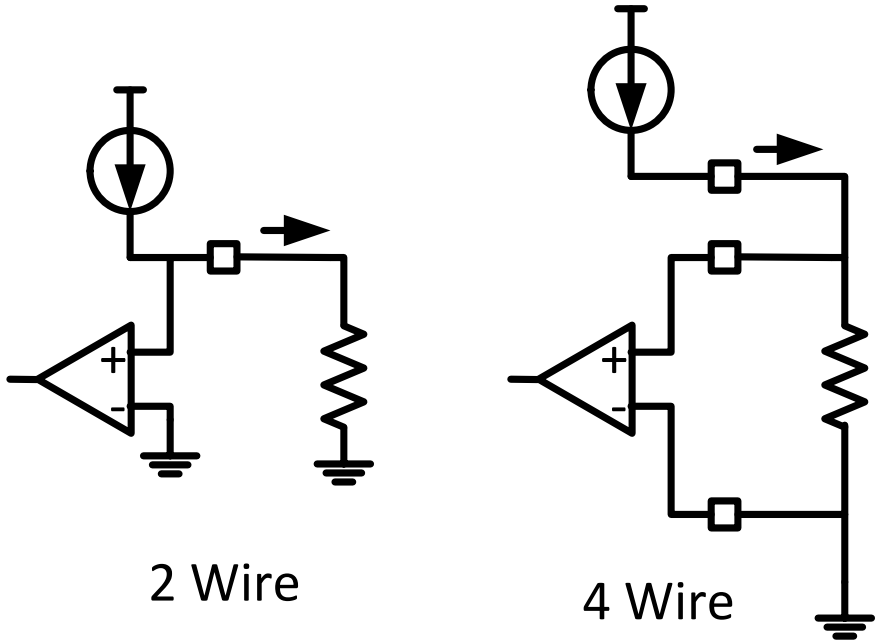
AFE Control and Configuration

- Write to Control Registers to configure.
- Read Status Registers to obtain results.
- Multiple interface ports support redundancy.



Passive Sensor Measurements

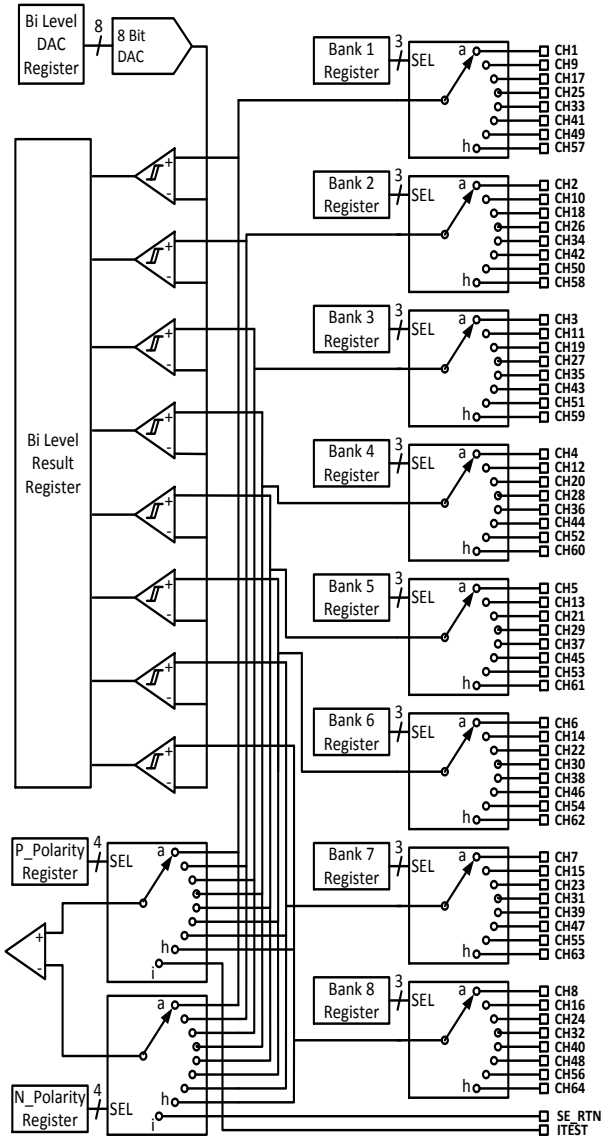
- Current source provides known stimulus.
- “Two Wire” measurement includes cable impedance.
- “Four Wire” measurement reduces error at the expense of more device pins.



Telemetry Multiplexer

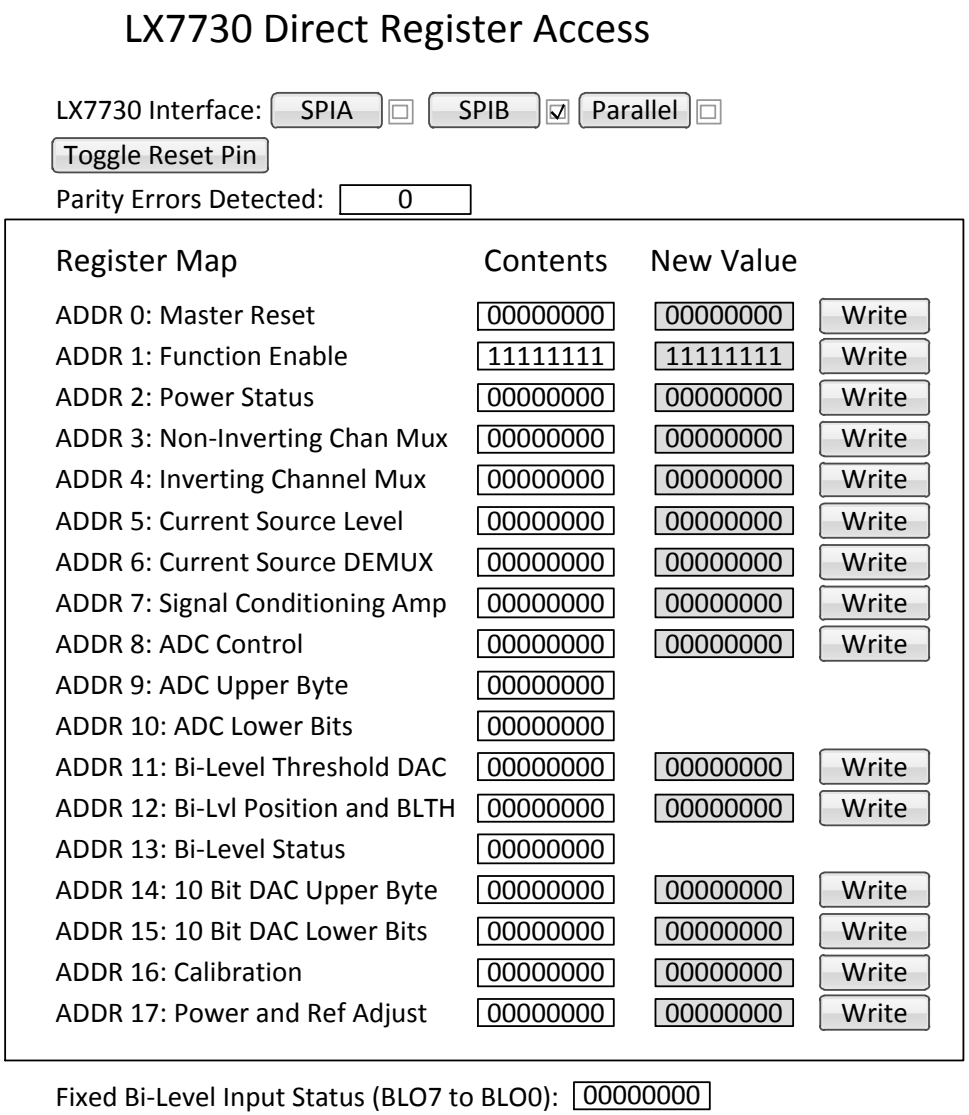
- Inputs configurable as 32 differential or up to 64 single ended inputs.
- 8 inputs can be simultaneously compared to an adjustable threshold.

	Pos 1	Pos 2	Pos 3	Pos 4	Pos5	Pos 6	Pos 7	Pos 8
Bank 1	CH1	CH9	CH17	CH25	CH33	CH41	CH49	CH57
Bank 2	CH2	CH10	CH18	CH26	CH34	CH42	CH50	CH58
Bank 3	CH3	CH11	CH19	CH27	CH35	CH43	CH51	CH59
Bank 4	CH4	CH12	CH20	CH28	CH36	CH44	CH52	CH60
Bank 5	CH5	CH13	CH21	CH29	CH37	CH45	CH53	CH61
Bank 6	CH6	CH14	CH22	CH30	CH38	CH46	CH54	CH62
Bank 7	CH7	CH15	CH23	CH31	CH39	CH47	CH55	CH63
Bank 8	CH8	CH16	CH24	CH32	CH40	CH48	CH56	CH64



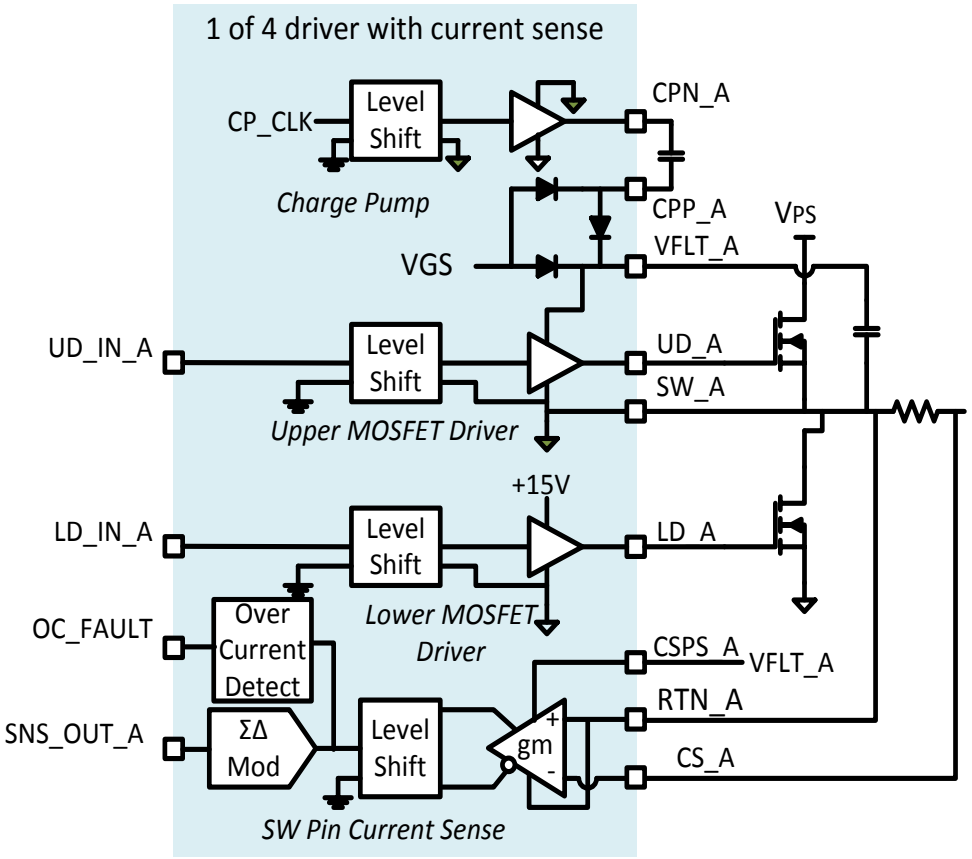
HDL modules for AFE

- SPI interface
- Parallel interface
- Single register reads and writes
- Data logging routine
- Calibration



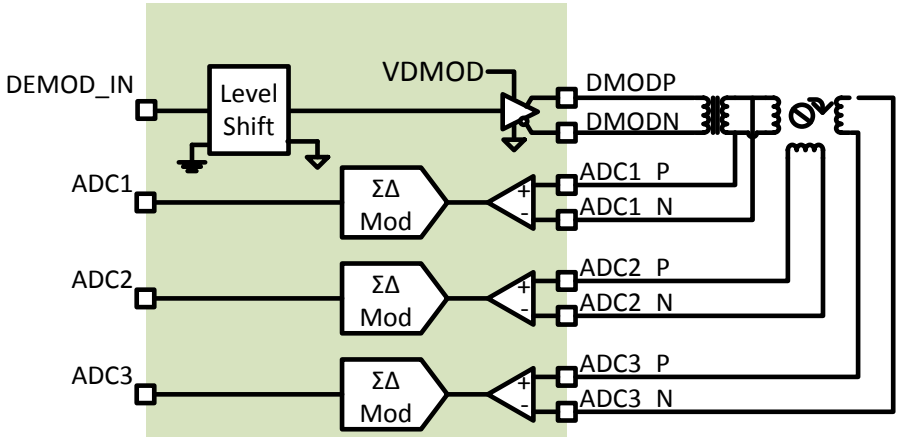
Motor Driver AFE

- Motor types:
  - Bipolar Stepper
  - Unipolar Stepper
  - BLDC and PMSM
- Half bridge driver
  - N ch switches
- Floating current sense
  - Measure at switch node.
  - Requires high CMR.
  - ΣΔ bit stream to FPGA.



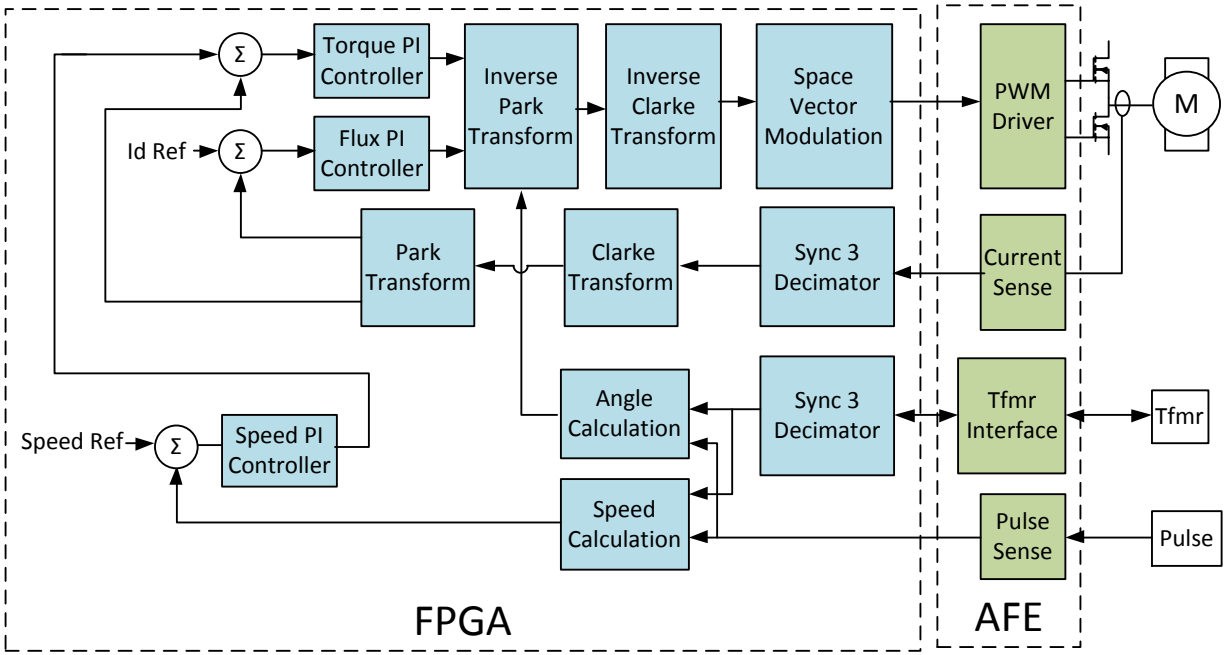
Position Sensing with Resolver

- Carrier frequency driver
  - Driven by repetitive bit stream.
- Sense inputs for sine and cosine.
  - ΣΔ Modulators in parallel
- FPGA provides signal processing
  - Parallel sinc3 filtering
  - Tracking converter for position and speed.



Motor Driver Partitioning

- The signal processing is performed by the fabric and the driver and feedback interfaces are implemented in the AFE.



Standard Motor Driver HDL modules

- 2 phase bipolar drive with microstepping
- Stepper average current regulation
- Sinc 3 filter and decimator w adjustable accuracy
- Pulse exciter for Resolver or LVDT
- Tracking Resolver to digital converter
- BLDC motor with trapezoid drive
- PMSM with sinusoidal drive
- Field oriented transformations
- Space vector modulation
- Fault management

Questions