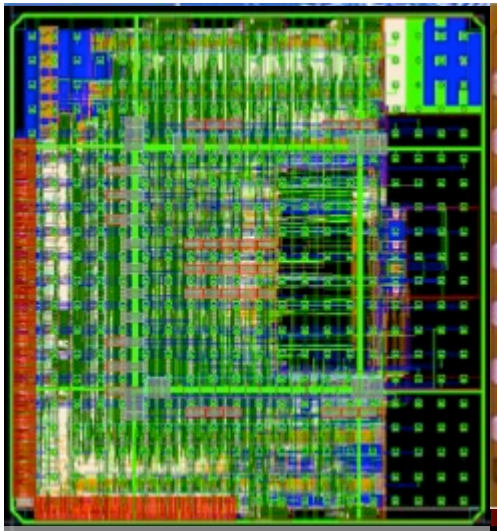
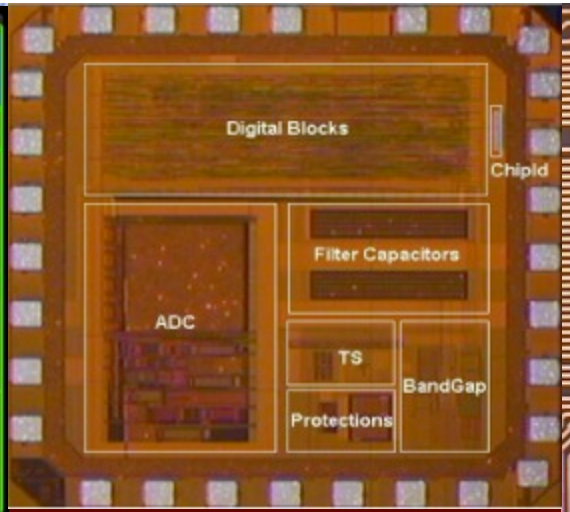
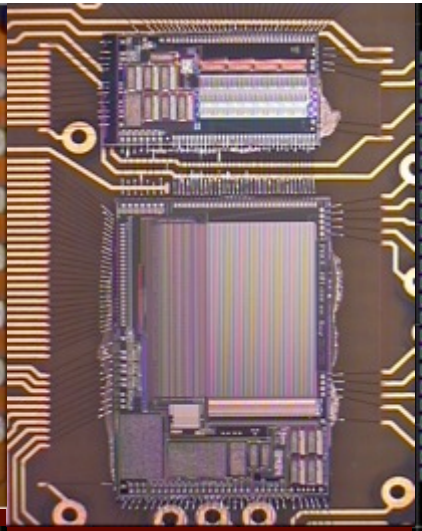
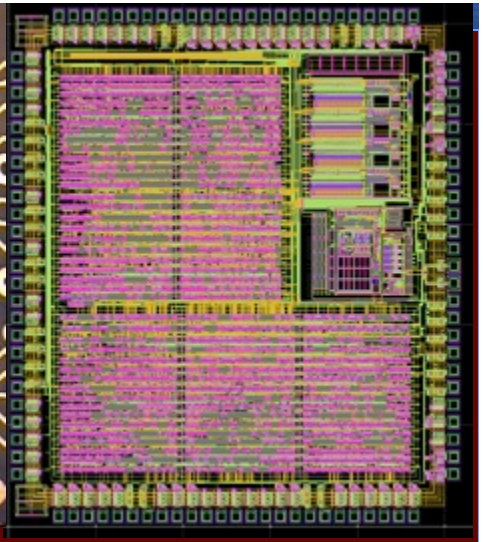
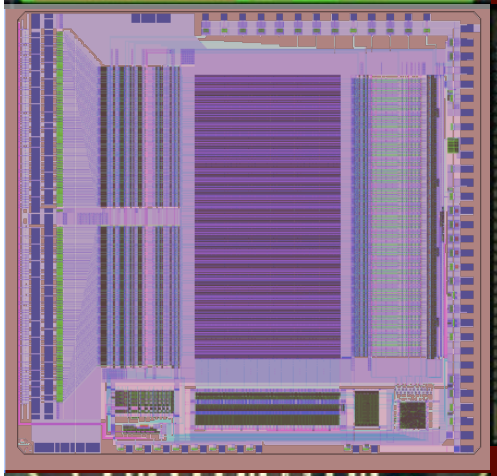
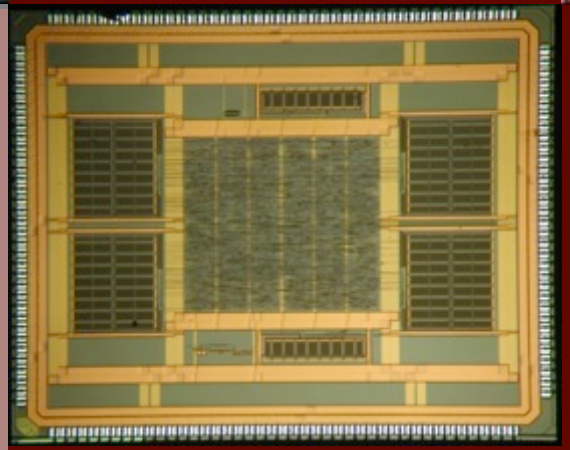












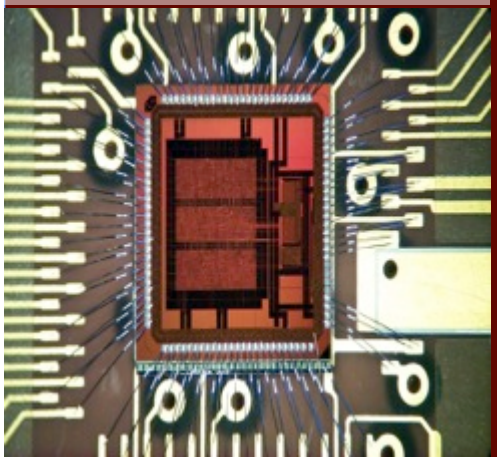
How Chips Pave the Road to the Higgs Particle: *Chips at CERN*

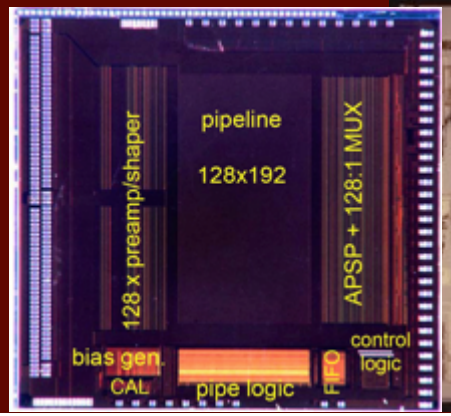
Erik H.M. Heijne

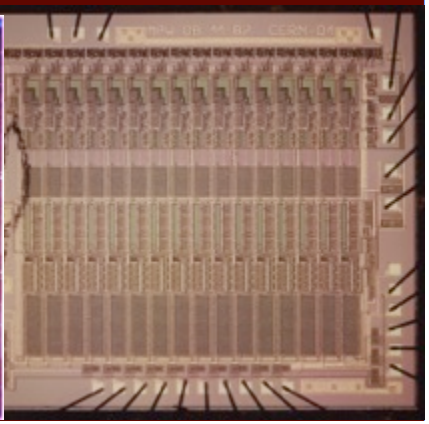
CERN – PH Dept. CH 1211
Geneva 23

Institute for Experimental and Applied Physics of the Czech Technical University in Prague

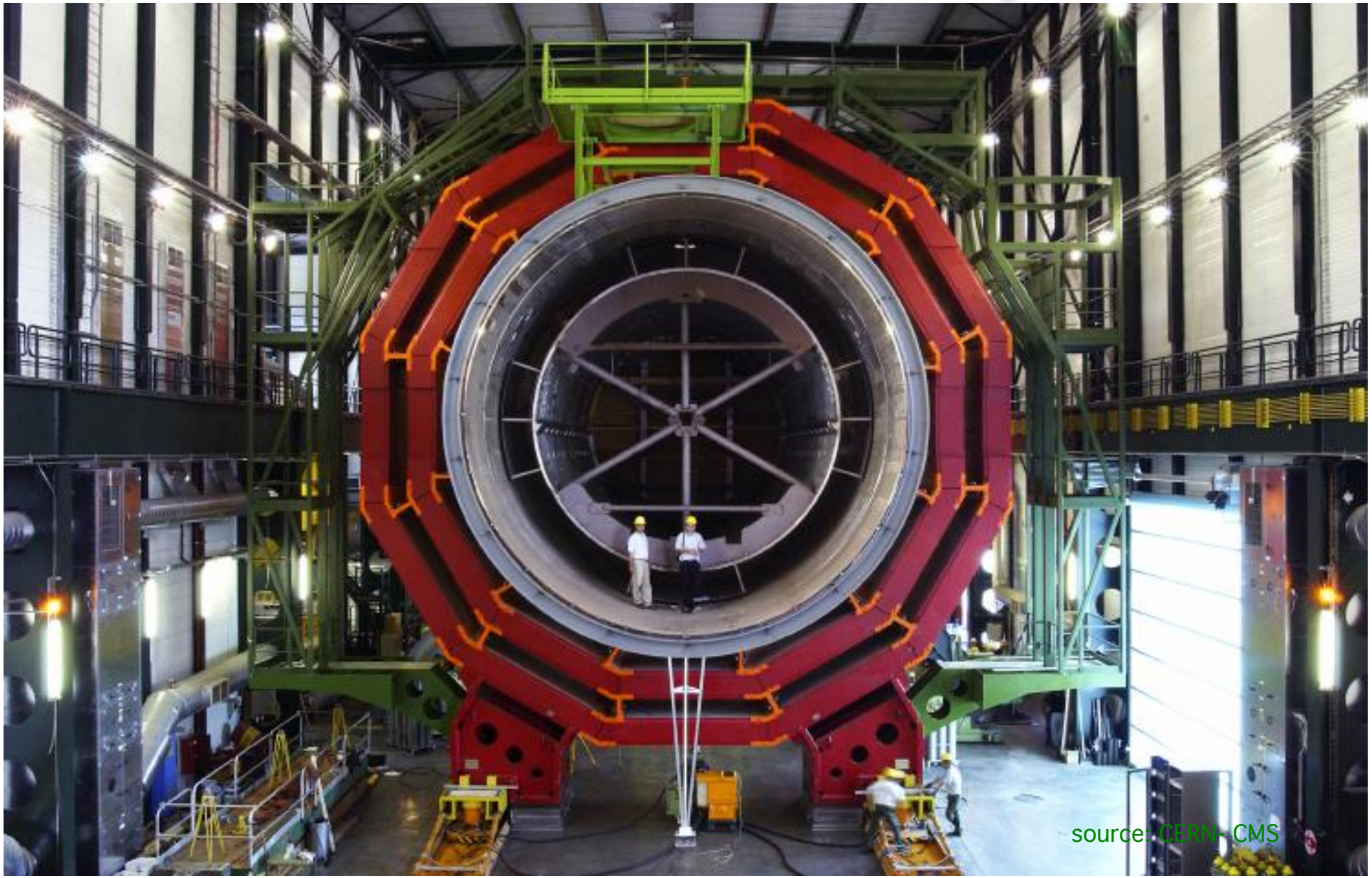
Nikhef Amsterdam
Erik.Heijne@cern.ch



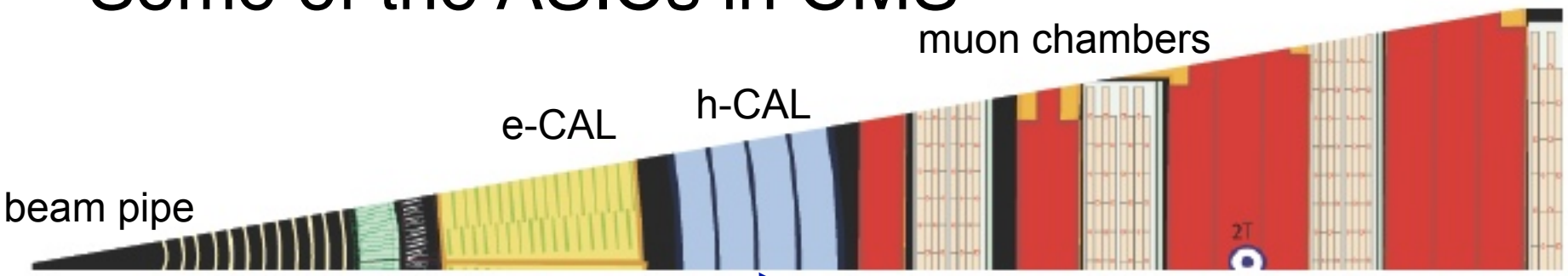




Experiment is Giant 'Camera' with Magnetic Field

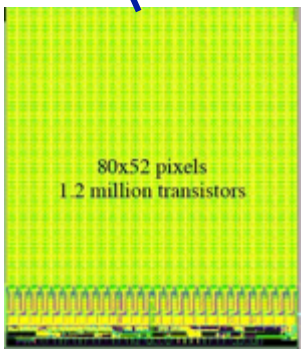


Some of the ASICs in CMS

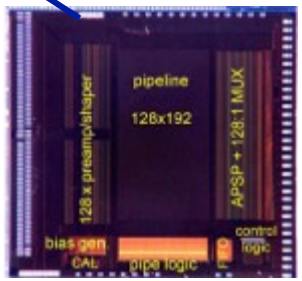


Si strip tracker

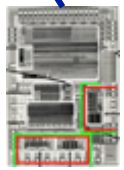
pixel detector



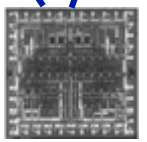
PSI46 pix det
16 800 chips
66 M segments
1 m^2 Si sensor



APV25 Si det
110 000 chips
9.3 M segments
198 m^2 Si sensor



QIE8 calorimeter
220 400 chips



MAD muon det
181 000 chips
25 000 m^2 gas-filled

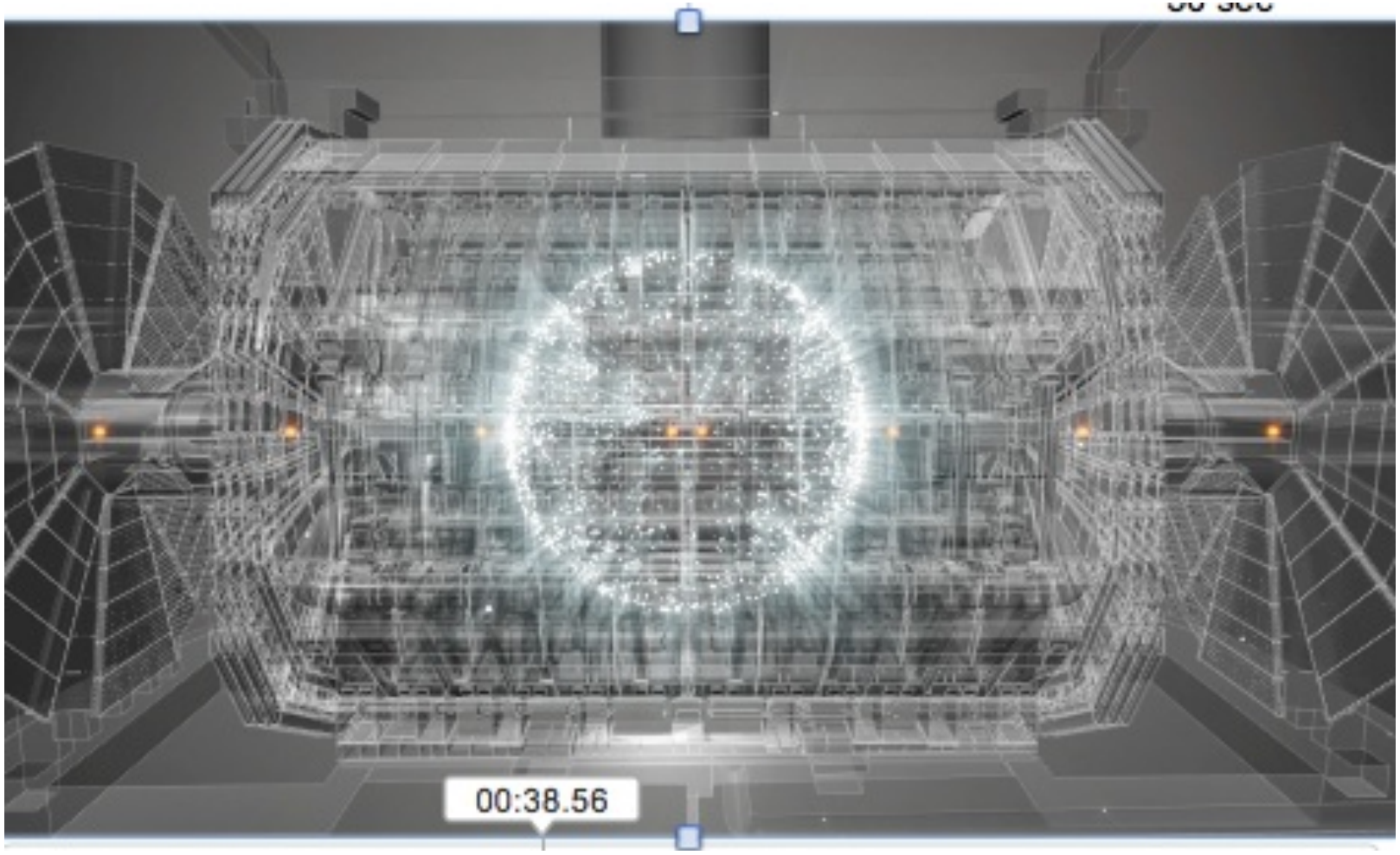
Chips to scale 1 cm

Total CMS
appr. 1 million chips
700 000 ASICs

Animation of Bunch Crossings and Timing

screenshot

~70 sec



source: CERN

Chip design for CERN experiments

Highly segmented sensors essential

- increasing particle multiplicity
- Si lithography provides μm precision
- multiple chains ampli-discri/ADC-SRAM-logic

Radiation hardness needed

- rare good events impose high rates
- 10^7 crossings/s x 100 collisions x 10^7 s/year

Start of radhard studies ~1980 NRL, LETI, Sandia, ..
Serious design efforts from 1986 + IMEC/INVOMEC

Our approach for experiments at CERN

Understand details of our environment

TID, displacements, SEE, (flash?) ...

Understand effects on sensors and chips

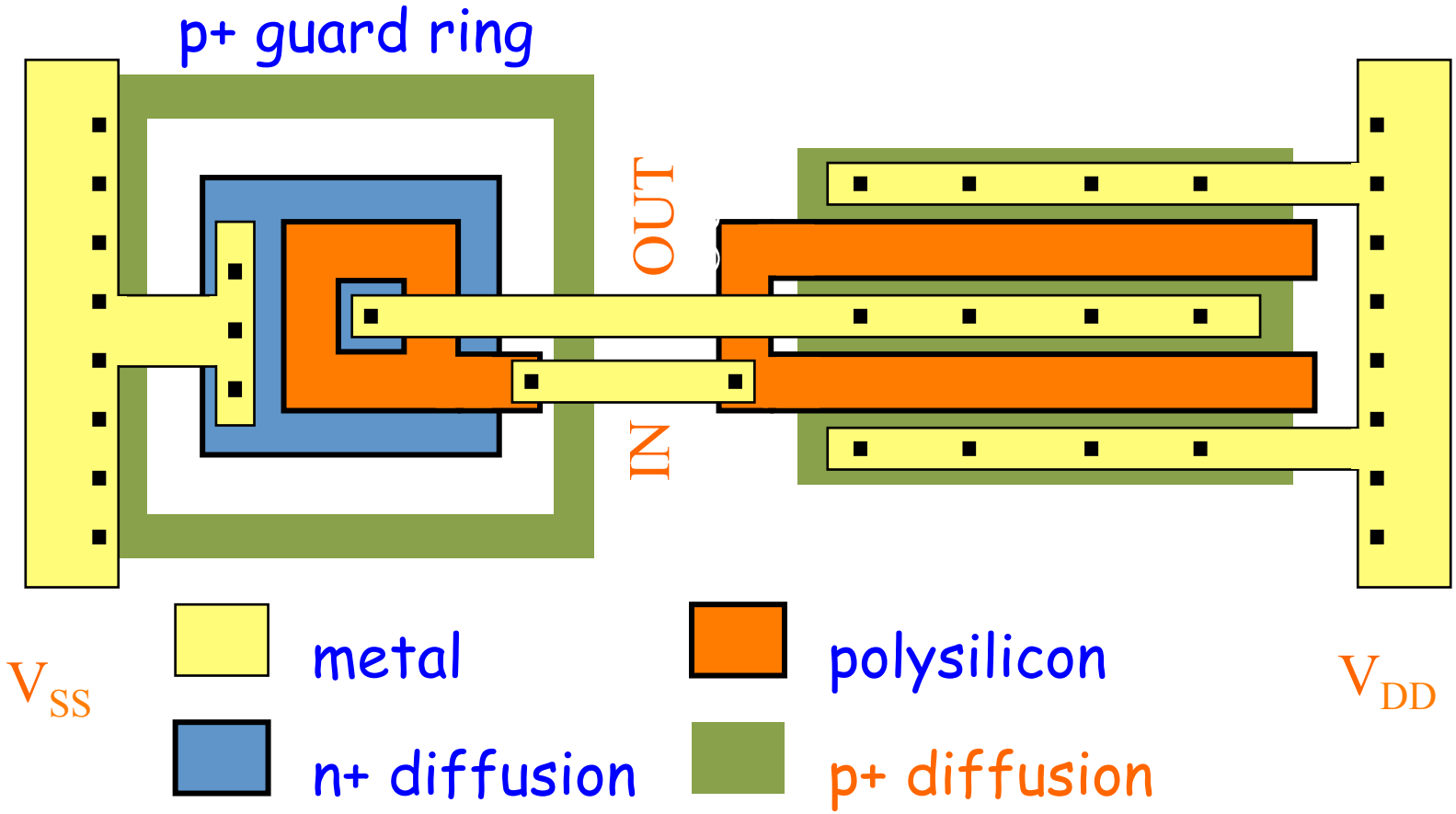
leakage currents, threshold shift, gain,..
instruments, test-chips, irradiation facilities,..

Find implementation to achieve radhard

standard CMOS
need >10Mrad

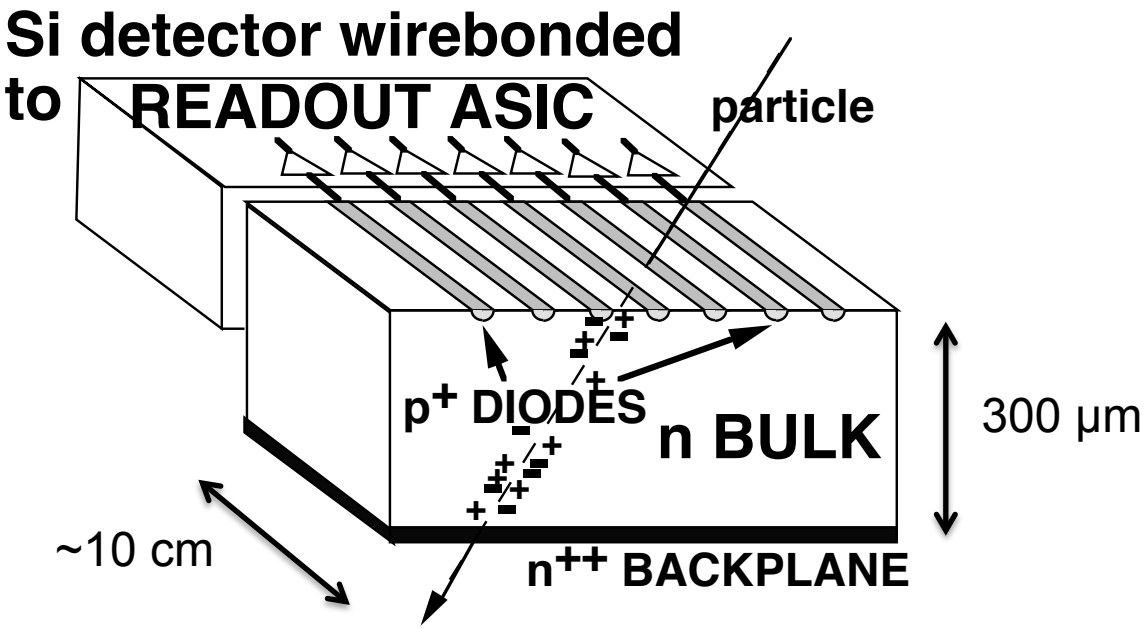
Evaluate samples in realistic test situations

Enclosed n-Transistor is Radiation Tolerant



need to study physics of radiation effects in devices

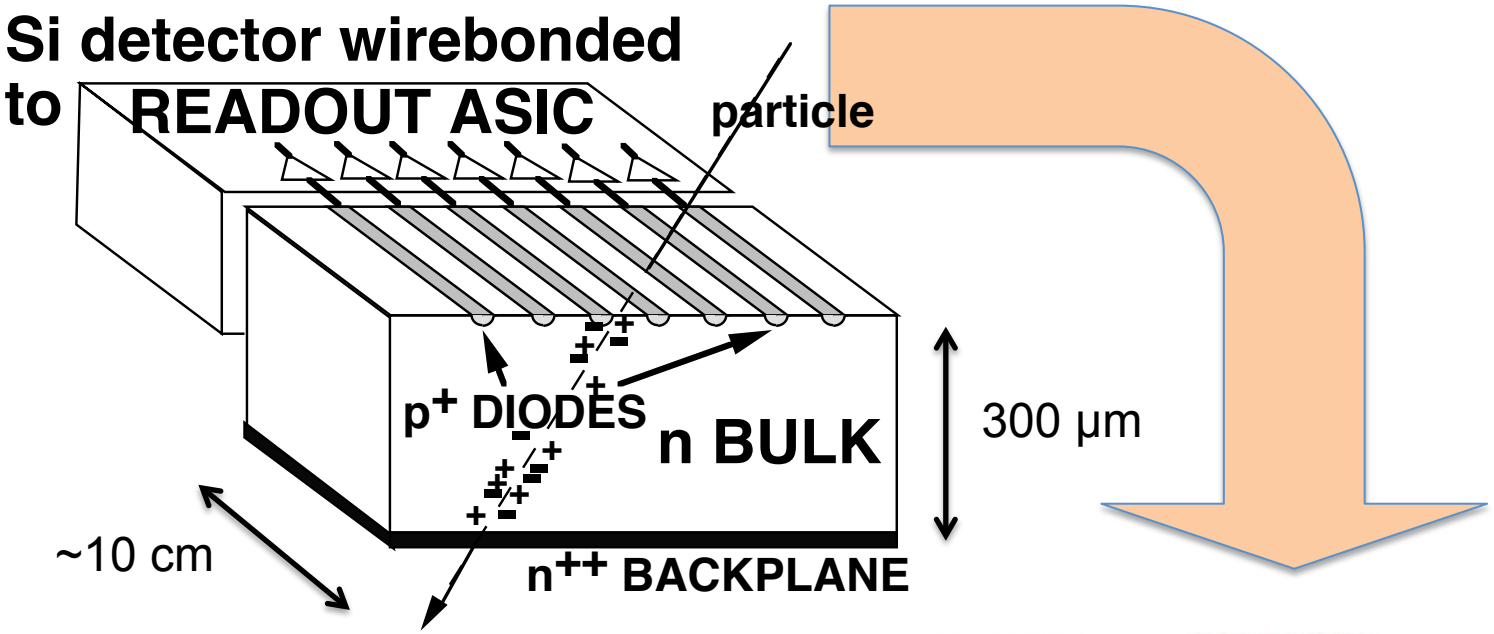
Si Sensors and CMOS Chips



Fully depleted Si Sensor
divided in parallel strips:
“Microstrip Detector”

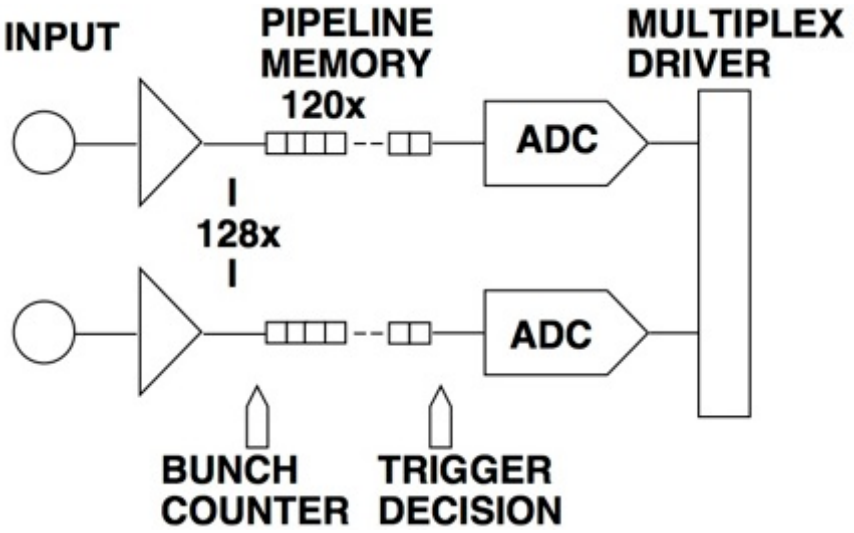
Individual readout chain
for each segment
Signal ~20 000 e-h pairs

Si Sensors and CMOS Chips



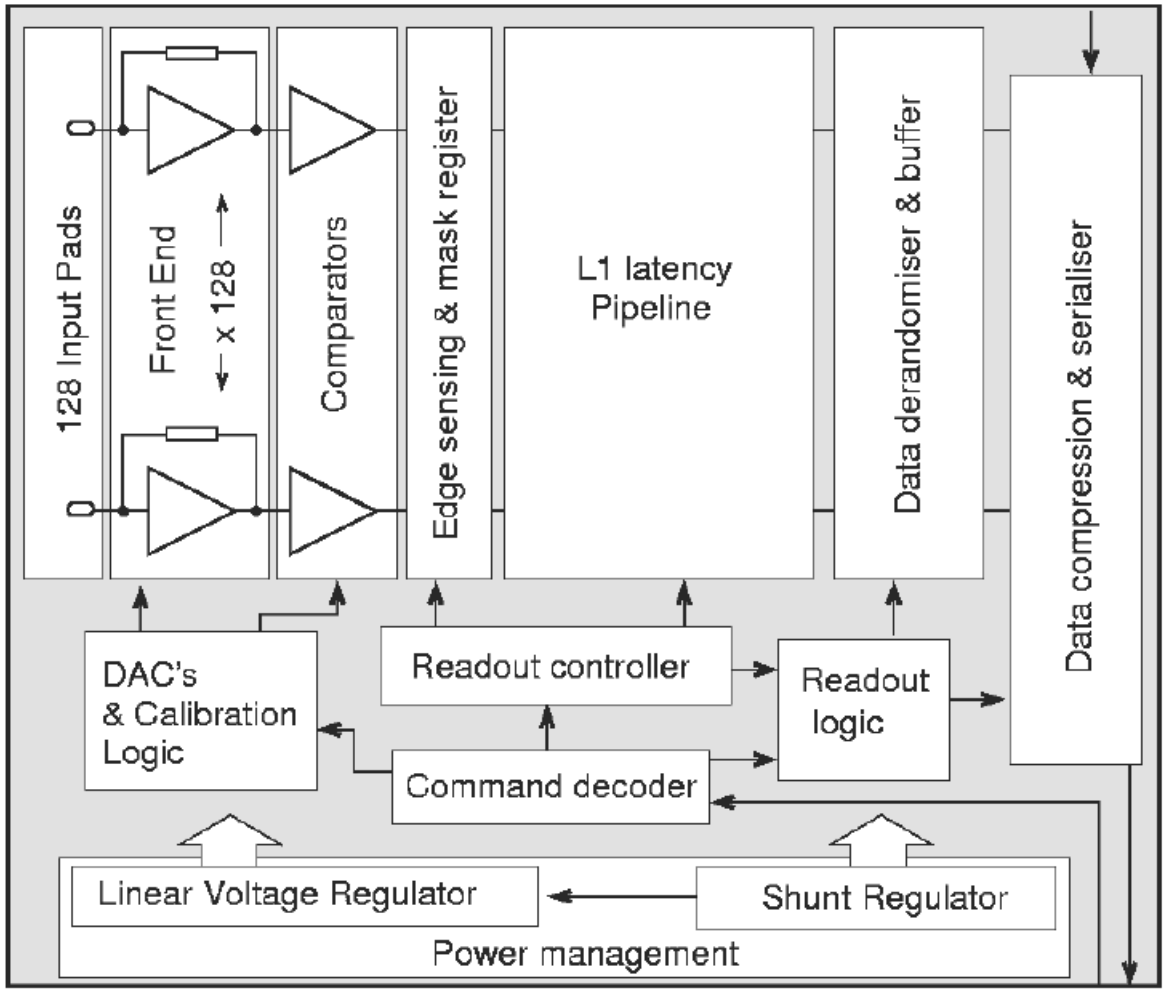
Fully depleted Si Sensor divided in parallel strips: "Microstrip Detector"

Individual readout chain for each segment
Signal ~20 000 e-h pairs



ATLAS Si Detector Readout ABCN25

Example

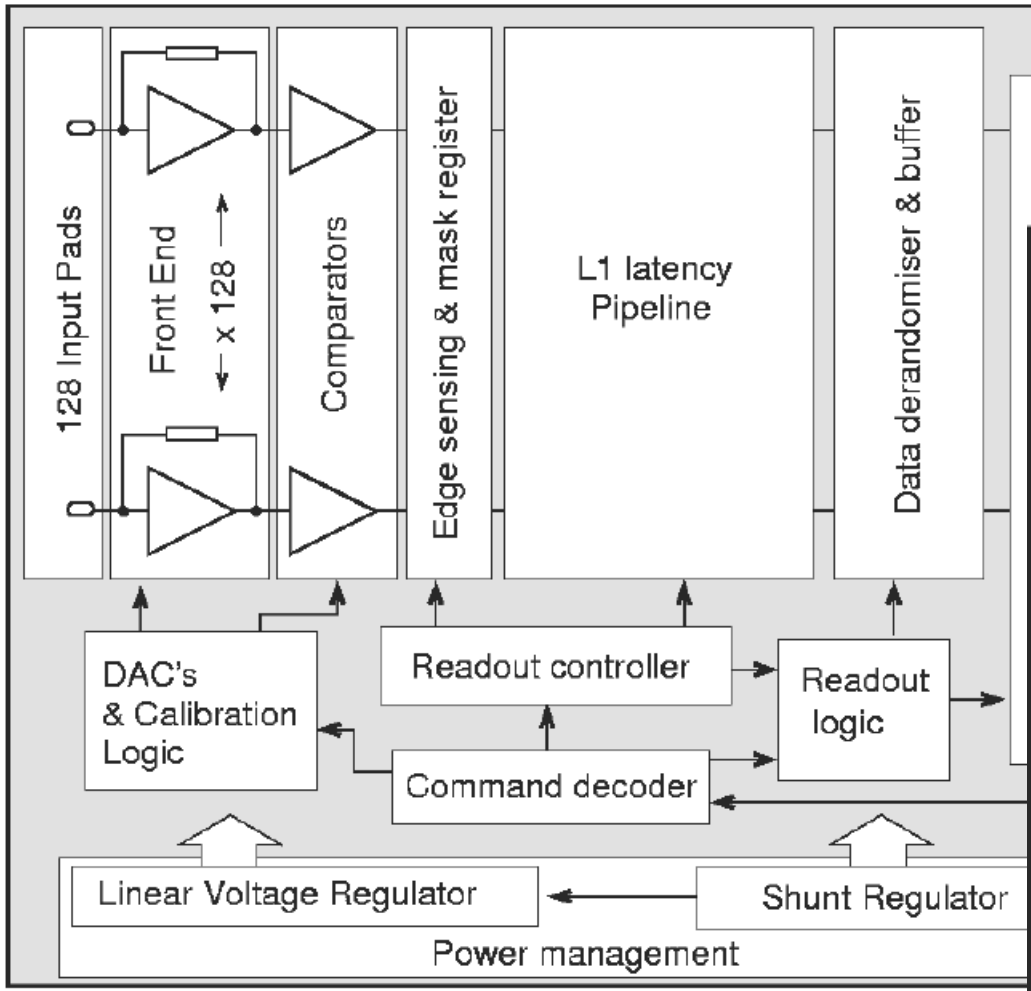


128 parallel channels
Amplifier + Comparator

Binary Pipeline Memory

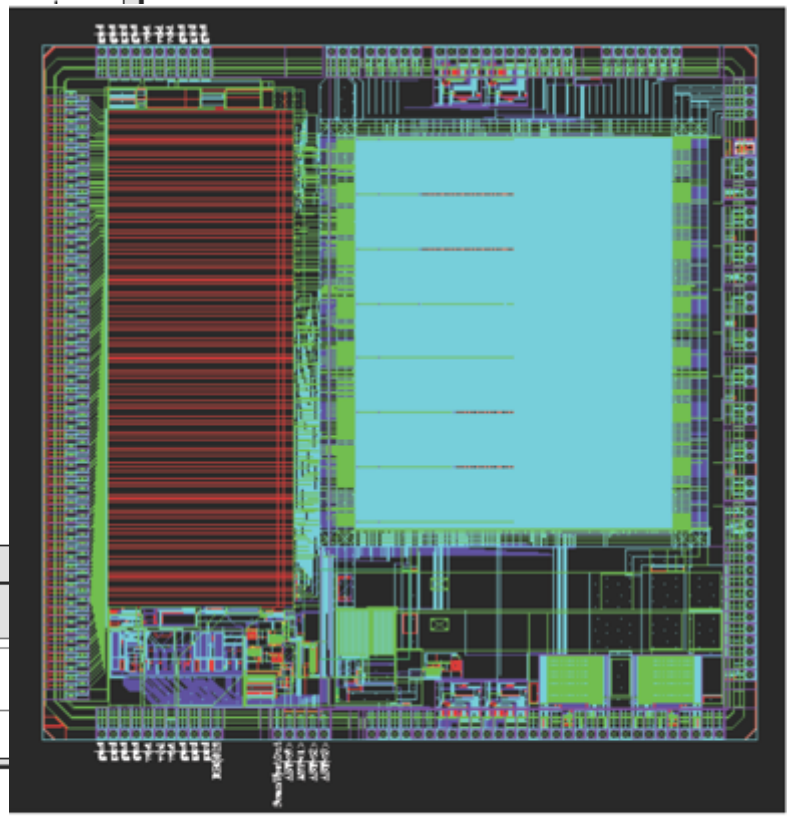
ATLAS Si Detector Readout ABCN130

Example



128 parallel channels
Amplifier + Comparator

Binary Pipeline Memory

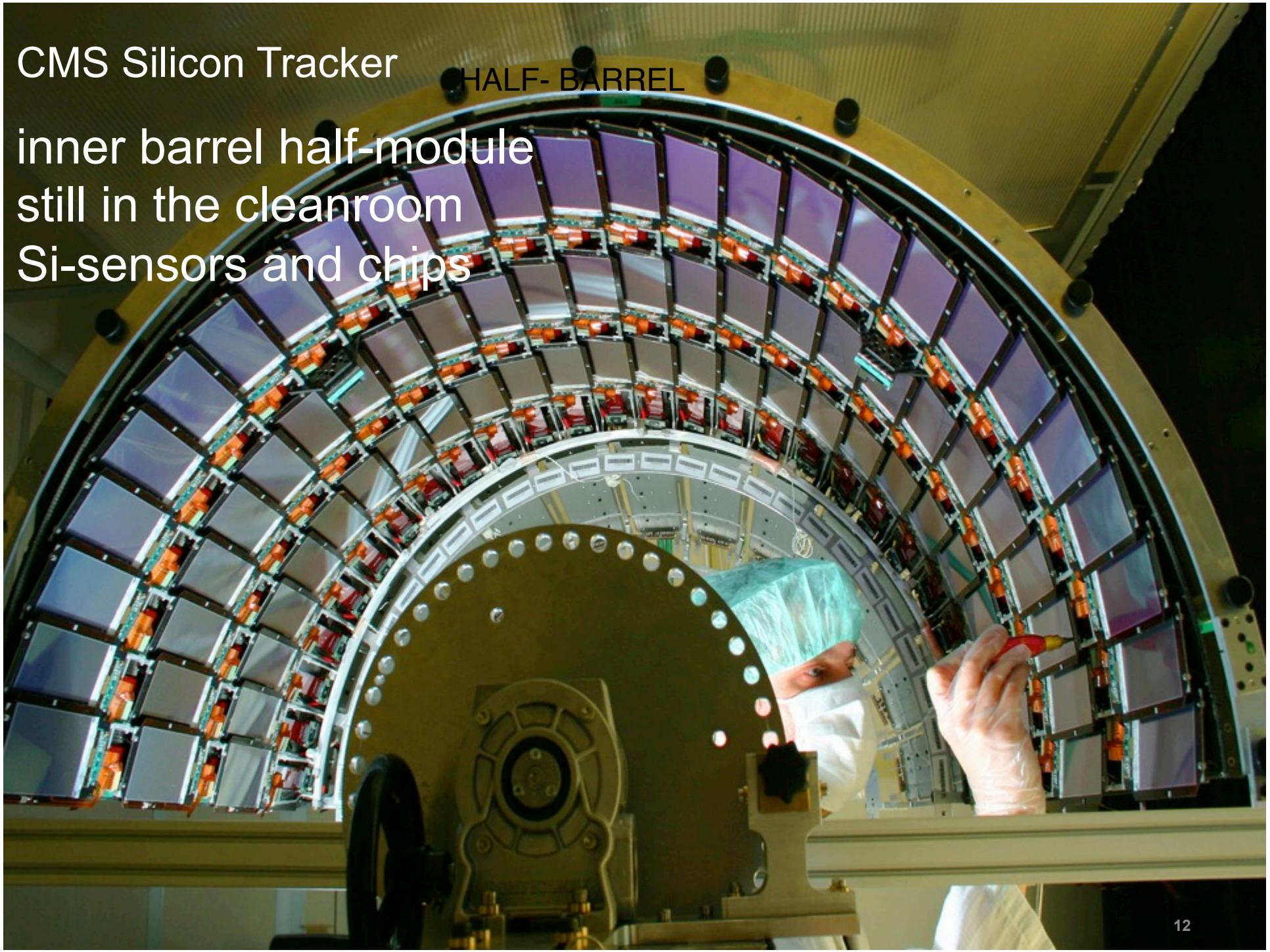


7.7 x 7.5 mm^2 0.5W

CMS Silicon Tracker

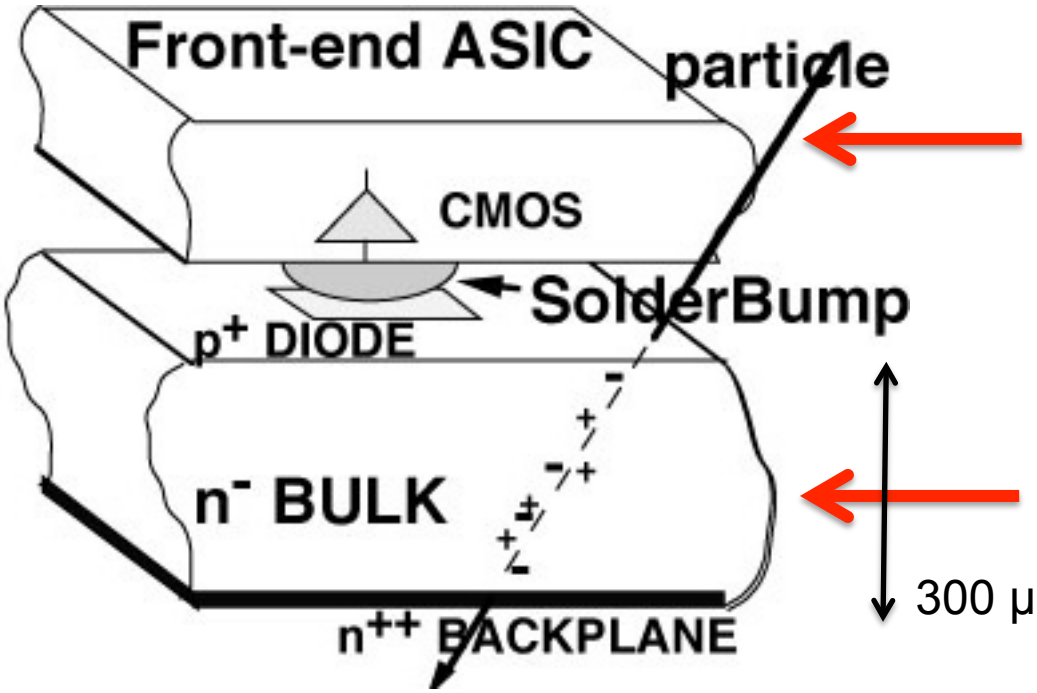
HALF- BARREL

inner barrel half-module
still in the cleanroom
Si-sensors and chips



Hybrid Pixel Detectors

critical development for inner layers
high precision, high rate capability



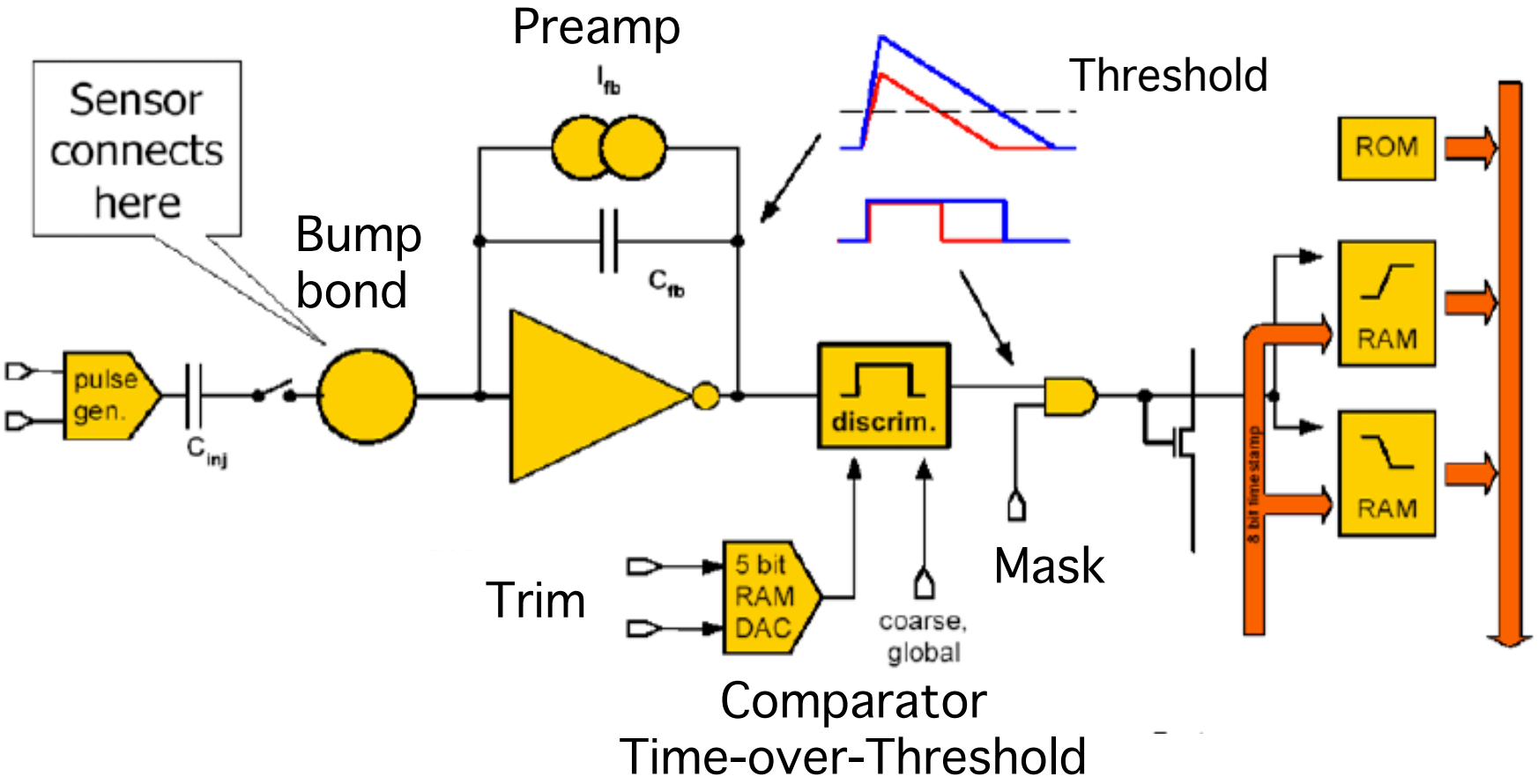
Readout matrix

Pixel e.g.50μmx50μm
Typical matrix 256x256

Sensor matrix

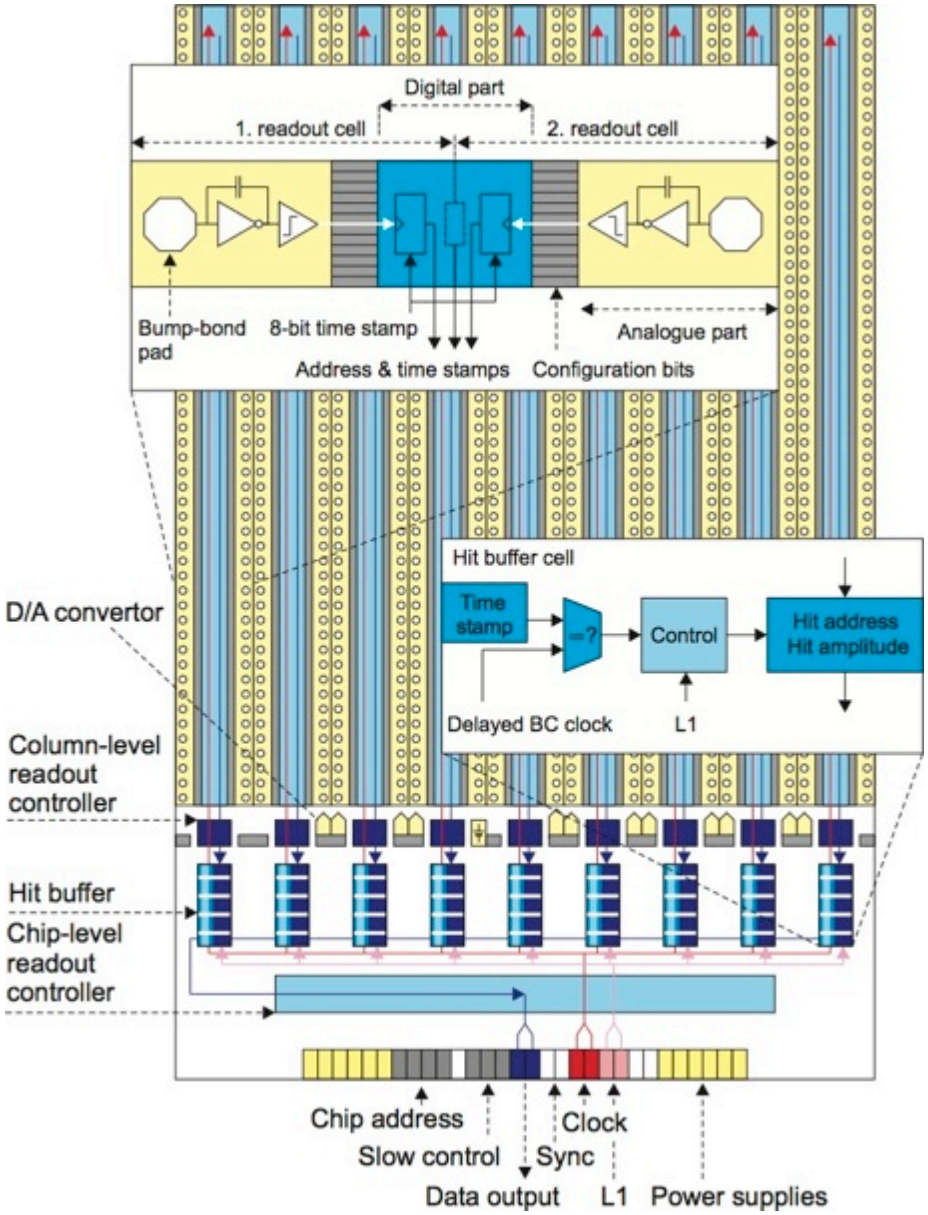
300 µm

Block diagram of circuit in ATLAS pixel imager



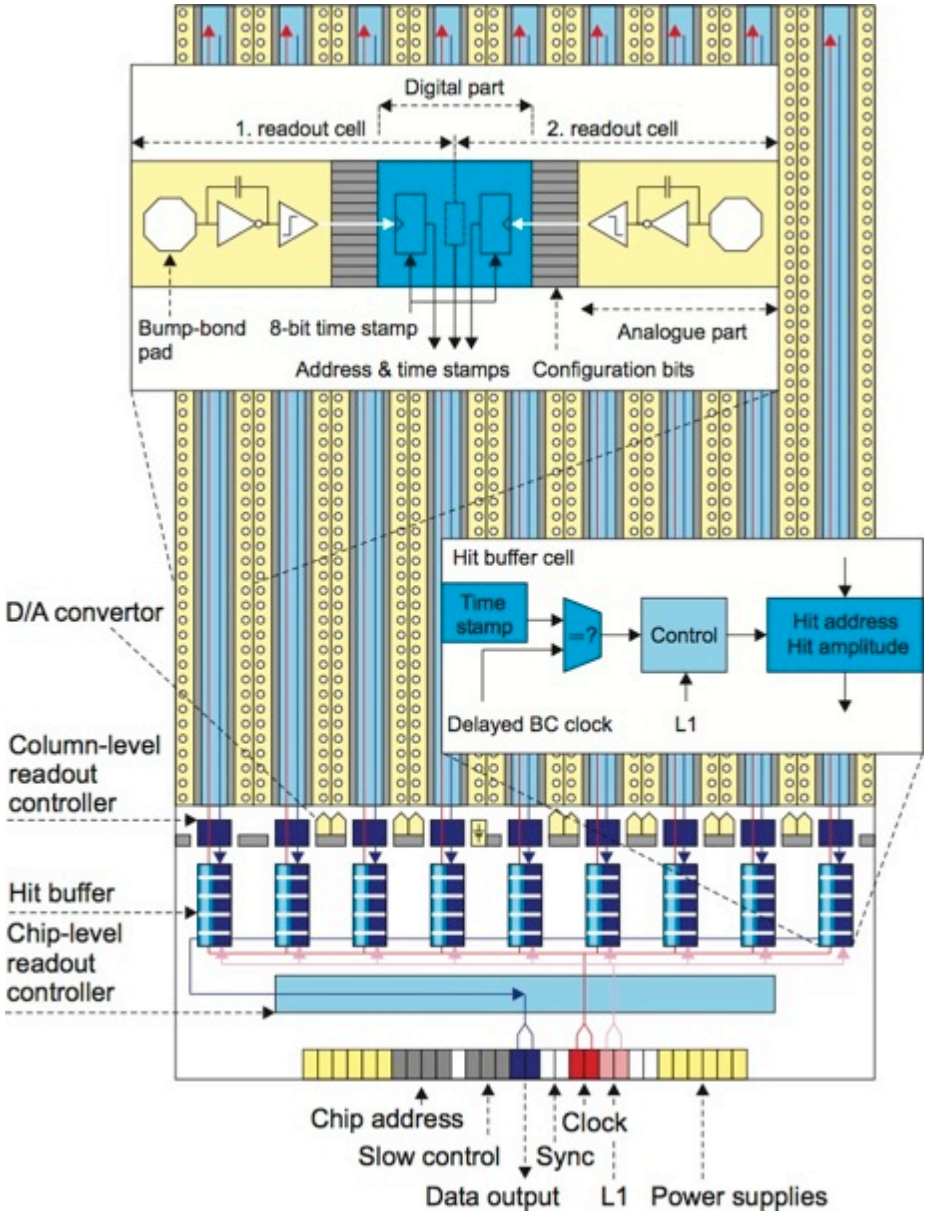
from Garcia, LBNL Berkeley

Pixel-readout chip “FE-I3” in ATLAS



18 x 160 pixels of 50μmx400μm

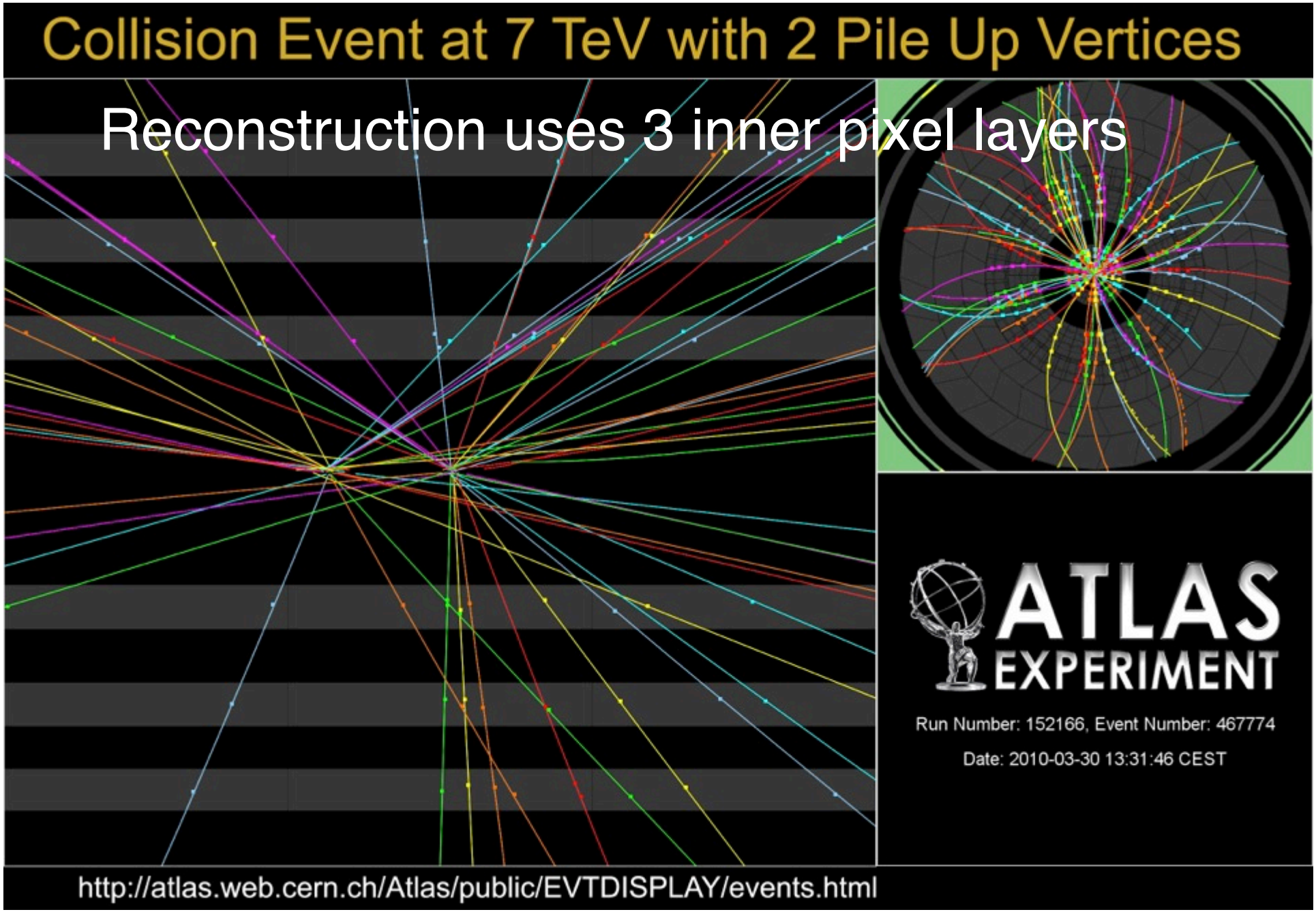
Pixel-readout chip “FE-I3” in ATLAS



11 mm

7.4 mm
18 x 160 pixels of 50μmx400μm

ATLAS Inner Si Pixel Layer


Collision Event at 7 TeV with 2 Pile Up Vertices
Reconstruction uses 3 inner pixel layers
ATLAS
EXPERIMENT
Run Number: 152166, Event Number: 467774
Date: 2010-03-30 13:31:46 CEST
http://atlas.web.cern.ch/Atlas/public/EVTDISPLAY/events.html

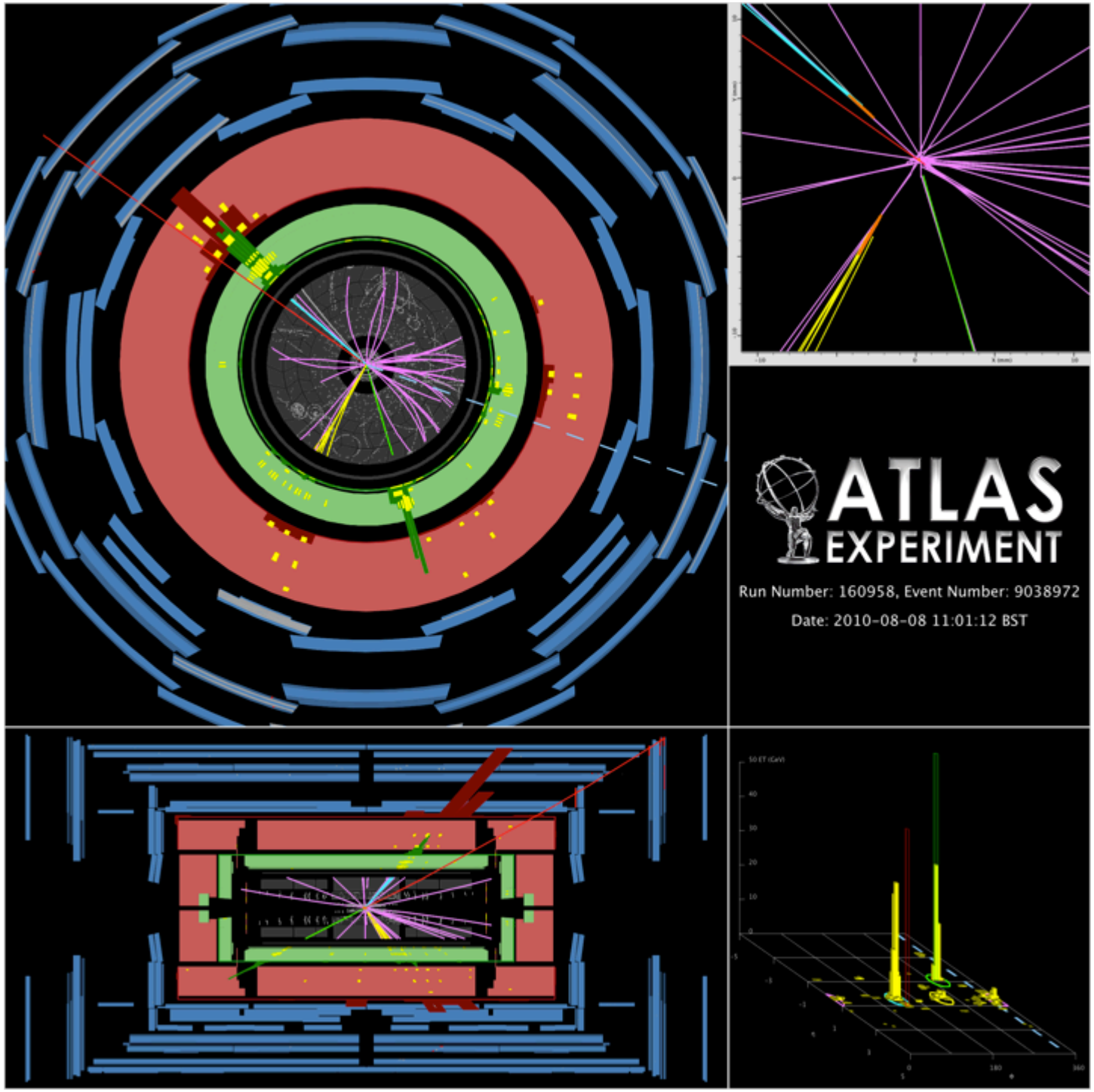
2011 LHC
Imaging now
All Electronic
2 views

Many Tracks
and 2 “Jets”

40 million / sec

Secondary
Vertices:
indicate
short-lifetime
particles

see blow-up

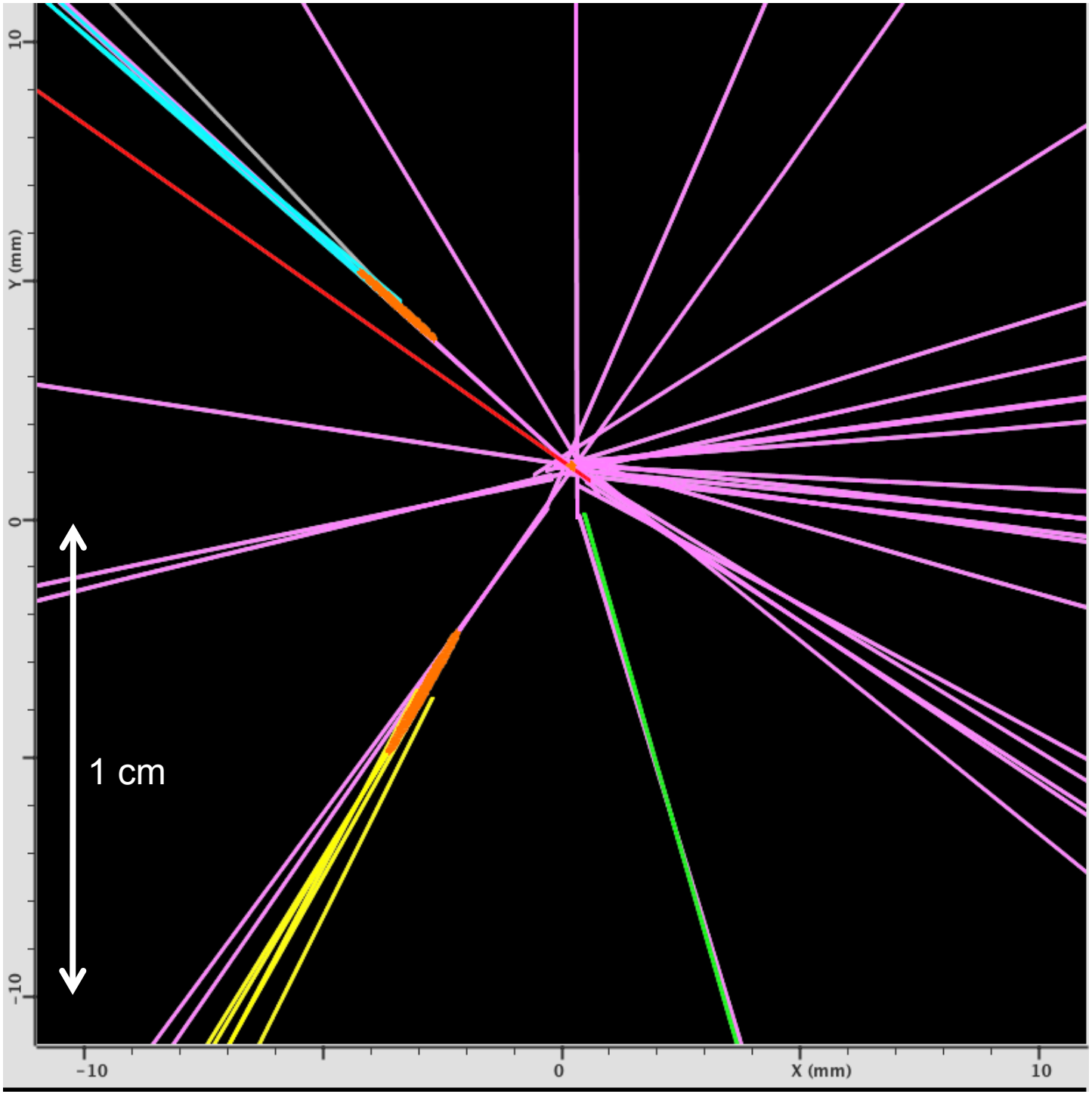


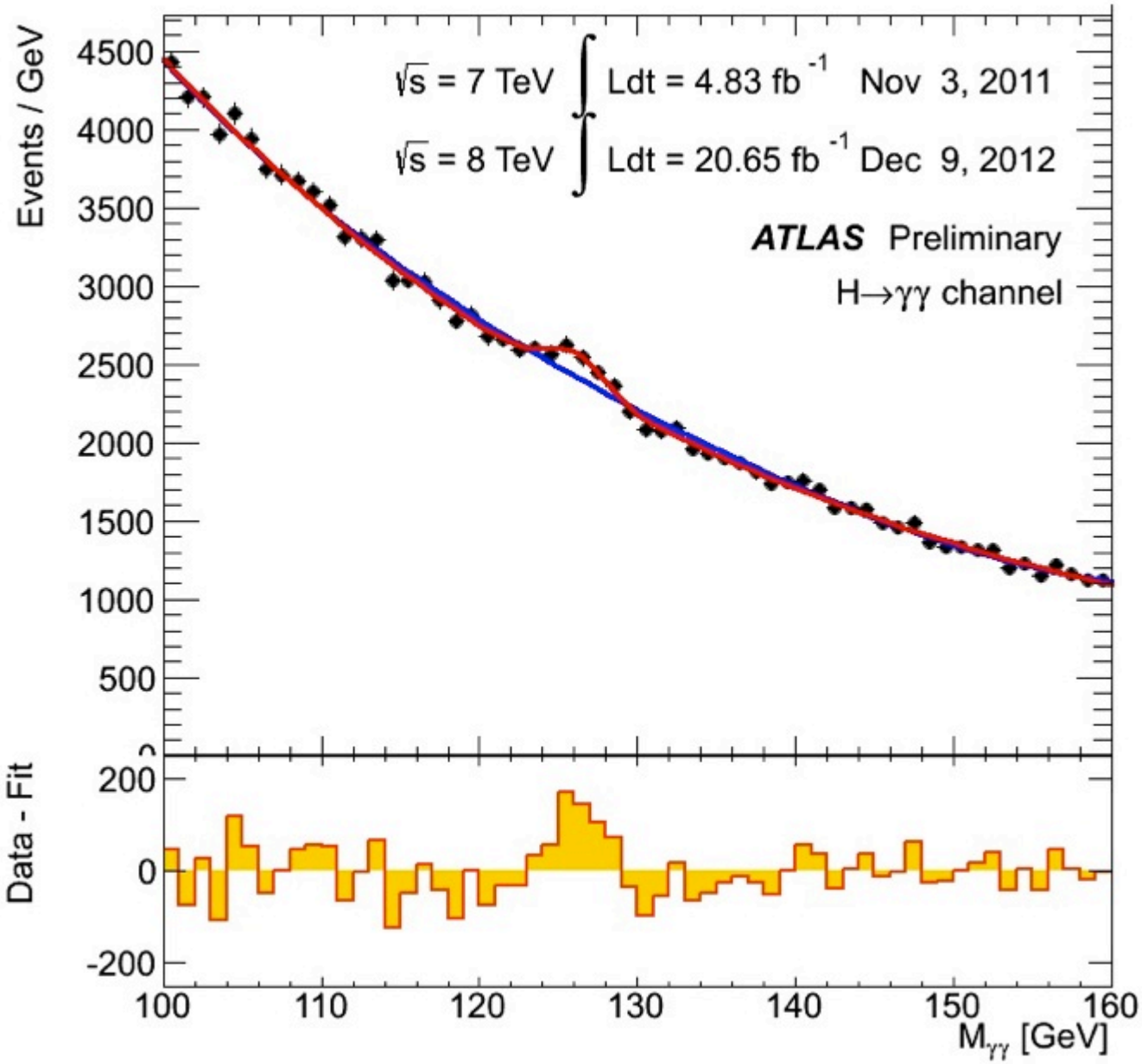
ATLAS

Details around Primary Vertex

Secondary Vertices with reconstruction uncertainty ellipses (orange)

Note the 1cm scale: all this is INSIDE beam pipe





ATLAS

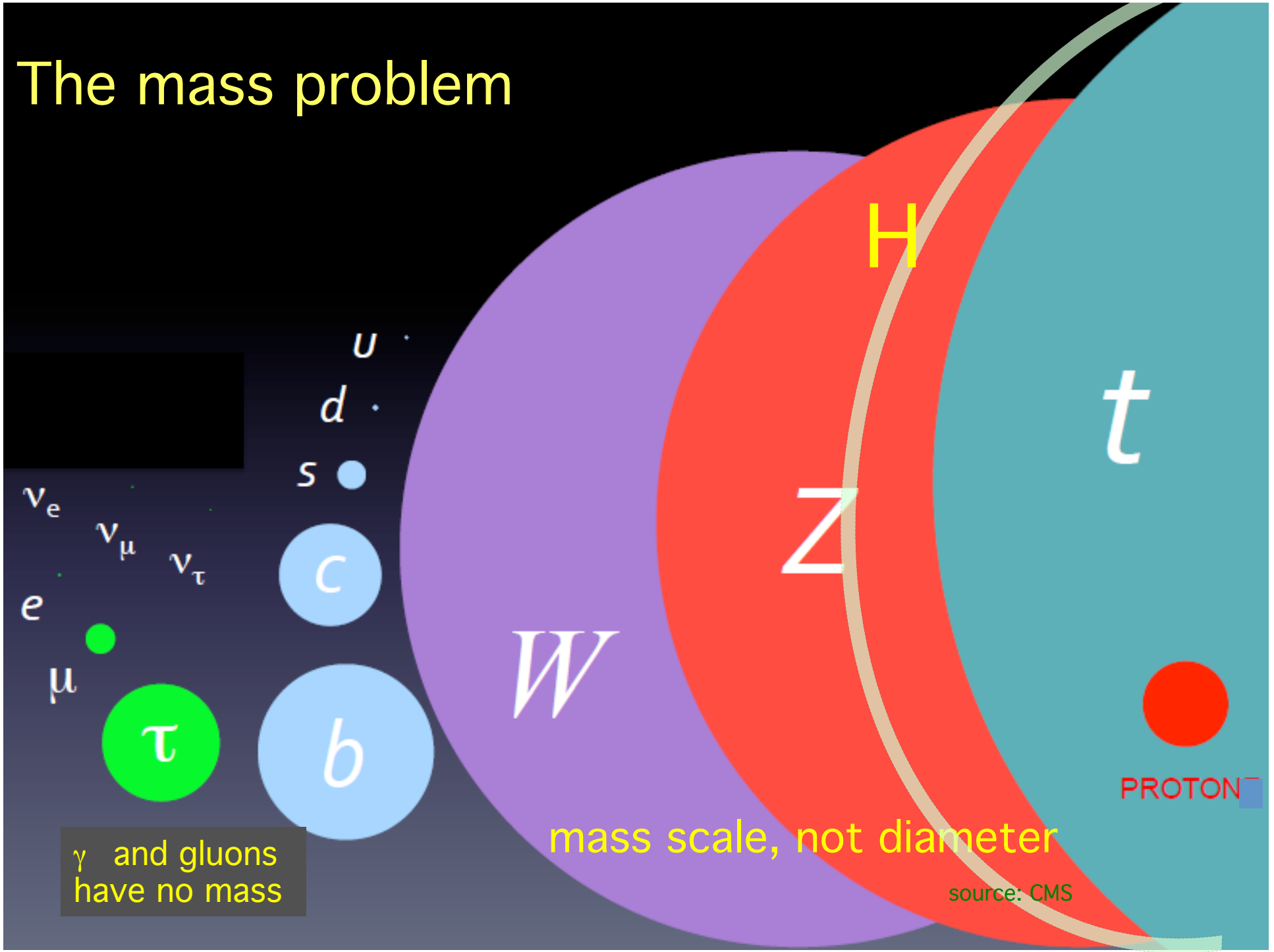
All “events” with
2 energetic photons
emerging from the
primary vertex

Ordered by sum of
measured energy
in GeV of all
decay products
in each interaction

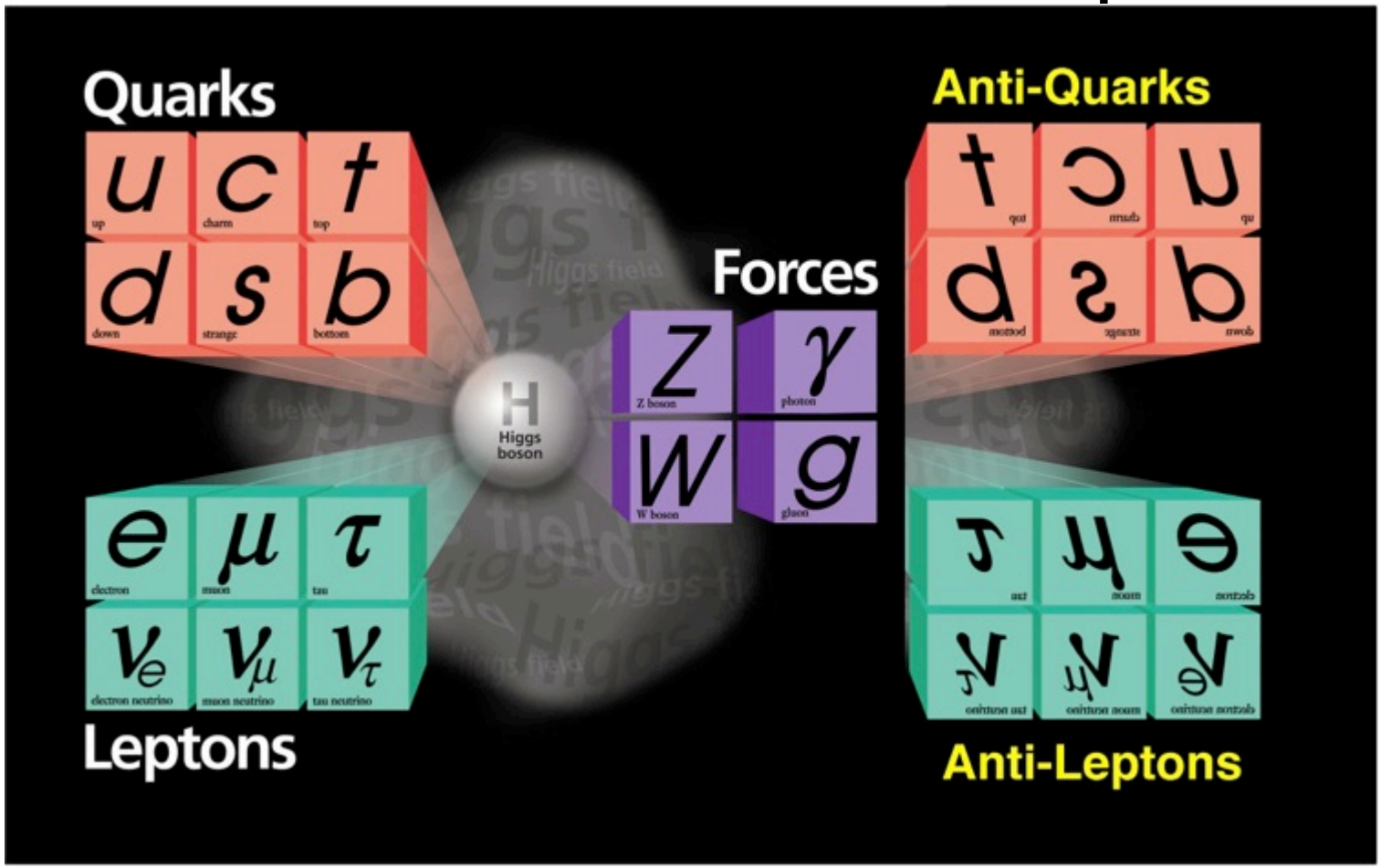
An excess of events
is observed around
126 GeV

just OK at
4 July 2012

The mass problem



A new Periodic Table is complete



Many questions remain:

- why 3 generations
- where are the original antiparticles
- why are masses so different
- .....

THE END

Some History

Earliest PMOS chip for particle physics: LETI ~1977

Mead-Conway revolution: can we have own chips on MPW?

1984 Sherwood Parker/Terry Walker at Stanford:
Microplex switched capacitor feedback

1987 Pierre Jarron/Erik Heijne
Amplex continuous feedback with dark current compensation

1990 several groups start similar projects

2000→now
chips become primary focus of experiment design

Evolution in on-chip data storage

~1985 parallel-serial CCD analog pipeline

1992 analog storage on feedback capacitors

1999 analog storage on memory bank:
"APV25" installed in CMS

2002 comparator first, binary storage
iteration "ABCD" actually installed in ATLAS

2005 SRAM allows variable retention times

2014 more input channels
more digital processing

Chain of Data Processing and Filters