CENTRE NATIONAL D'ÉTUDES SPATIALES

A Thales / Finmeccanica Company

Design and test of MROD, a 2 Channels Video Chain Mixed-Signal ASIC for High Resolution Mission

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Thales Alenia Space France

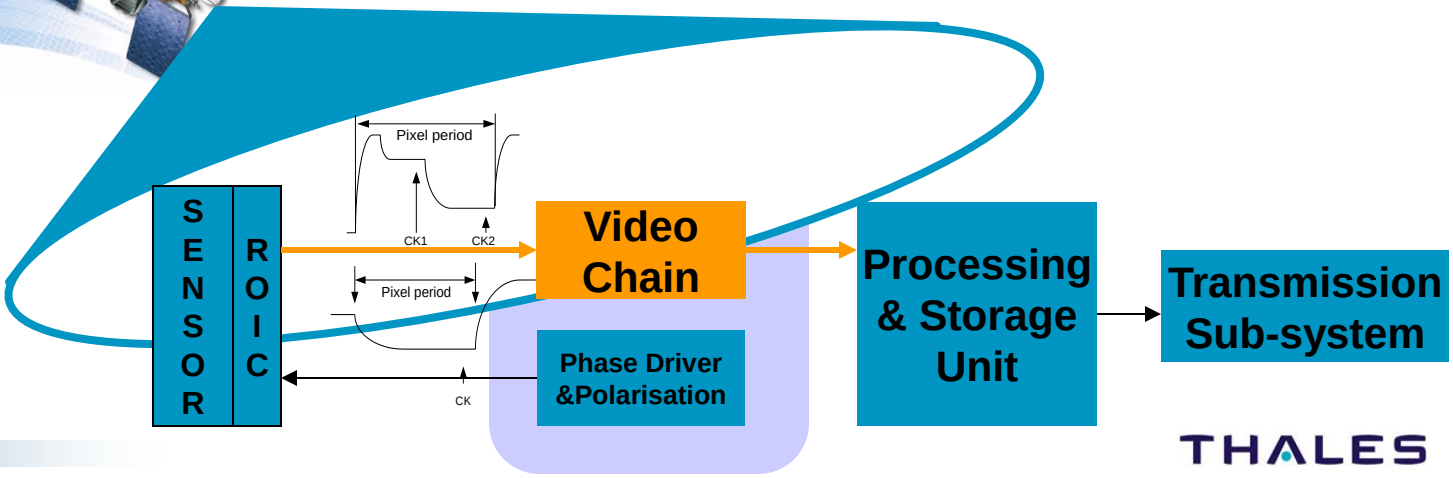
THALES

Agenda

- ✓ Project context, objectives and organization
- ✓ Technology Selection
- ✓ Methodology and design tools
- ✓ MROD Architecture and Design
- ✓ MROD prototype manufacturing
- ✓ MROD preliminary performances
- ✓ Electrical test results
- ✓ Radiation tests
- ✓ Conclusion

Optical satellite instruments for High Resolution Earth observation:

- Wide use of Charge Coupled Devices and CMOS Active Pixel Sensors
- Need for a specific conditionning of the analog signals from the read-out circuits before processing and storage
  - Amplification & Correlated Double Sampling
  - Analog to digital conversion
- Challenging constraints
  - Noise reduction, Sensitivity, power dissipation
  - Extreme Temperature, Radiations, Life-time
  - ⇒ **Increase the level of integration !**

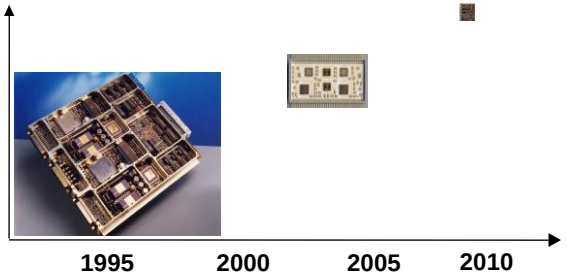


Project Objectives

Existing off-the-shelf components do not meet all the performances and environment requirements…

Benefit from CMOS low power technology to:

- Allow high integration
- Improve radiometric performance
- Optimise power budget



Answer to future space mission needs by making available a chip at the highest standards of the state-of-the art integrated CCD processors.

⇒ **Competitive process initiated by CNES in the frame of « CMOS video chain for CCD and/or APS » Action de R&T : R-CS1/09-0025**

- Granted to Thales Alenia Space
- Development of the mixed ASIC MROD demonstrator

⇒ **MROD candidat for OTOS mission and futur High Resolution observation based on CCD or CMOS.**

Project organisation

THALES ALENIA SPACE France

- MROD Specification
- Mixed ASIC design and Verification
- Functional and radiometric test bench
- Functional tests
- Radiometric tests

Sub-Contractor

- Radiation test bench
- Radiation tests

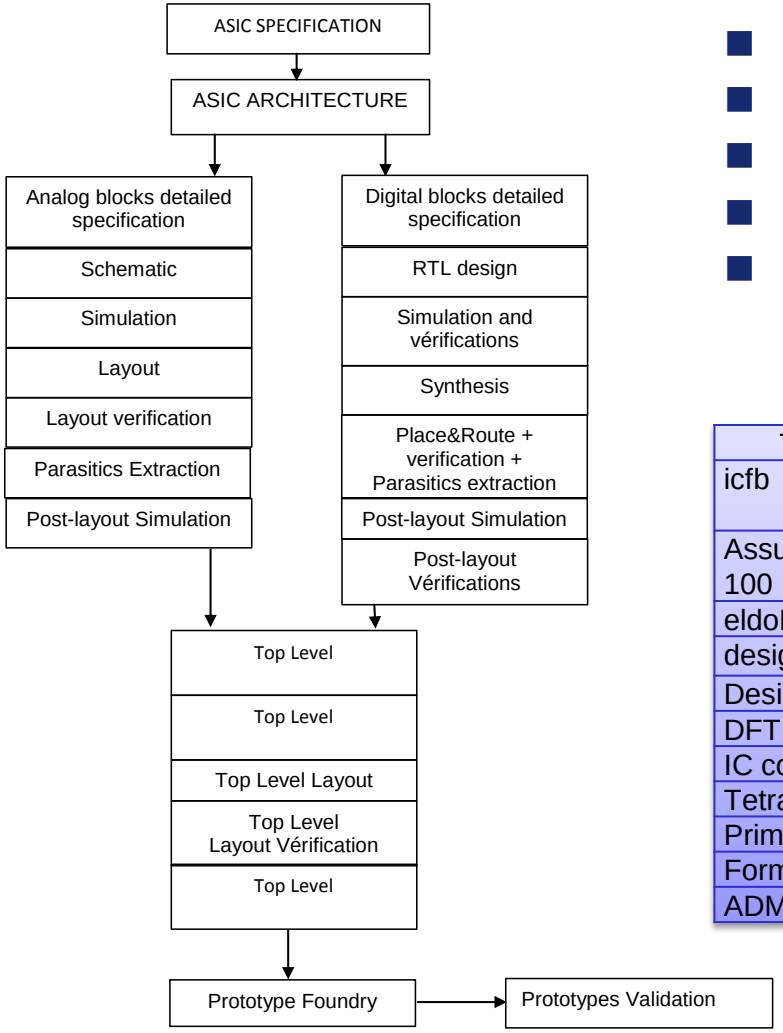
Technology selection

- **Using a wide set of weighted criterion :**

	weight
Technical characteristics	3
Space Environment	3
Design Kit and models	3
Accessibility	2
High reliability Back-End	2
Low Cost prototyping	1

- **Final selection :**
  - **XFAB XH035 : BiCMOS 0.35µm.**
  - **Large experience with this technology (test vehicles, PAHTRS, VASP, …)**

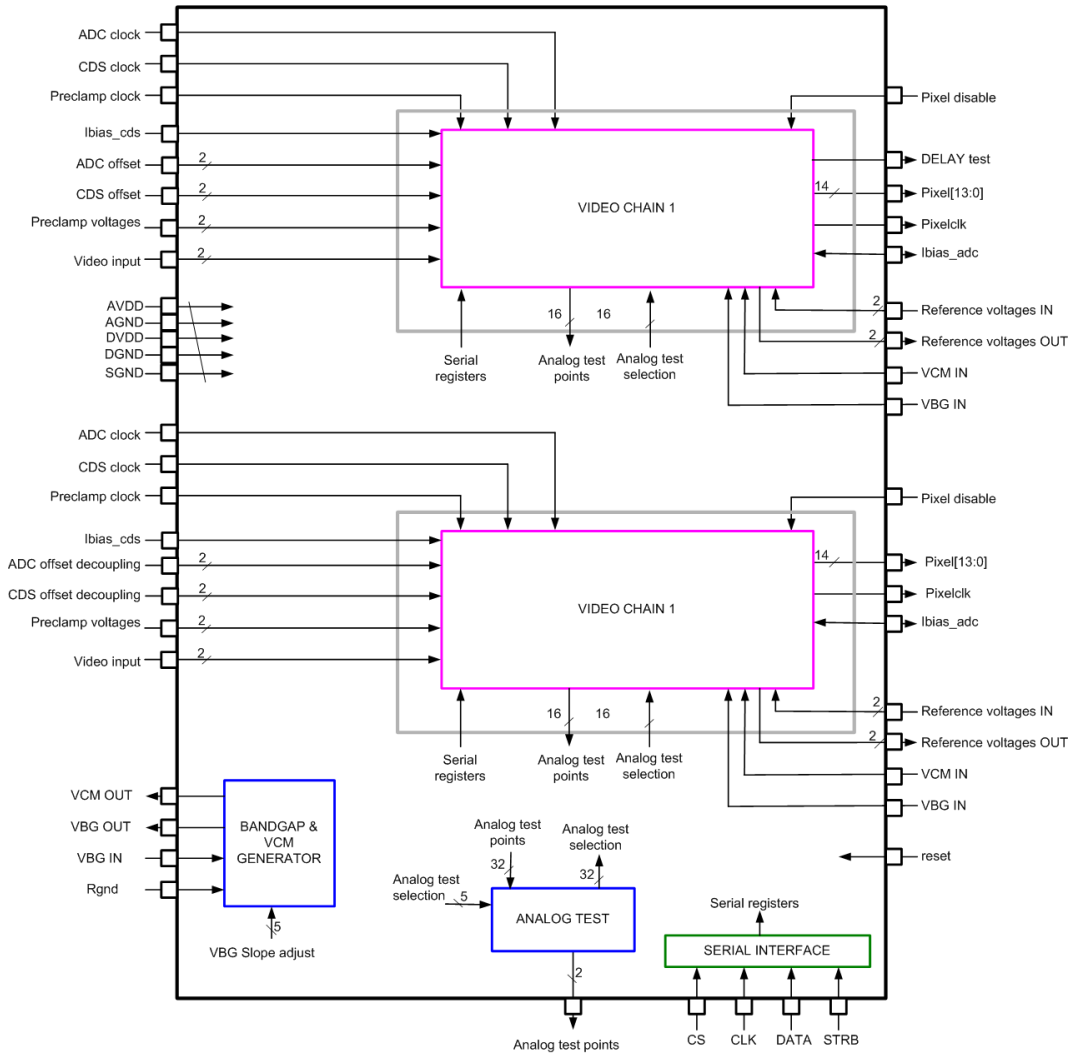
Methodology and design tools



- **Mixed Analog and Digital flow**
- **State-of-the Art Tools**
- **Methodology Based on ECSS-Q-ST-60-02 C**
- **Hardening by design: TID, SEL, SEU and SET**
- **Digital cells from proprietary hardened digital library**

Tool name	Vendor	Version	Comments
icfb	Cadence	V6.1.3.500.19	Schematic and layout suite
Assura & QRCX 100	Cadence	v04.10.001	DRC, LVS, extrcation
eldoD	Mentor	v11.1	Analog simulation
design kit	XFAB	ps035_03	
Design Compiler	Synopsys		Logic synthesis
DFT compiler	Synopsys		Scan insertion
IC compiler	Synopsys		Place and Route
Tetramax	Synopsys		ATPG generator
Prime time	Synopsys		Static Timing Analysis
Formal Pro	Mentor		Formal Proof
ADMS Questa	Mentor	v11.1	Mixed simulation

MROD Architecture



- 2 independent video channels with CCD and CMOS capability
- BANDGAP and VCM voltages generation
- Serial interface for configuration
- Analog test interface

MROD Architecture

Video channel features :

- Preclamp
- CDS + PGA (gain 8/8 to 8/1)
- ADC 14 bits
- 1V±20% Reference voltage generator on 8 bits for fine gain tuning
- CDS coarse offset DAC on 8 bits
- ADC offset DAC : coarse on 6 bits, fine on 10 bits
- Reference and offset voltage buffers
- Programmable delay on CDS and ADC clocks
- VIDEO INTERFACE with SDR and DDR capability

MROD Design

Technology :

XFAB XH035

CMOS 0.35µm

Chip :

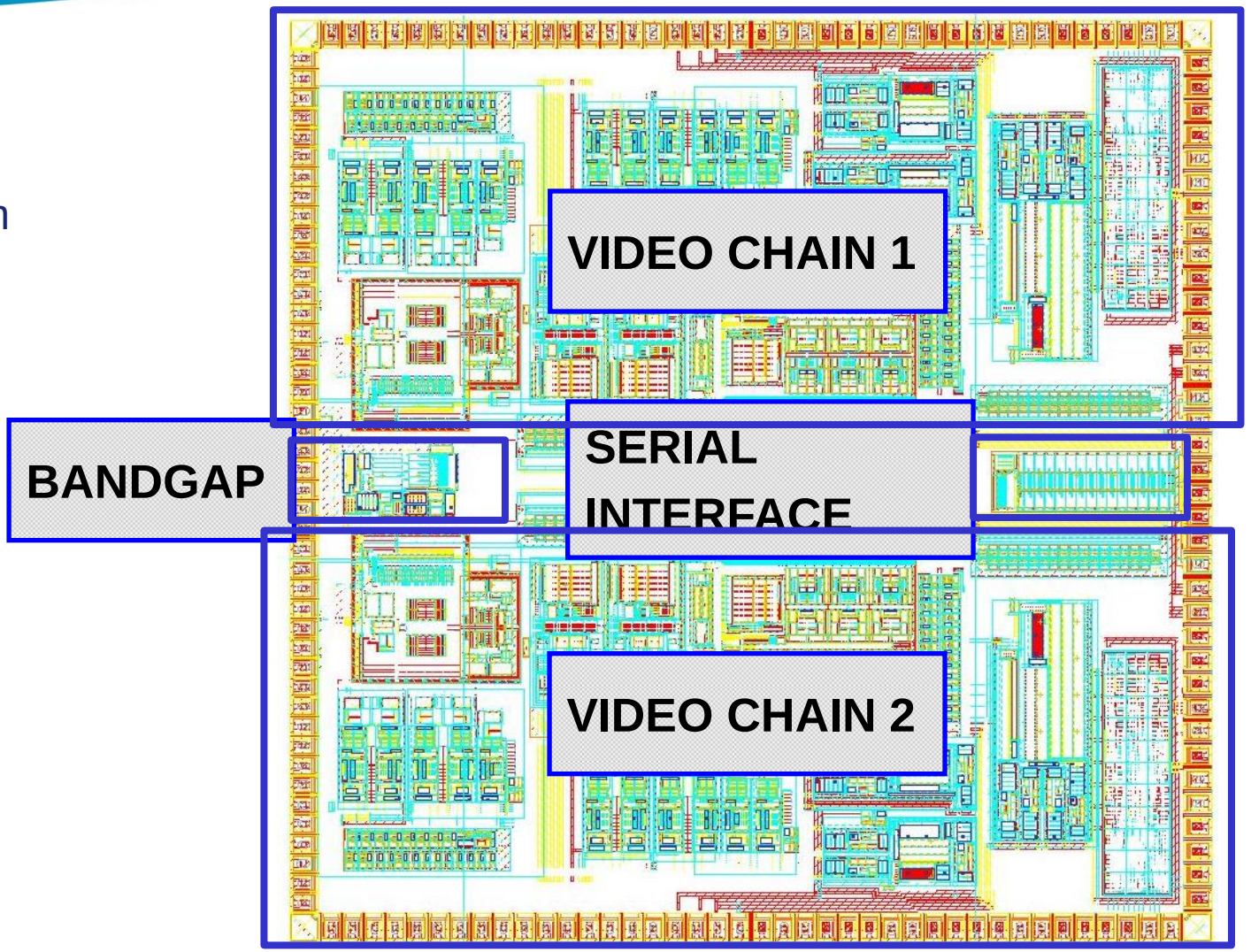
9mm X 9mm

81mm²

160 IOs

Digital :

2x1.5 mm²



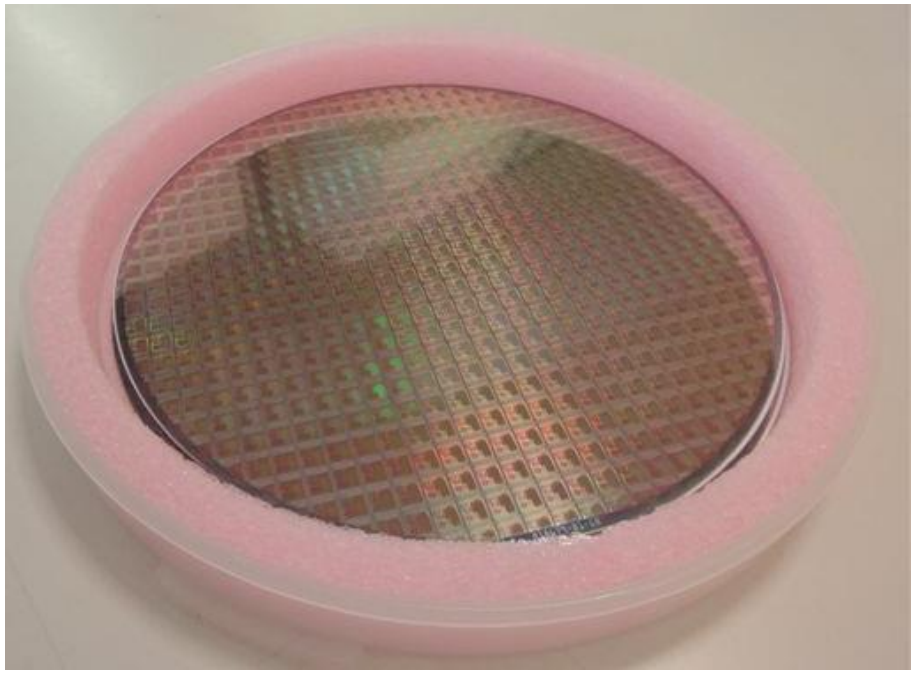
MROD prototype manufacturing

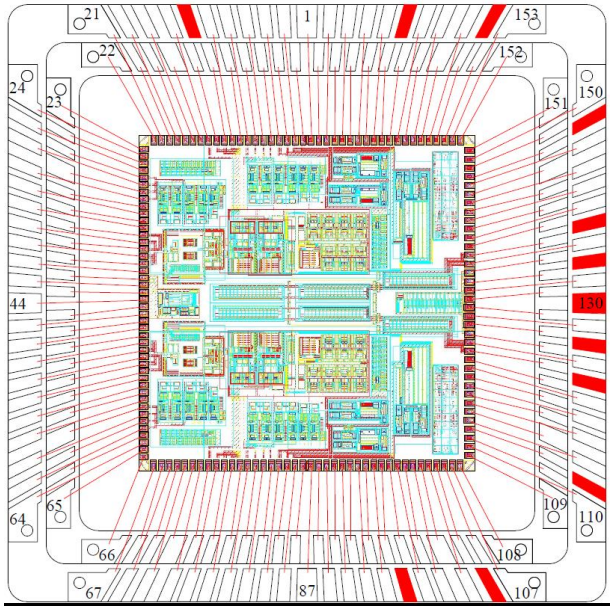
Foundry :

- XFAB
- MLM, 3 X 8'' wafers

Packaging :

- MICROSS
- CQFP 172





MROD preliminary performances

Functional features	min	max	comment
Video Channel	0	2	Power shut down capability
CDS	CCD	CMOS	video signal input
Video signals	Diff	Pseudo diff	
CDS Gain x1 à x4	x1	x4	fine tuning ±20% range through VREF. x8 available
ADC	14 bits		with 12 bits performances goal
Output code	SDR on 14 bits	DDR on 7 bits	
Differential input range	2xVref		at gain x1
Clock delay programming	0ns	30ns	Step ~1ns
Multi sampling per pixel			
Preclamp			For CCD DC suppression
CDS coarse offset range	-0.5V	+0.5V	Differential on 8 bits
ADC coarse offset range	-0.25V	+0.25V	Differential on 6 bits
ADC fine offset range	-62.5mV	+62.5mV	Differential on 10 bits
Serial interface		10MHz	Shift registers with strobe

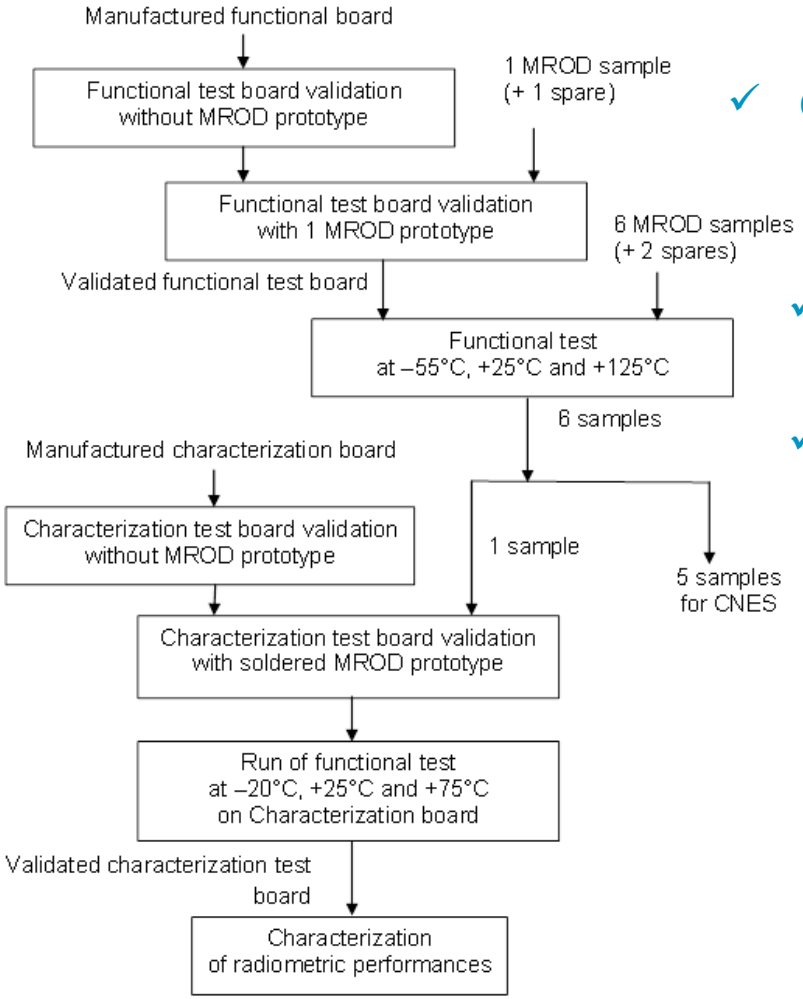
MROD preliminary performances

Radiometric performances	min	max	comment
Pixel frequency	1MHz	12MHz	in worst case
DNL	±0.5 $LSB_{12\ bits}$		Typical at gain x1 (measured on functional test bench)
INL	±2$LSB_{12\ bits}$		
CDS + ADC noise	0.7 lsb_{12bits}		
ADC ONLY	0.4 lsb_{12bits}		
Video level saturation recovery		1 pixel	
Consumption ADC ONLY	275mW		Typical per channel @ 12MHz
Consumption CDS + ADC / CCD	415 mW		

Environment	min	max	comment
Junction temperature	-55°C to	+125°C	
Performances temperature	-20°C	+75°C	
Radiation tolerant up to 100krad		100krad	
Latchup immunity		70 MeV.cm²/m	
SEU			DICE flip-flop

Electrical test results

Validation plan



✓ **done**

✓ **done**

✓ **Done at ambient temperature on 5 parts, 100% functional coverage.**

✓ **Temperature tests on-going**

✓ **Board under manufacturing**

Electrical test results

22 functional tests :

Test Name	Test Number	Sampling frequency		Temperature		
		1MHz	12MHz	-55°C	ambient	+125°C
State during reset	TEST # 01xxx			X	X	X
State after reset	TEST # 02xxx			X	X	X
Serial interface	TEST # 03xxx	X		X	X	X
Access to internal analog test points	TEST # 04xxx	X			X	
Bandgap temperature slope trimming range	TEST # 05xxx	X		X	X	X
VCM trimming range	TEST # 06xxx	X		X	X	X
Reference voltages trimming range	TEST # 07xxx	X		X	X	X
Biasing current	TEST # 08xxx	X		X	X	X
ADC ONLY mode with CMOS differential signal	TEST # 09xxx	X	X	X	X	X
CDS+ADC mode with CMOS signal	TEST # 10xxx	X	X	X	X	X
CDS+ADC mode with CMOS signal and DDR	TEST # 11xxx	X	X	X	X	X
CDS+ADC mode with CCD signal	TEST # 12xxx	X	X	X	X	X
CDS gain	TEST # 13xxx	X	X	X	X	X
CDS coarse offset range and resolution	TEST # 14xxx	X		X	X	X
ADC coarse offset range and resolution	TEST # 15xxx	X		X	X	X
ADC fine offset range and resolution	TEST # 16xxx	X		X	X	X
Preclamp switches impedance	TEST # 17xxx			X	X	X
ADC clock delay programming	TEST # 18xxx	X		X	X	X
CDS clock delay programming	TEST # 19xxx	X		X	X	X
PIXEL clock delay	TEST # 20xxx	X		X	X	X
Multi sampling	TEST # 21xxx		X		X	
Pixel disable	TEST # 22xxx	X		X	X	X

Electrical test results

13 radiometric tests :

Test Name	Test Number	Supply	Sampling frequency	Temperature		
		±5%	1MHz 12MHz 15MHz 17MHz 19MHz	-20°C	ambient	+75°C
Bandgap temperature slope trimming	TEST # 30xxx			X	X	X
Noise	TEST # 31xxx	X	X	X	X	X
Linearity	TEST # 32xxx	X	X	X	X	X
Linearity with alternate white and black pixel	TEST # 33xxx	X	X	X	X	X
Coupling noise between video channels	TEST # 34xxx	X	X	X	X	X
Pixel saturation recovery	TEST # 35xxx	X	X	X	X	X
CCD synchronous noise rejection	TEST # 36xxx		X	X	X	X
Input common mode rejection ratio	TEST # 37xxx	X	X		X	
Power supply rejection ratio	TEST # 38xxx		X		X	
Serial interface coupling noise with video channel	TEST # 39xxx		X		X	
Input current with DC restore capacitor	TEST # 40xxx		X	X	X	X
CDS offset settling	TEST # 41xxx			X	X	X
ADC offset settling	TEST # 42xxx			X	X	X

Electrical test results

Functional tests synthesis at ambient temperature :

- ✓ **5 MROD prototypes tested at ambient temperature**
- ✓ **100% of the functionalities are validated : no design bug**
- ✓ **100% yield : confirmes XFAB techno performance**

- ✓ **Next slides are illustrating main results :**
  - ✓ ADC ONLY
  - ✓ CDS+ADC
  - ✓ CDS gain
  - ✓ Offsets
  - ✓ Programmable delay

Electrical test results

ADC ONLY :

Close to full scale

				Sampling frequency 1MHz			Sampling frequency 12MHz		
CODE GS :				+25°c			+25°c		
Measured parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
PIXEL_1_FS	13820	15220	lsb	15040	15052	15060	15023	15036	15045
PIXEL_2_FS	13820	15220		15031	15056	15095	15024	15049	15089
Calculated parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
I_CHANNEL_1_FS			mA	62,8	66,0	67,4	79,8	83,4	85,2
I_CHANNEL_2_FS				60,6	64,8	67,9	78,3	82,6	85,6
I_MROD_FS				124,9	132,1	135,9	159,5	167,4	171,4
Idyn_CHANNEL_1_FS			mA/MHz	1,50	1,58	1,63			
Idyn_CHANNEL_2_FS				1,59	1,62	1,66			
Erreur CH1	-1	1	%	-0,6%	-0,6%	-0,5%	-0,5%	-0,5%	-0,4%
Erreur CH2	-1	1	%	-0,9%	-0,6%	-0,4%	-0,8%	-0,6%	-0,4%
Calculated parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
Power dissipation on 3V3			mW	412	436	449	526	552	566

Close to 0

PIECE					Sampling frequency 1MHz			Sampling frequency 12MHz		
CODE GS :					+25°c			+25°c		
TEST number	Measured parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
TEST # 09045	PIXEL_1_LS	365	2365	lsb	1405	1411	1416	1413	1422	1436
TEST # 09046	PIXEL_2_LS	365	2365	lsb	1398	1423	1455	1408	1426	1456
					+25°c			+25°c		
TEST number	Calculated parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
TEST # 09051	I_CHANNEL_1_LS			mA	60,3	63,9	66,0	78,1	81,1	82,5
TEST # 09052	I_CHANNEL_2_LS				60,6	64,7	67,5	78,3	82,6	85,5
TEST # 09053	I_MROD_LS				122,3	130,0	133,0	157,8	165,1	168,7
TEST # 09058	LSB_ERROR_1	-1	1	%	-0,38%	-0,34%	-0,30%	-0,23%	-0,15%	-0,05%
TEST # 09059	LSB_ERROR_2				-0,39%	-0,33%	-0,24%	-0,55%	-0,27%	-0,11%
TEST # 09060	Idyn_CHANNEL_1_LS			mA/MHz	1,39	1,56	1,61			
TEST # 09061	Idyn_CHANNEL_2_LS				1,58	1,63	1,67			
TEST number	Calculated parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
Power dissipation on 3V3				mW	404	429	439	521	545	557

- Less than ±1% error versus theory at 1 and 12MHz
- No significant impact of sampling frequency

CDS + ADC : CMOS signal

Close to full scale

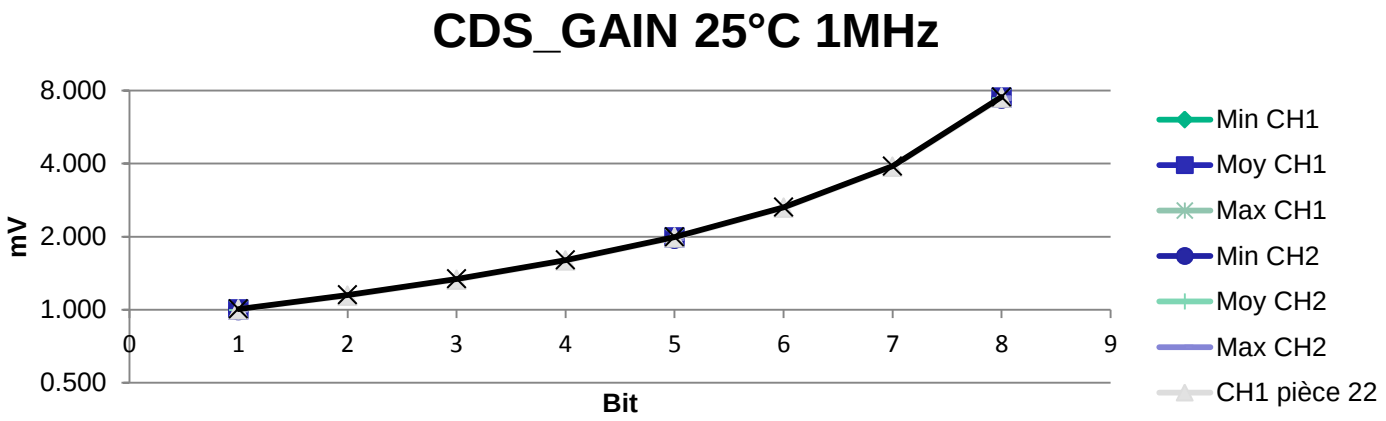
PIECE					Sampling frequency 1MHz			Sampling frequency 12MHz		
	CODE GS :				+25°c			+25°c		
TEST number	Measured parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
TEST # 10011	PIXEL_1_FS	13720	15320	lsb	15037	15096	15152	14995	15054	15105
TEST # 10012	PIXEL_2_FS	13720	15320	lsb	15075	15162	15199	15044	15129	15164
					+25°c			+25°c		
TEST number	Calculated parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
TEST # 10013	I_CHANNEL_1_FS			mA	99,4	101,8	104,0	120,8	123,4	125,0
TEST # 10014	I_CHANNEL_2_FS				97,3	100,8	105,4	121,4	124,0	129,0
TEST # 10015	I_MROD_FS				200,2	204,0	207,9	243,7	248,8	255,2
TEST # 10016	Idyn_CHANNEL_1_FS			mA/MHz	1,88	1,96	2,17			
TEST # 10017	Idyn_CHANNEL_2_FS				2,01	2,10	2,19			
TEST number	Calculated parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
Power dissipation on 3V3				mW	661	673	686	804	821	842

Close to 0

PIECE					Sampling frequency 1MHz			Sampling frequency 12MHz		
	CODE GS :				+25°c			+25°c		
TEST number	Measured parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
TEST # 10011	PIXEL_1_LS	365	2365	lsb	1407	1453	1502	1399	1445	1498
TEST # 10012	PIXEL_2_LS	365	2365	lsb	1415	1492	1520	1408	1484	1511
TEST number	Calculated parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
TEST # 10013	I_CHANNEL_1_LS			mA	97,4	100,4	102,4	118,7	122,1	124,0
TEST # 10014	I_CHANNEL_2_LS				97,5	100,9	105,5	121,5	124,1	129,0
TEST # 10015	I_MROD_LS				198,4	202,8	207,8	241,7	247,7	252,7
TEST # 10016	Idyn_CHANNEL_1_LS			mA/MHz	1,93	1,98	2,03			
TEST # 10017	Idyn_CHANNEL_2_LS				2,00	2,09	2,19			
TEST number	Calculated parameter	Low Limit	High Limit	Unit	min	moy	max	min	moy	max
Power dissipation on 3V3					655	669	686	798	817	834

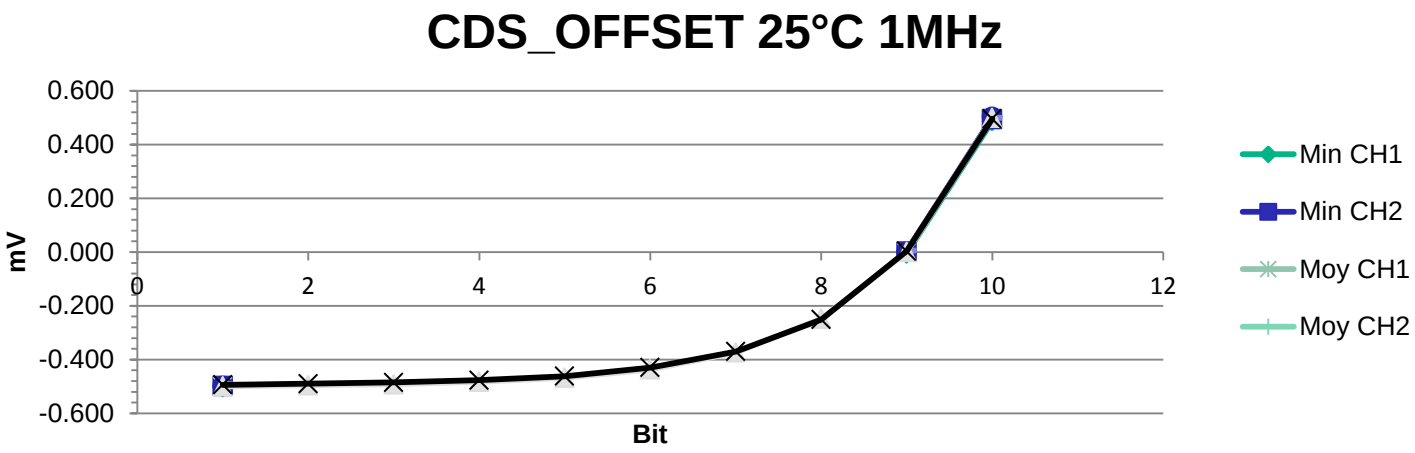
- **No significant impact of sampling frequency**

CDS programmable gain :



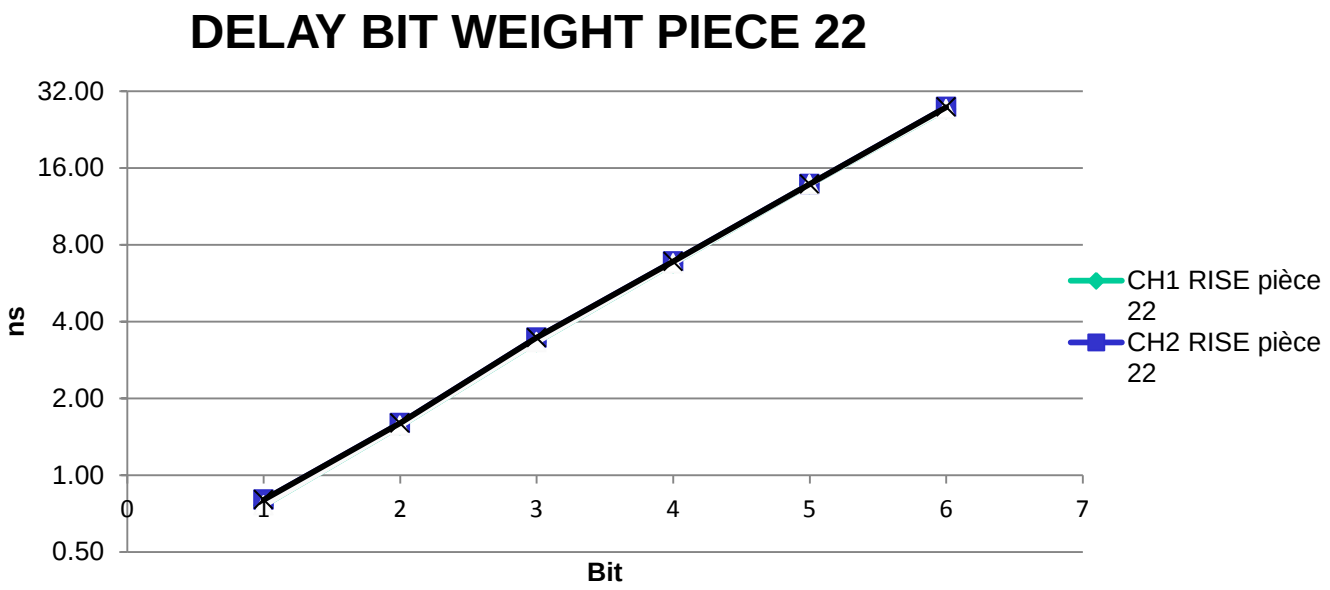
- **As expected**

CDS programmable offset :



- ±0.5V as expected
- ADC coarse and fine programmable offset are also as expected

Programmable delay :



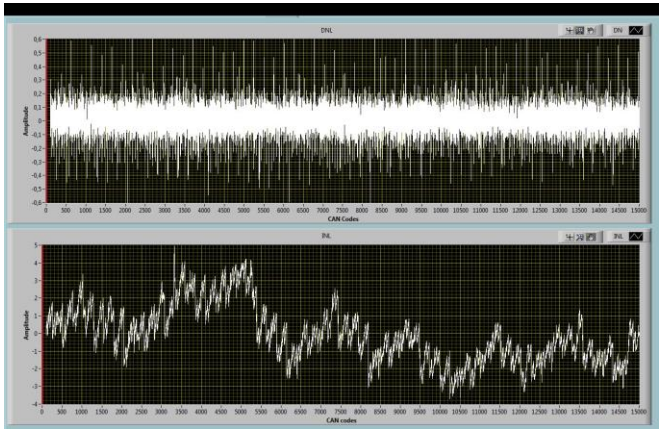
- Min delay close to 4ns
- Delay lsb < 1ns
- Max programmed delay > 25ns

Electrical test results

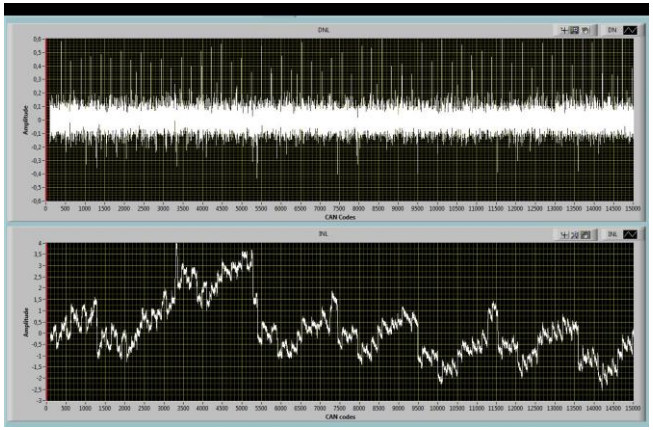
Preliminary noise and linearity measurement done on the functional test bench are showing results close to the estimated performances :

- **0.57 lsb_{12bits} referred input thermal noise at gain x2 (CDS + ADC)**
- **DNL < ±0.5 lsb_{12bits} and INL < ±2 lsb_{12bits} at 4MHz (limited by the signal generator)**

Ramp with alternate black pixel

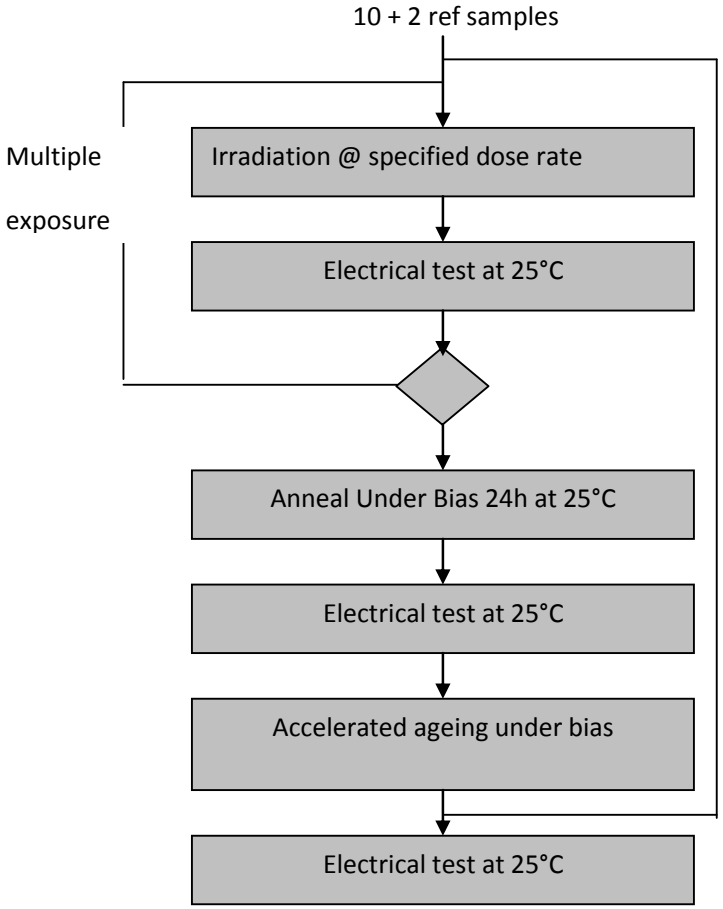


Ramp with alternate white pixel



- **Linearity is consistent in all functioning modes (ADC ONLY and CDS + ADC)**

TID campaign up to 100 krad, with steps at roughly 10, 20, 30, 40, 50 and 70 krad:



- ✓ **Electrical and irradiation benches are manufactured and validated**
- ✓ **Burnin of MROD parts is on-going**
- ✓ **TID results expected by the end of summer**
- ✓ **No SEE in the frame of the on-going contract.**

Conclusion

- ✓ The design of a high performances dual video processor demonstrator is done
- ✓ 100% of the functionalities are silicon validated
- ✓ Preliminary radiometric performances are consistent with estimation
- ✓ Radiometric tests are planned during summer
- ✓ TID results are expected by the end of summer

THANKS for y