An ASIC for Spaceborne Radiation Monitors

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Abstract

The IDE 3465 is an application specific integrated circuit (ASIC) that has been designed for the readout of silicon detectors for charged particles. The chip has 20 inputs of charge sensitive pre-amplifiers (CSA), a total of 37 digital logic trigger outputs, and one analogue multiplexer output for pulse heights. Out of the 20 channels, 16 have a high gain with saturation at 2.6 pC, and 4 have a low gain with saturation at 26 pC. In the high-gain channels, the charge sensitive pre-amplifier is connected to one slow shaper of 1-µs shaping time and two fast shapers of 250-ns shaping time, while the low-gain channels have only one slow shaper and one fast shaper of 1-µs and 250-ns shaping time. Each fast shaper output is connected to a comparator, which triggers when the pulse shape exceeds the reference level that can be programmed by 8-bit DACs. The two fast shapers and comparators of the high-gain channels are used for charges in the range from 1 fC to 100 fC and from 100 fC to 2.6 pC, respectively. The fast shapers and comparators of the low-gain channels are designed for charges in the range from 1 pC to 26 pC. Each comparator feeds a mono-stable output, which can be connected directly to an FPGA. The chip requires negative and positive voltage supplies (-2 V, +1.5 V and +3.3 V) and one reference bias current to generate its internal biases. The total power consumption is less than 65 mW, depending on the input event rate and options enabled. The chip has a 356 bit register, programmable via serial interface, which allows one to set various functions, to program digital-to-analogue converters (DACs), and to tune parameters. All amplifier inputs are protected by diodes against over-voltage and electro-static discharge (ESD). The chip is SEU/SEL radiation hardened by design and manufacture.

I. Introduction

A. *Objectives*

The IDE3465 is a full custom-application specific integrated circuit (ASIC) for the readout of space based charged particle detectors that use silicon sensors for charged particle tracking and/or counting. Such instrumentation can help providing answers to scientific questions and support space weather data acquisition. The ASIC is developed from the IDEAS TAP-family of trigger ASICs and have been designed in two versions, the IDE3464 engineering model (EM) and the radiation hardened IDE3465 flight model (FM). The IDE3465 is integrated into the Next Generation Radiation Monitor (NGRM) [1] and the ASIC development has reached an ESA technology readiness level (TRL) > 6. The NGRM shall be used for example in the EDRS-C. The development is also relevant for other applications, and will be the baseline ASIC for the upcoming RADEM radiation monitor for the JUICE mission [2].

B. *Radiation Detector Readout Principle*

Figure 1 shows the detector readout principle. A charged particle interacts in the silicon sensor and generates an electric charge that is proportional to the energy deposited in the interaction. The electrodes of the sensor are biased to generate an electric field inside the sensor, which moves the free charges and thereby generates a current. The electrodes are connected to the inputs of the charge sensitive amplifiers (CSA) in the ASIC. The CSAs integrate the induced currents over time and deliver a pulse height that is proportional to the energy dissipated in the particle interaction. The ASIC delivers individual trigger signals for every channel when a pulse height exceeds the programmed threshold. In addition, the system can read out the pulse height from all channels.

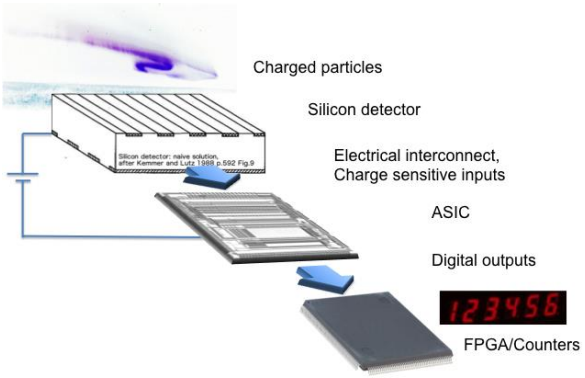

Figure 1: Radiation detector readout principle.

A. *Specific Goals*

The ASIC has charge sensitive amplifiers with two different fixed gains to accommodate different charged particles (*e*, *p*, ions) in the silicon sensor. There are up to two comparators per channel and their reference voltages can be programmed independently using 8-bit DACs. Each comparator result can be a direct input a field-programmable gate array (FPGA), which provides coincidence logic and digital counting. Important goals of this development were the low power dissipation and the relatively high radiation tolerance against single event effects, *i.e.*, 50 MeVcm^2/mg linear energy transfer threshold (LET_{th}).

A. *Design Heritage for Space Instrumentation*

Our group has designed similar ASICs in previous years. For this type of ASIC, our space heritage includes the analogue

front-end for the silicon charged particle trackers in AGILE [3], Stereo/Plastic [4], PAMELA [5], AMS1 and AMS2 [6], MEGA [7], BepiColombo [8], FOXSI [9], and ASTRO-H [10]. Other space heritage is described in [11].

II. Experimental Technique

A. *Architectural Overview*

Figure 2 shows the block diagram of the ASIC. The chip has 20 inputs of charge sensitive pre-amplifiers (CSA), a total of 37 digital logic trigger outputs, and one analogue multiplexer output for pulse heights. Out of the 20 channels, 16 have a high gain with saturation at 2.6 pC, and 4 have a low gain with saturation at 26 pC. The chip contains a bias network that generates all bias needed for the operation. The chip has a programmable configuration register that allows one to control internal bias values and other settings.

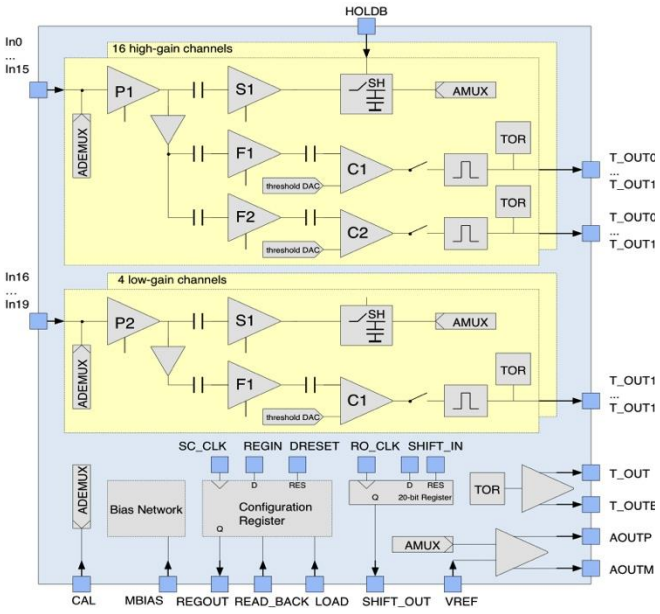

Figure 2: Block diagram of the chip.

B. *Channel Architecture*

Figure 3 shows a block diagram of a high-gain channel. The pre-amplifier (P1) integrates over time the electrical current and outputs a voltage step. The pre-amplifiers are designed for a capacitive load of 30 pF. The shaping amplifier (S1) has 1-µs shaping time and provides pulse height for sample-and-hold (SH) to the analogue multiplexer (AMUX). The other two shaping amplifiers (F1, F2) have 250-ns shaping time and provide pulse heights to the comparators (C1, C2), which trigger a mono-stable. The outputs from the mono-stables can be used by the system to count triggers from each channel individually or in coincidence.

A. *Signal Timing*

Figure 4 shows a timing diagram of the most important signals. The current in the pre-amplifier of channel N (2) generates a trigger at **T_OUT*N*** and a trigger at **T_OUT** (3). These signals can be used for external coincidence and counting. The system can sample the pulse heights from all channels by activating **HOLDB** at the peaking time T_p (4). The system acquires the pulse heights at the differential current at **AOUT** by applying **SHIFT_IN_B** and **RO_CLKB**.

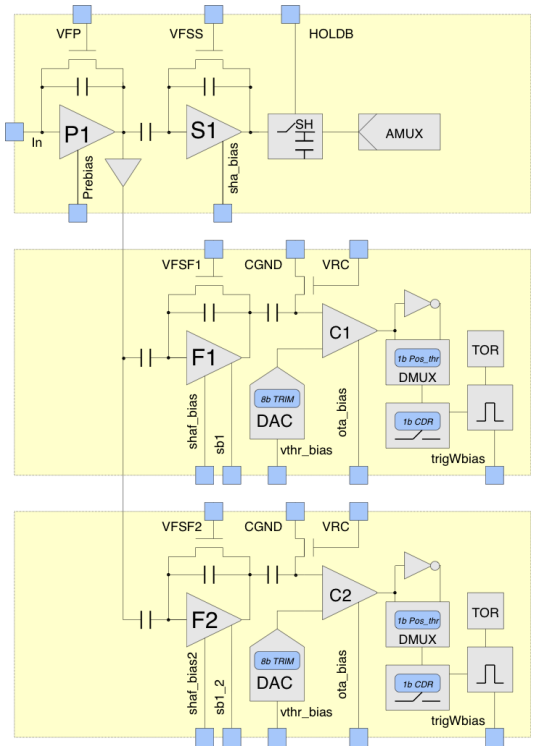

Figure 3: Block diagram of a high-gain channel.

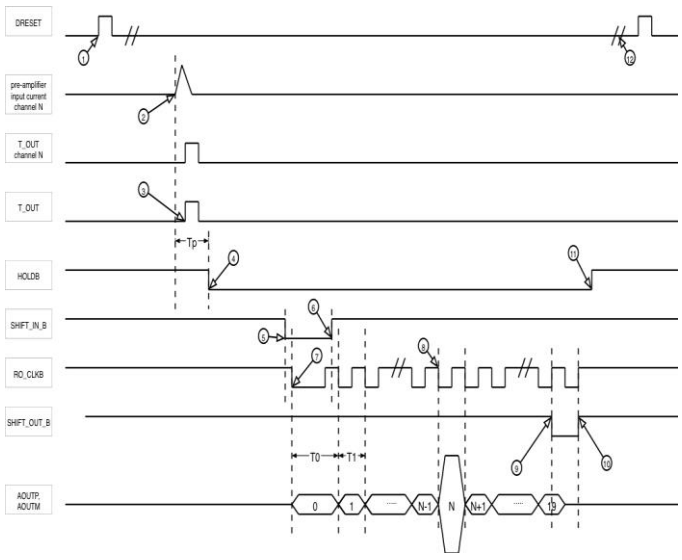

Figure 4: Signal timing.

B. *Specifications*

Table 1 summarizes the ASIC specifications. The values were experimentally validated on a few samples of the flight model ASIC.

A. *Radiation Tolerance*

The flight model ASIC was designed to meet the radiation requirements set for the NGRM [1]. The digital circuits have been designed using guard rings to prevent single event latch-up (SEL). Tests with heavy ion beams show a SEL threshold

higher than 116 MeVcm^2/mg. The programmable configuration register has been designed to correct for single-event upset (SEU), *i.e.*, each register cell has triple redundancy with a self-correcting circuit and a SEU output signal. The 0.35 µm CMOS process meets the 100-krad total-ionizing dose requirements (TID).

Table 1: Specifications.

20 charge sensitive inputs	< 2.6 pC in 16 high-gain channels < 26 pC in 4 low-gain channels
37 digital logic trigger outputs	32 outputs from the 2 comparators in the high-gain channels 4 outputs from the comparator in the low-gain channels 1 OR from all comparators
1 analogue output	Pulse height spectroscopy from all channels
Noise	0.45 fC ENC in high-gain channels 5 fC ENC in low-gain channels
Trigger threshold, minimum	1.5 fC and 71 fC in high-gain channels 150 fC in low-gain channels
Power	62.5 mW maximum, typical consumption 50 mW
Rate, maximum	> 1 Mcps/channel capability at the trigger outputs > 2.5 kcps/channel with analogue readout of all channels
Radiation tolerance	The chip is SEL immune (SEL LET_{th}>100 MeV/mg/cm2) The chip is radiation tolerant by design and manufacture, with respect to single event upsets

B. *Layout*

Figure 5 shows a photograph of the chip. The pre-amplifier inputs are located on the top and trigger outputs are on the bottom. The chip has many pads on the left and right side for power supplies and pads to monitor or apply internal bias settings. Except for the main bias, the bias pads do not need to be used during normal operation, because these are generated internally. The chip is designed for wire bonding.

C. *Manufacture*

The chip was designed and manufactured in AMS 0.35-µm CMOS technology [13] using our radiation tolerant full-custom ASIC design library. Table 2 summarizes the manufacturing information.

Table 2: Manufacture.

Supplier	IDEAS
Wafer fab	AMS
Technology	0.35 µm CMOS
Epitaxial layer	Yes
Metal Layers	4
Capacitor option	Double poly
Chip dimensions	6045 µm × 7140 µm

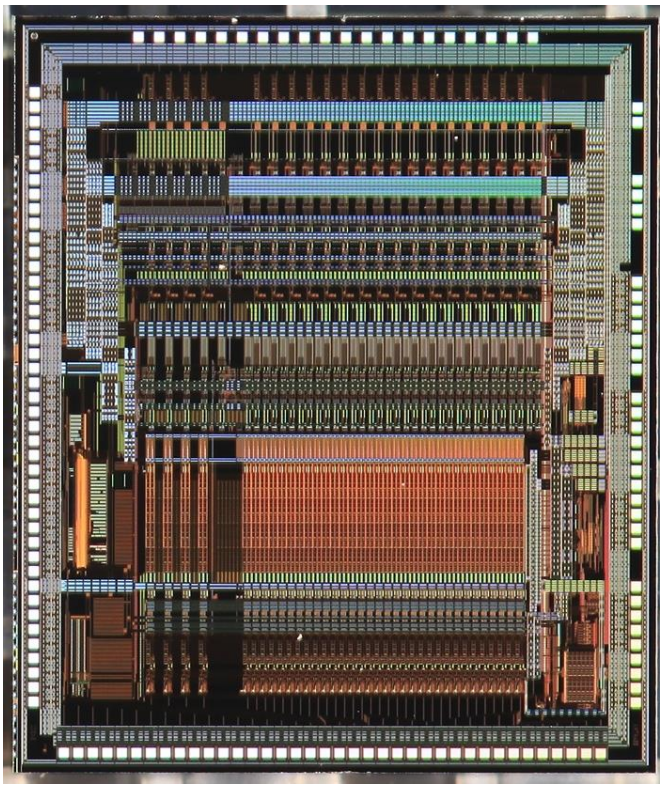

Figure 5: Photograph of the flight model ASIC.

III. RESULTS

A. *Input Charge Range*

Figure 6 shows the pulse height measured versus the input charge in a high-gain channel (top) and a low-gain channel (bottom) at different temperatures. The pulse height was measured at **AOUTM** and **AOUTP** using a test system with differential current-to-voltage converter and analogue-to-digital converter. At room temperature, the high-gain channel has a linear gain of about 330 µA/pC up to 2.6 pC; the low-gain channel has a linear gain of about 32 µA/pC up to 26 pC.

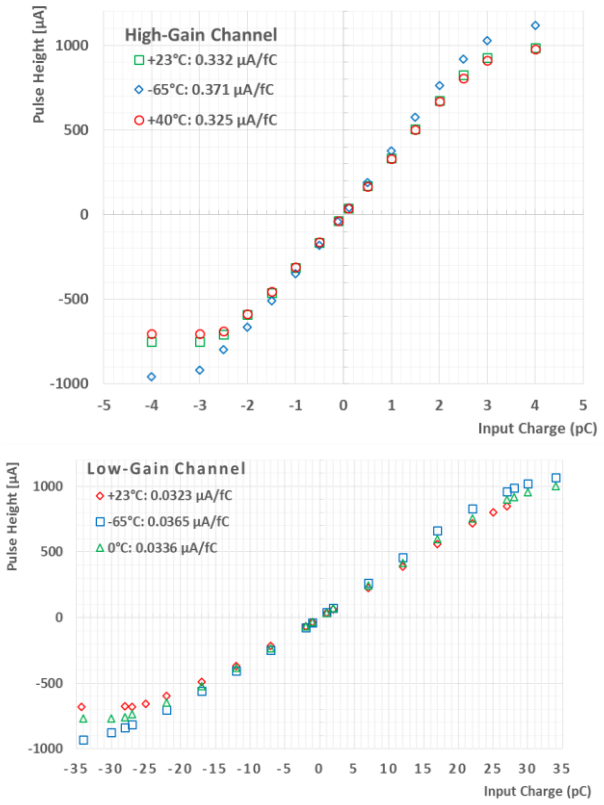

Figure 6: Measurement of the pulse height versus injected charge in a high-gain channel (top) and a low-gain channel (bottom) at different temperatures.

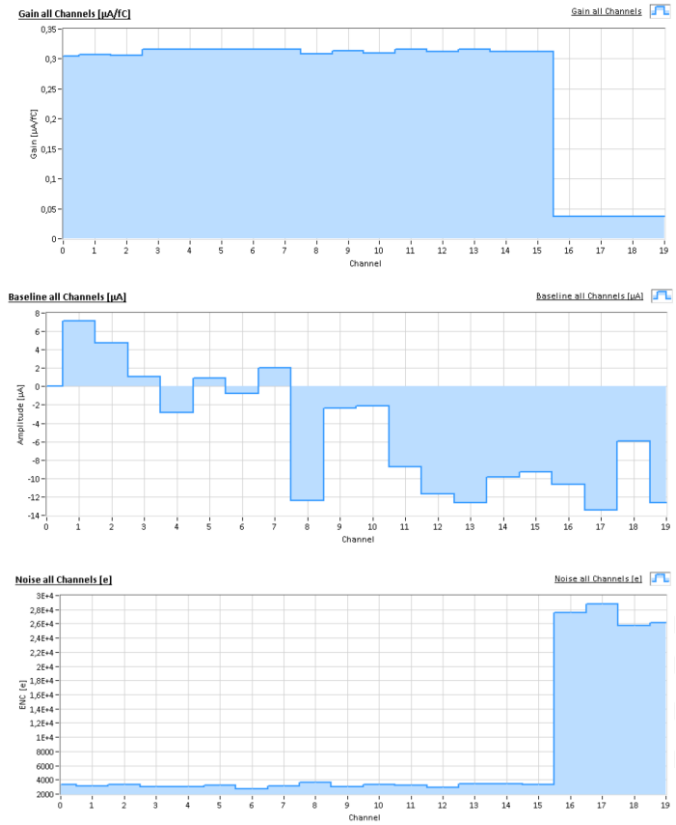

Figure 7: Gain, baseline, and equivalent noise charge (ENC) in all channels of the chip under test.

A. *Noise*

Figure 7 shows the baseline, the equivalent noise charge (ENC) and the gain from all 20 channels in the chip under test. We measure ENC of 0.45 fC in high-gain channels and 5 fC in low-gain channels. The noise does scale as expected with the saturation charge.

B. *Trigger Threshold Characteristics*

To verify rate capability, we injected test pulses at a constant rate of 1 MHz into one channel, and at that rate, we observe zero loss counts in the channel. Figure 8 show the rate capability of the high-gain channel high threshold and low threshold discriminator as a response to a 1 MHz, 200 fC input ramp signal. The ASIC is capable of trigger rates beyond 1 MHz.

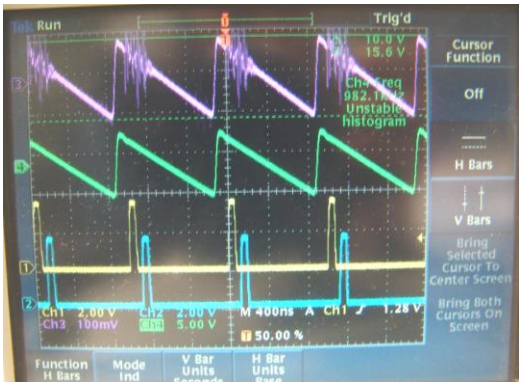

Figure 8 Measurement of the trigger output rate capability.

C. *Performance with Temperature*

Figure 9 and Figure 10 show the gain and noise measured versus temperature in the range from -65 °C to +40 °C. The gain decreases by about 0.1 %/°C with increasing temperature relative to the gain at the lowest temperature. The noise is about constant within the measurement error.

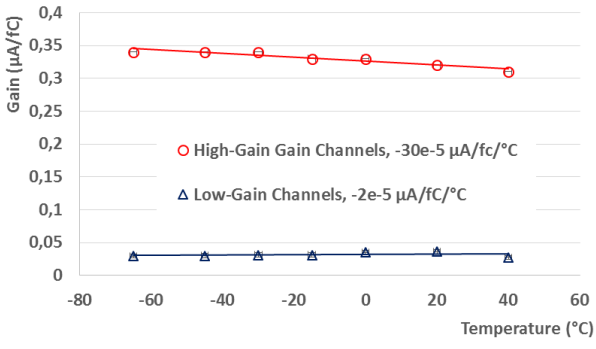

Figure 9: Mean value of the gain from high-gain channels and low-gain channels measured versus temperature.

D. *Radiation Testing*

The IDE3465 has been tested for radiation tolerance with respect to Single Event Effects (SEE) at Université Catholique de Louvain using the Heavy Ion Irradiation Facility (HIF).

The ASIC was tested using the M/Q ion cocktail with 40 µm penetration depth in Si. The ions with highest energy

available at UCL were 459 MeV $^{132}Xe^{26+}$ ions resulting in a linear energy transfer in silicon (LET (Si)) of 67.7 MeV/mg/cm^2. To induce SEL, the ASIC was mounted on a test card with heaters to increase the ASIC temperature to 80°C. The test card was mounted on a 3-axis movable test-frame. The ASIC was tilted in respect to the ion beam to produce a slanted ionization track. The resulting LET_{eff} was thus increased to 116 MeV/mg/cm^2. The results of the irradiation tests show that the IDE3465 does not latch-up at 116 Mev/mg/cm^2.

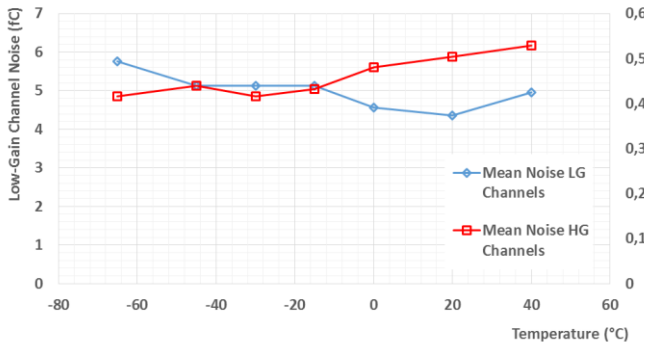

Figure 10: Mean equivalent noise charge (fC) from high-gain and low-gain channels measured versus temperature.

IV. SUMMARY

We have developed an ASIC that can be used for charged particle counting with silicon detectors in space. The ASIC was designed to meet the requirements of the ESA Next Generation Radiation Monitor (NGRM) [1]. The main characteristics are the two types of channels with saturation charge of 2.6 pC and 26 pC, respectively. Each channel provides trigger outputs that can be directly connected to an FPGA for additional logic and counting. Single event effect tests show that the ASIC has a latch-up threshold of more than 116 MeVcm^2/mg. The work on a successor for the ASIC is ongoing as a part of the ESA RADEM project.

ACKNOWLEDGEMENTS

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