Contribution ID: **41**   Type: **Poster**

An ASIC for Spaceborne Radiation Monitors

Monday 30 June 2014 14:40 (40 minutes)

The IDE 3465 is an application specific integrated circuit (ASIC) that has been designed for the readout of silicon detectors for charged particles. The chip has 20 inputs of charge sensitive pre-amplifiers (CSA), a total of 37 digital logic trigger outputs, and one analogue multiplexer output for pulse heights. Out of the 20 channels, 16 have a high gain with saturation at 2.6 pC, and 4 have a low gain with saturation at 26 pC. In the high-gain channels, the charge sensitive pre-amplifier is connected to one slow shaper of 1-μs shaping time and two fast shapers of 250-ns shaping time, while the low-gain channels have only one slow shaper and one fast shaper of 1-μs and 250-ns shaping time. Each fast shaper output is connected to a comparator, which triggers when the pulse shape exceeds the reference level that can be programmed by 8-bit DACs. The two fast shapers and comparators of the high-gain channels are used for charges in the range from 1 fC to 100 fC and from 100 fC to 2.6 pC, respectively. The fast shapers and comparators of the low-gain channels are designed for charges in the range from 1 pC to 26 pC. Each comparator feeds a mono-stable output, which can be connected directly to an FPGA. The chip requires negative and positive voltage supplies (-2 V, +1.5 V and +3.3 V) and one reference bias current to generate its internal biases. The total power consumption is less than 65 mW, depending on the input event rate and options enabled. The chip has a 356 bit register, programmable via serial interface, which allows one to set various functions, to program digital-to-analogue converters (DACs), and to tune parameters. All amplifier inputs are protected by diodes against over-voltage and electro-static discharge (ESD). The chip is SEU/SEL radiation hardened by design and manufacture. Tests with heavy ion beams show a SEL threshold higher than 116 MeVcm2/mg. The programmable configuration register has been designed to correct for single-event upset (SEU), i.e., each register cell has triple redundancy with a self-correcting circuit and a SEU output signal. The 0.35 μm CMOS process meets the 100-krad total-ionizing dose requirements (TID).

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Session Classification: Poster Session