

# Creating and Updating Standards for New Analog and Mixed – Signal ICs for Space Missions

# AMICSA 2014

(Analogue and Mixed –Signal Integrated Circuits for Space Applications) CERN, Geneva, Switzerland June 30 - July 1, 2014

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NASA's Curiosity Mars rover has driven within robotic-arm's reach of the sandstone slab at the center of this April 23 view from the rover's Mast Camera. The rover team plans to have Curiosity examine a target patch on the rock, called "Windjana," to aid a decision about whether to drill there. *Image Credit: NASA/JPL-Caltech/MSSS* 

# **AMICSA** and **NEPAG**

- I would like to thank Boris Glass and the AMICSA 2014 Program Committee for this opportunity.
- AMICSA is a unique workshop.
- This is our third consecutive participation and we are happy to be here.
- This work was sponsored by the NASA Electronic Parts Assurance Group, NEPAG



### Introduction

#### New Technology Infusion into MIL/Space Standards

- On December 20, 2013, the Defense Logistics Agency (DLA) released revision K of microcircuit specification, MIL-PRF-38535.
- This document revision is significant because it updates existing requirements and creates requirements for new analog, mixed-signal and other integrated circuits (ICs) including those that are built as flip-chips and with columns attached.
- It also introduces and enables Class Y, a new category of microcircuits for space.
- Development of Class Y was a NASA-led initiative for the space community to infuse new technology into military/space standards.

### **Microcircuit Specification MIL-PRF-38535, Revision K**

- Revision K
  - Released 20 Dec2013
- Includes Class Y requirements
  - New Technology Infusion
  - Developed by G12 Task Group
  - Under NASA leadership



AMSC N/A

### MIL-PRF-38535, Revision K (Contd.)

- DLA email announcing the release of MIL-PRF-38535, Revision K
- Introduces and enables Class Y, infuses new technology into DoD standards

From: Akbar, Muhammad A DLA CIV LAND AND MARITIME [mailto:Muhammad.Akbar@dla.mil]
Sent: Friday, December 20, 2013 8:57 AM
Cc: Heber, Robert M (DSCC); Gemperline, Joseph L DLA CIV LAND AND MARITIME
Subject: Approved and dated copy of MIL-PRF-38535 revision K

Hi all,

Please see attached letter for MIL-PRF-38535 revision K which is approved and dated December 20, 2013.

The major changes/updates to this revision K are:

(a) To add new class Y (non-hermetic space application products) requirements including screening, QCI/TCI and RHA tables;

(b) To update/modified and combined screening, QCI/TCI and RHA requirements tables from MIL-STD-883 method TM 5004/5005 and MIL-PRF-38535 tables;

(c) To add multi-product wafer (MPW) requirements per JEDEC task group recommendations; and

(d) To add package integrity demonstration test plan (PIDTP) requirements for BGA/CGA packages.

Please use below DLA Land and Maritime website for downloading the approved MIL-PRF-38535 revision K and change summary.

http://www.landandmaritime.dla.mil/programs/milspec/ListDocs.aspx?BasicD oc=MIL-PRF-38535

Happy holiday and prosperous happy new year

With regards

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### **Space Parts World**



NEPAG is actively involved with the procurement process - parts users and standards organizations join hands to ensure timely delivery of reliable parts from suppliers.

### MIL-PRF-38535K Development Poster Child Used

#### Device Selected

- Picked one of the most complex parts
  - Xilinx Virtex 4 and 5 FPGAs, were used as the poster child.
- These devices are called the system-on-a-chip (SOC) as they
  - Are high performance
  - Contain all varieties of functions
    - o Analog, digital, mixed-signal
  - Represent state-of-art packaging
    - Flip chip construction
    - o Column grid arrays.
  - Represent advanced technology
    - o V-4 is 90nm
    - o V-5 65nm
- They also use signal integrity capacitors of the base metal electrode (BME) construction.

### Infusion of New Technology into MIL Standards Qualifying New Packaging Technology

### Issue

 How to address the manufacturability, test, quality, and reliability issues unique to specific non-traditional assembly/package technologies intended for space applications?

### Proposal

- Each manufacturer to develop a Package Integrity Demonstration Test Plan (PIDTP).
- Addresses issues unique to non-hermetic construction and materials, such as potential materials degradation, interconnect reliability, thermal management, resistance to processing stresses, thermo-mechanical stresses, & shelf life.
- The PIDTP shall be approved by the qualifying activity after consultation with the space community. Ref: 38535K, Para B.3.11

### Infusion of New Technology into MIL Standards Applicability of the PIDTP

- The Package Integrity Demonstration Test Plan (PIDTP) requirement would apply to:
  - Non-hermetic packages (e.g., Class Y). Ref: 38535K, H.3.4.4.1.1.
  - Flip-chip assembly. Ref: 38535K, H.3.4.4.1.2.
  - Solder terminations. Ref: 38535K, H.3.4.4.1.3.
- Microcircuits employing more than one of above technologies shall include elements for each in the PIDTP.
   Ref: 38535K, H.3.4.4.1.

### Screening Requirements in 38535K Class V vs. Class Y

### Screening

- Same for both V and Y except the differences related to hermeticity vs. non-hermeticity.
- Column Attached Parts (as offered by Manufacturers)
  - 100% DC electricals post column attachment (same for V and Y)
  - Visual inspection (same for V and Y)
  - No additional screening requirement for V or Y



The Hubble Space Telescope (HST) is a 2.4m (7.9-ft) aperture space telescope. It was carried into low Earth orbit by a Space Shuttle in 1990, and it remains in operation.

## QCI Requirements in Draft 38535K Class V vs. Class Y

- Quality Conformance Inspection (QCI) (Land Grid Array)
  - Group A :
    - Same for both V and Y
  - Group B:
    - Same, except hermeticity vs. non-hermeticity differences
  - Group C:
    - Same
  - Group D:
    - Same except hermeticity vs. non-hermeticity differences
    - Added PIDTP.
      - PIDTP (Flip-chip) and PIDTP (Solder terminations): Same for V and Y
      - PIDTP (Non-hermetic packages): Class Y only
  - Group E:

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Same for both V and Y

### Column Attached Parts (as offered by Manufacturers)

- Columns shear test
- Group A, Subgroup 1 only:
  - Same for V and Y

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### 38535K

#### Pre/Post Column Electricals

- The manufacturer shall perform post column attachment electrical characterization over temperature and compare data with pre-column attachment process to assess any changes due to the column attach process. (Ref: 38535K, H.3.4.4.1.3)
- Note: Although the whole space community worked on these changes, the DLA is the final authority on approval/disapproval decisions. All questions related to the acceptability of new designs, alternate test methods should be addressed to them.

### Pre and Post Column Attach Data (Ref: BAE Presentation at Oct. 2012 Class Y meeting)

#### BAE SYSTEMS

### Electrical Test With or Without Columns

#### BAE Systems performs burn-in and 3-temp testing without columns

Post-column attach: BAE Systems performs room temp testing only

#### CGA Module Test Experiment (requested by Aerospace/NASA)

- 3 RAD750 devices were 3-temp tested without columns (Land Grid Array)
- Columns were attached
- Devices were then re-tested with columns (Column Grid Array)
- All 3 parts passed full Group A test both pre- and post-column
- Test results were compared pre- and post-column

Comparison of Input-Output	Input leakage (high voltage) (IIH)	+25C -55C	< 0.5% < 6%	< 1% < 1.5%	< 0.5% < 1.5%
Test Parameters shows < 8% deltas		+125C	< 7%	< 7%	< 8%
between pre- and post- column electrical test:	Input leakage (low voltage) (IIL)	+25C -55C +125C	< 1% < 3% < 1.5%	< 1.5% < 3.5% < 2%	< 1% < 3.5% < 2%
	Voltage Output High (VOH)	+25C -55C +125C	< 0.5% < 1% < 0.5%	< 0.5% < 0.5% < 0.5%	< 0.5% < 0.5% < 0.5%
	Voltage Output Low (VOL)	+25C -55C +125C	< 3.5% < 6% * < 4%	< 7% < 7% < 4%	< 3.5% < 5% < 3.5%
	Dynamic I/O Idd	+25C -55C +125C	< 3% < 3% < 3%	< 3% < 3% < 3.2%	< 3% < 2.5% < 3%
			* except 1 pir	1 at 12%	

Approved for public release; No Export Controlled Data (release # ES-MVA-042213-0173)

### **Issues Going Forward**

- Looking Ahead for Classes V and Y:
  - Space community to work with DLA to
    - Certify column attach service providers
      - $\circ~$  Six Sigma, BAE, STS, others
    - Ensure ESD surveys are current
      - $\circ$  NASA to provide support
    - Monitor on-going JEDEC task group activities
- Looking Ahead for Class Y:
  - Space community to work with DLA to
    - Qualify Xilinx V-4 / V-5 CN package per newly released 38535K.
      - Xilinx announced at the SPWG (Space Parts Working Group , April 2014) that CN packages will be offered with Six Sigma columns
    - Schedule QMLY audits of front runner suppliers (and their supply chains)
      - o Xilinx, Aeroflex, e2V

- Signal integrity capacitors used in microcircuits
  - MIL-PRF-38535, Para 3.15.1 specifies screening requirements
  - Base metal electrode (BME) capacitors used with low-voltage high speed microcircuits do not meet Para 3.15.1
    - o BMEs were meant to be used in commercial applications
    - However, the upscreened versions of the BMEs have also found their way into microcircuits and hybrids of interest to the space community
    - The suitability of BMEs for use in space applications is being evaluated
      - > The goal is to have an acceptable screening flow

#### Burn-in of microcircuits

- With the availability of analog-to-digital (A/D) and digital-to-analog (D/A) converters operating at high frequencies (several hundred MHz to GHz), the screening and qualification of such microcircuits is being reviewed by the industry and government users with the goal of clarifying and adding to the existing requirements.
- The next few sheets discuss issues related to burn-ins.

- Bl is the key screening step considered essential to weed out product infant mortality.
- Our recent audit and specification review work has shown that the microcircuits BI screening requirements as stated in MIL-STD-883, Test Method 5004, are **out of date and have multiple interpretations**.
- Why are they out of date?
  - Were developed more than 25 years ago
  - Then: were at 5-micron technology node
  - Now: 45-nm space products in development, on their way to QMLV certification. Made possible by
    - o Dual-use technology
    - Advances in packaging technology
    - Availability of system-on-a-chip (SOC) products, which could be easily called assemblies
  - With column grid arrays (CGAs), screening is no longer practical (e.g., fixturing and potential damage to the parts)
  - Changing business landscape

- No clear interpretation any longer
  - Varied implementation
- Periodic, frequent updates are needed!
- **Recent Activities** 
  - At the request of NASA, the Aerospace Corporation and others, a Task Group was formed to provide guidance.
  - More rigorous assessment is being done during audits and specification reviews pending guidance from the task group



Launched June 10, 2011, the Aquarius/SAC-D mission is a partnership between NASA and Argentina's space agency (CONAE) using advanced technologies to make global space-based measurements of ocean salinity.

- Review the role and fundamentals of BI.
- Is the high-temperature reverse bias test (HTRB) still meaningful?
- Static BI
  - How many needed
  - Biasing of each circuit
  - Electrical measurements
  - Changing business landscape
  - Meaningful readings
  - Dynamic Bl
    - Voltage
    - Frequency
    - Output loading
    - Ensuring proper BI of high speed devices

#### Parametric Deltas

- Which parameters.
- Limits
- Ensure the readings are meaningful



This image of an outcrop at the "sheepbed" locality, taken by NASA's Curiosity Mars rover, shows welldefined veins filled with whitish minerals, interpreted as calcium sulfate. These veins form when water circulate through fractures, depositing minerals along the sides of the fracture. These veins are Curiosity's first look at minerals that formed within water that percolated within a subsurface environment. The vein-fills are similar in appearance to the Sheepbed rock unit in the Yellowknife Bay area of Northwest Canada.

#### Junction temperature

- How to achieve maximum allowable junction temperature
- Limited-temperature (restricted-temperature) range parts
  - What is the allowed BI temperature?
  - BI duration time/temp table in TM 1015, applies to hybrids but is not applicable to microcircuits
  - What temp range to do final (post BI) electricals?
  - Are hot spots a concern?
- New technology CGAs
  - Suppliers don't recommend post-CGA BI
  - How to ensure infant mortality removal after installation of columns
- Supply chain management
  - Additional BI to catch parts potentially damaged by extra handling?
- Hybrids parts
  - BI temperature, time, voltage
  - Element evaluation burn-in
- Hybrid crystal oscillators
  - BI temperature, time, voltage

### **Radiation Test References**

#### NSREC Data Workshop Papers

- Farokh Irom and Shri G. Agarwal, "Compendium of Single-Event Latchup and Total Ionizing Dose Test Results of Commercial Analog to Digital Converters," NSREC Data Workshop 2012.
- Farokh Irom, Shri G. Agarwal, Mehran Amrbar, "Compendium of Single-Event Latchup and Total Ionizing Dose Test Results of Commercial and Radiation tolerant Operational Amplifiers," NSREC Data Workshop 2014. (Paper number W-41, to be presented in July 2014)

### Conclusion

#### • MIL standards need periodic reviews to

- Clarify requirements
- Update requirements
- Add new requirements
- Ensure Implementation
  - audits
  - SMD reviews
- Never boring
  - Always new issues to work
- Flexibility needed
  - Especially when it comes to adapting new technology

#### Thank you!



Gravity Recovery and Interior Laboratory (GRAIL) mission, used twin spacecraft flying in formation to investigate the moon's gravity field, a possible inner core and how Earth and other rocky planets formed. The probes were launched September 2011, arrived with the New Year, and operated until December 17, 2012.

# **Backup Slides**

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### Monolithic vs. Hybrid Microcircuits and Related Issues



**A New Issue**: No MIL capacitors to satisfy the needs of new high-speed, low voltage designs. They are using Commercial **BME** (Base Metal Electrode) capacitors with unproven space heritage. Affects Classes V/Y.

BME Used?	Yes, but not tested to 3.15 (Xilinx V-4/V-5 FPGAs, are Class Y candidates)	Yes, but meet existing element evaluation requirement which are not as stringent as for 38535.
Mitigation	<b>Evaluate</b> BMEs (NASA, Aerospace, Suppliers, ESA, JAXA)	<b>Stop use</b> until evaluation done. (Ref: G12 letter to DLA)

### Infusion of New Technology into the QML System **G12** Class Y Effort at a Glance



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Thanks to everyone who contributed to the successful landing and operation of the Curiosity Rover!

NASA's Mars Science Laboratory (Curiosity rover) Launched: Nov. 26, 2011 Landed : Aug. 5, 2012

# http://nepp.nasa.gov



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