SEE Characterization of a Magnetometer Front-End ASIC Using a RHBD Digital Library in AMS 0.35 μm CMOS

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Contents

Introduction

- Application of IMSE and US Mixed-Signal Design expertise to space ASICs
  - Collaboration with Instituto Nacional de Técnica Aeroespacial (INTA) started in 2008
  - Selection of technology from an European foundry (AMS 0.35μm)
    - Mature, reliable, long-life (automotive market)
    - Reduced prototyping and low-volume production cost
    - Suitable for moderate performance MS designs
  - Start from the ground
    - Technology evaluation and characterization (TID, temperature)

Front-End Magnetometer Interface Chip

- General-purpose analog interface for high-accuracy, low-frequency data acquisition.
  - To be used initially in a six-axis magnetometer application based on Anisotropic Magnetoresistors (AMRs)
    - Six 16-bit dual-slope ADCs
    - Four 15-bit single-slope ADCs
    - Three 9-bit current-steering DACs
    - SPI interface for configuration and data acquisition
  - Using IMSE's proprietary rad-tolerant digital library.

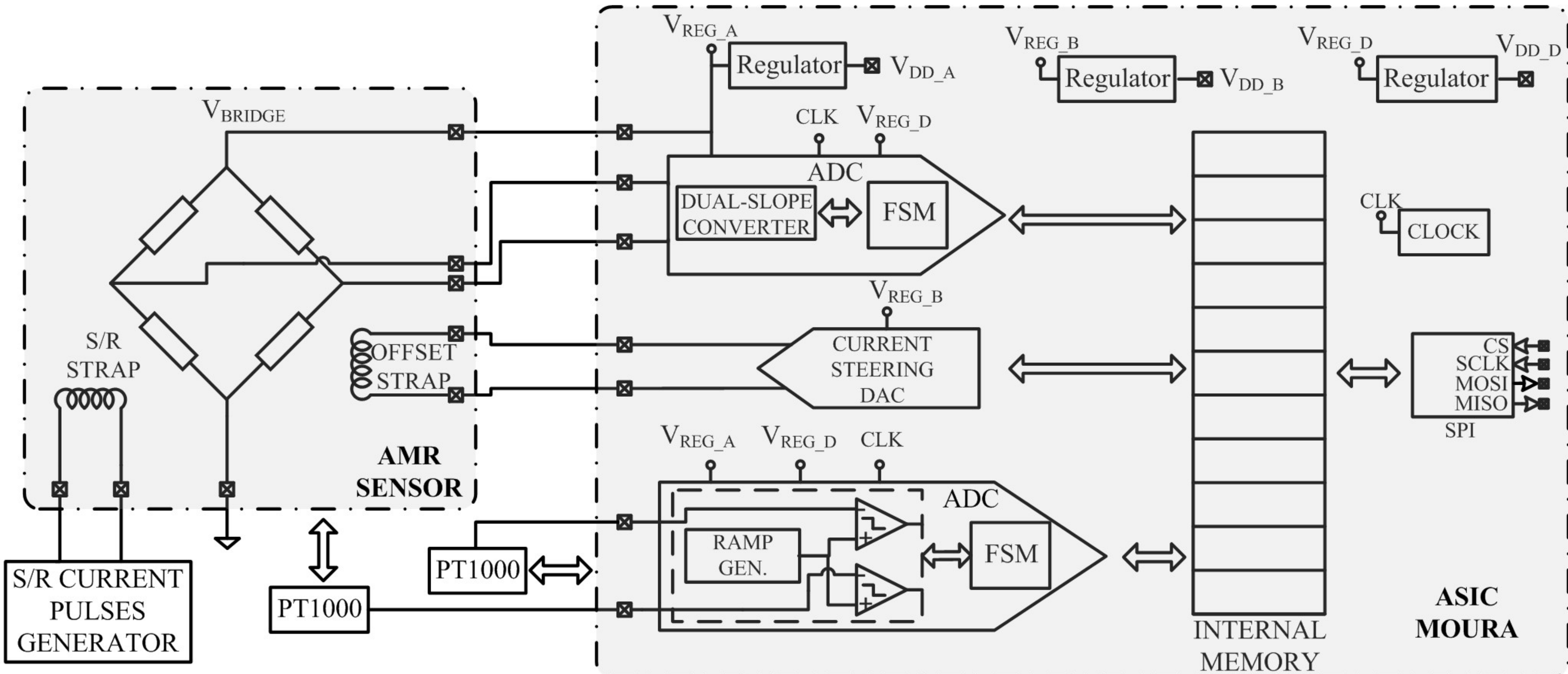
Front-End Magnetometer Interface Chip (2)

- Radiation Hardening by Design
  - Rad-Tolerant digital library: ringed-source (R-S) layout, increased drive strength, guard-rings.
  - Configuration registers duplicated with continuous monitorization of discrepancies.
  - Finite-State Machines using One-Hot encoding.
  - Analog blocks use R-S layout

Front-End Magnetometer Interface Chip (3)

- Dual-Slope Converters (x6)
  - 100 MHz clock: 16-bit @ 2.6 ksps; 12-bit @ 20 ksps
- Single-Slope Converters (x4)
  - 100 MHz clock: 15-bit @ 3 ksps; 10-bit @ 77ksps
- D/A Converters (x3)
  - 9-bit (speed determined by SPI)

Front-End Magnetometer Interface Chip (4)



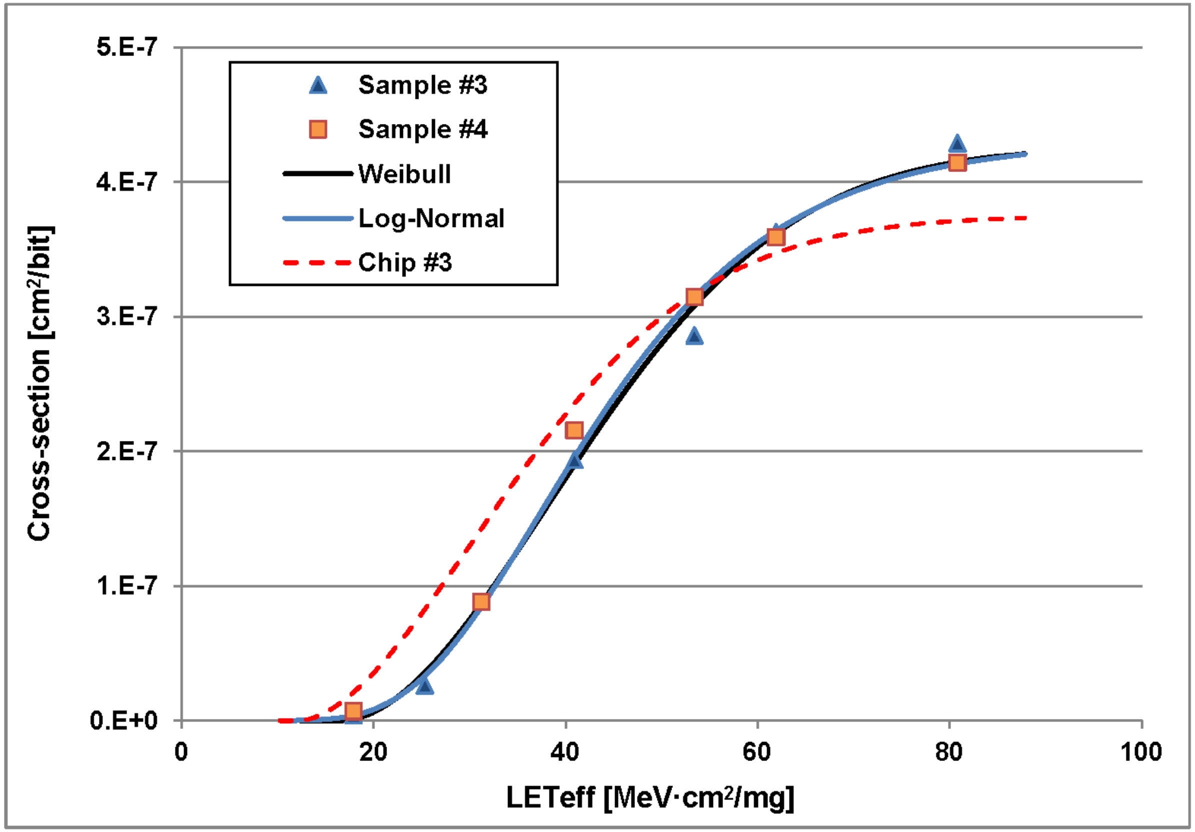
Single-Event Effects Tests

- Two samples tested in six hours of beam-time at UCL-HIF
- High LET cocktail, from Ne @ 55º (LET= 11.9) to Xe @ 40º (LET = 80.8)
- Three tests performed in parallel:
  - SEU, using 208-bit configuration register bank.
  - SEL, external monitoring of supply currents.
  - SET/SEU, recording ADC outputs.

Single-Event Upsets

- Uses the 208 bits in the configuration register.
  - Read ~ 35 times per second and rewritten if an error is detected. The full register is saved in a file when at least one bit is in error.
  - Each test to a fluence of 10^7 (lower LETs) or $5 \cdot 10^{-6}$ (higher LETs). At least 200 errors recorded in tests with lowest fluence.
  - Multiple bit errors assigned to SET in the clock and reset trees. Only single-bit errors considered as flip-flop SEU.
  - Cross-section values for oblique incidence corrected for geometric effects.

Single-Event Upsets – Cross Section



IMPROVED LIBRARY

FoM: $3.78 \cdot 10^{-8}$ MeV^2·cm^2·mg^{-2}

Upset Rate: $3.6 \cdot 10^{-8}$ bit^{-1}·day^{-1}

LET$_{th}$: 16.5 MeV·cm^2·mg^{-1}

σ_s: $4.3 \cdot 10^{-7}$ cm^2

PREVIOUS LIBRARY (CHIP #3)

FoM: $5.36 \cdot 10^{-8}$ MeV^2·cm^2·mg^{-2}

Upset Rate: $5.1 \cdot 10^{-8}$ bit^{-1}·day^{-1}

LET$_{th}$: 12.1 MeV·cm^2·mg^{-1}

σ_s: $3.75 \cdot 10^{-7}$ cm^2

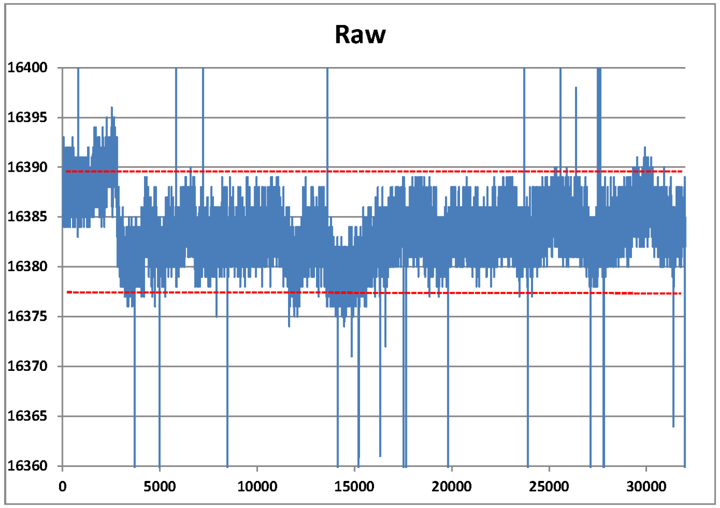
SEEs in A/D converters

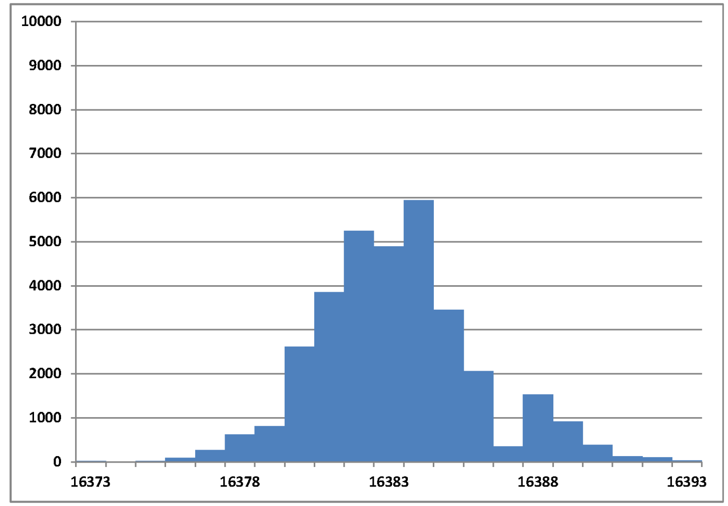
- In each irradiation step, with static inputs, recorded long series of output values (~ 35 ksamples) for each of the six ADCs at 35 readings/second
- Postprocessed to eliminate the effects of long and short-term drifts in baseline
- Counted as SEE errors all values with deviation > 4σ
- Inspection for burst errors

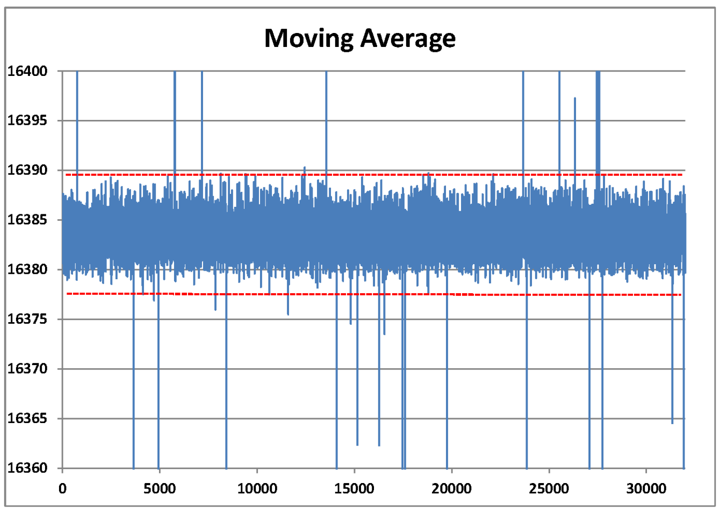
ADC Output Post-processing

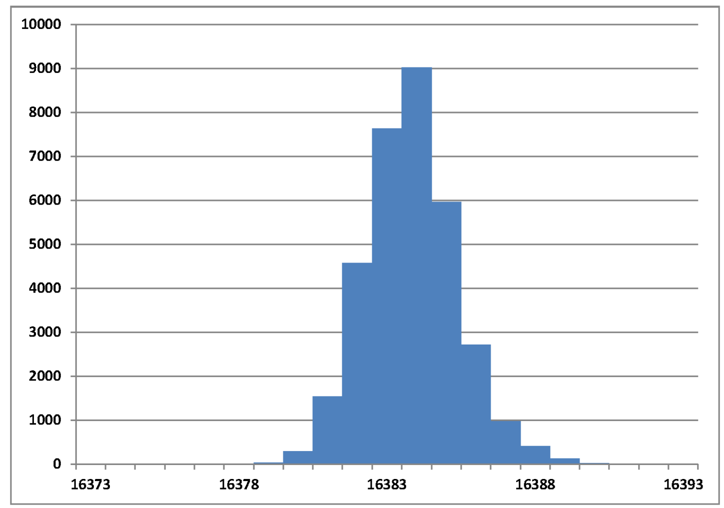
- Calculate σ_1
- Apply linear detrending, not counting points outside $4\sigma_1$, to remove long-term linear drift
- Calculate new σ_2
- Apply a moving average to eliminate short-term variations from the baseline. Excluding points outside $4\sigma_2$
- Calculate σ_3
- Count as SEE errors those points falling outside $4\sigma_3$

Converter Output -Histogram

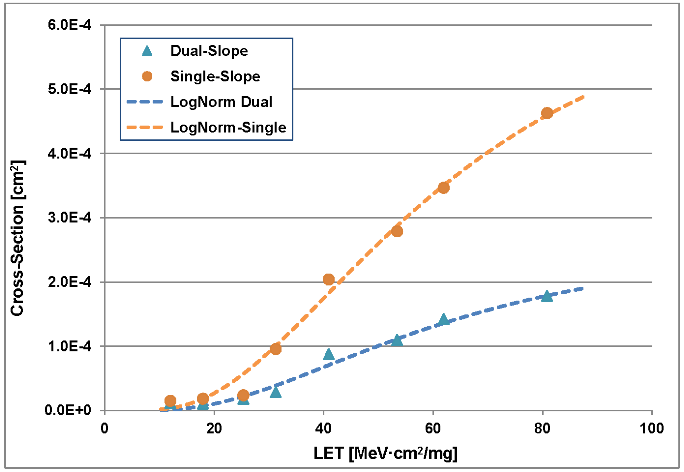








ADCs Cross-Sections and RMS error

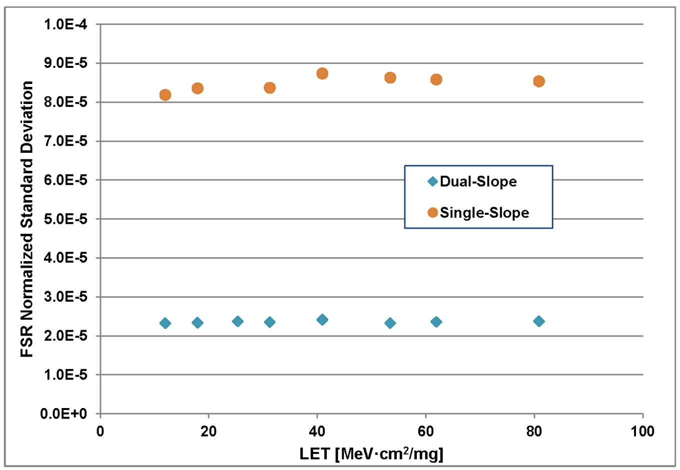


Cross-sections calculated counting as errors all the output values with deviation larger than 4σ.

Larger cross-section for Single-Slope ADC due to:

a) burst-errors

b) longer time window (ramp generator not reset)

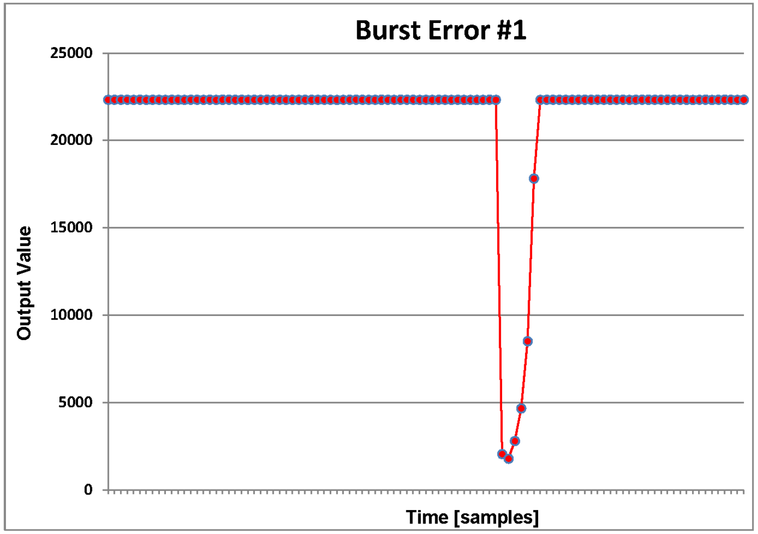


After post-processing and exclusion of the values outside 4σ, the standard deviation is not affected by SEEs, even with the high ion flux used in the experiments (10^4 ions·cm^{-2}·s^{-1})

Event Rates in ADCs

- Calculated from ADC cross section and ion flux rate as function of deposited energy in GEO environment
  - Deposited energy spectrum obtained with CREME-MC, using as sensitive volume the largest diffusion in the Flip-Flop (worst-case assumption)
  - Cross-section expressed as function of deposited energy, assuming z = 1μm
  - Error rates for deposited-energy slots obtained combining both curves
- Estimated error rates (GEO, GCR_{max}, 100 mils Al):
  - Dual Slope: $2.1 \cdot 10^{-5}$ day^{-1}
  - Single Slope: $3.4 \cdot 10^{-5}$ day^{-1}

Single-Slope ADC Burst-Errors



LET[Si]	#Bursts	Avg. Length
11,9	0	0
17,9	0	0
31,2	2	2,5
40,9	12	3,0
53,4	22	4,4
61,9	32	3,2
80,8	72	3,6

- Burst-errors happen simultaneously in the four single-slope converters. Only happen for deposited energy above ~ 30 MeV
- Produced by hits in the ramp generator circuit. Common block, needs time for automatic adjustment of current. It is reset only at power-up.
- Average burst length in the table is given in number recorded samples. At full conversion rate (all samples recorded) the numbers would have to be multiplied by 22 (ratio of time between readings to conversion time)

Summary for SEEs on ADCs

- SEEs do not appear to have a significant effect on the standard deviation (after removing values lying beyond 4σ)
- Cross-section is larger for single-slope converters, mostly due to burst errors. Those are caused by the recovery time of the ramp generator
- Error rates (GEO, at GCRmax, with 100 mils Al)
  - Single-slope: $3.4 \cdot 10^{-5}$ day^{-1}
  - Dual-slope: $2.1 \cdot 10^{-5}$ day^{-1}

Conclusions

- A complete mixed-signal design flow has been applied to the development of a Magnetometer Interface ASIC, using a Radiation-Tolerant digital library developed in-house.
- The ASIC has fullfilled the functional specifications at the maximum expected clock frequency (100 MHz)
- A SEEevaluation has been carried out for the digital and analog sections, and results confirm adequate hardening for interplanetary and geostationary missions.
- Future work will try to improve the single-slope converter to reduce burst-errors, and develop additional cells for the digital library.

Thank you for your attention!