SEE Characterization of a Magnetometer Front-End ASIC Using a RHBD Digital Library in AMS 0.35µm CMOS

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Abstract

A radiation-hardened-by-design (RHBD) digital library, developed for the Austria Microsystems (AMS) 0.35µm CMOS technology, has been applied in a mixed-signal ASIC that operates as a multi-channel data acquisition system for magnetometers using anisotropic magneto-resistances (AMR) as sensing elements. The circuit has been tested in the Heavy-Ion facilities of the Université Catholique de Louvain-la-Neuve (HIF-UCL). The experimental results demonstrate a LET threshold of 16.5 MeV·cm^2/mg and absence of latchup up to 80.8 MeV·cm^2/mg. This radiation-tolerant performance is obtained at the cost of a penalty in area and power with respect to the unhardened technology.

I. INTRODUCTION

This work is part of a planned long-term effort and collaboration between Instituto de Microelectrónica de Sevilla (IMSE), Universidad de Sevilla (US), and Instituto Nacional de Técnica Aeroespacial (INTA) to develop the infrastructure (design flow, technology characterization, libraries) needed for the development of space-grade circuits. The results are initially being applied in the design of scientific instrumentation for missions to Mars.

There is currently a trend in space applications towards small sized (nano-, pico-) satellites that is putting the development of spacecrafts at the reach of small industrial and academic groups. More than in other space applications, small weight and size together with a reasonable development cost are a strict requirement for components in that type of small satellites. The availability of an affordable and performant mixed-signal ASIC technology with known radiation behaviour will help in the design of the instrumentation for those miniature spacecrafts.

This paper presents the results of SEE tests carried out in the cyclotron facilities of UCL using as test vehicle an ASIC, implemented in the AMS 0.35µm CMOS technology, and designed to serve as a 16-bit mixed-signal front-end for a tri-axial magnetometer using low-cost anisotropic magneto-resistances (AMR) as sensing elements.

The following sections briefly present the system and circuit description and give details about the SEE characterization and test results. More details on system and circuit can be found in references [1-2].

II. SYSTEM DESCRIPTION

Fig. 1 shows a simplified block diagram of the proposed triaxial magnetometer. Only one of the three axes is shown in the diagram for simplicity. The magnetometer comprises two main elements, the first one is a linear magnetic field sensor that provides an output voltage proportional to the applied

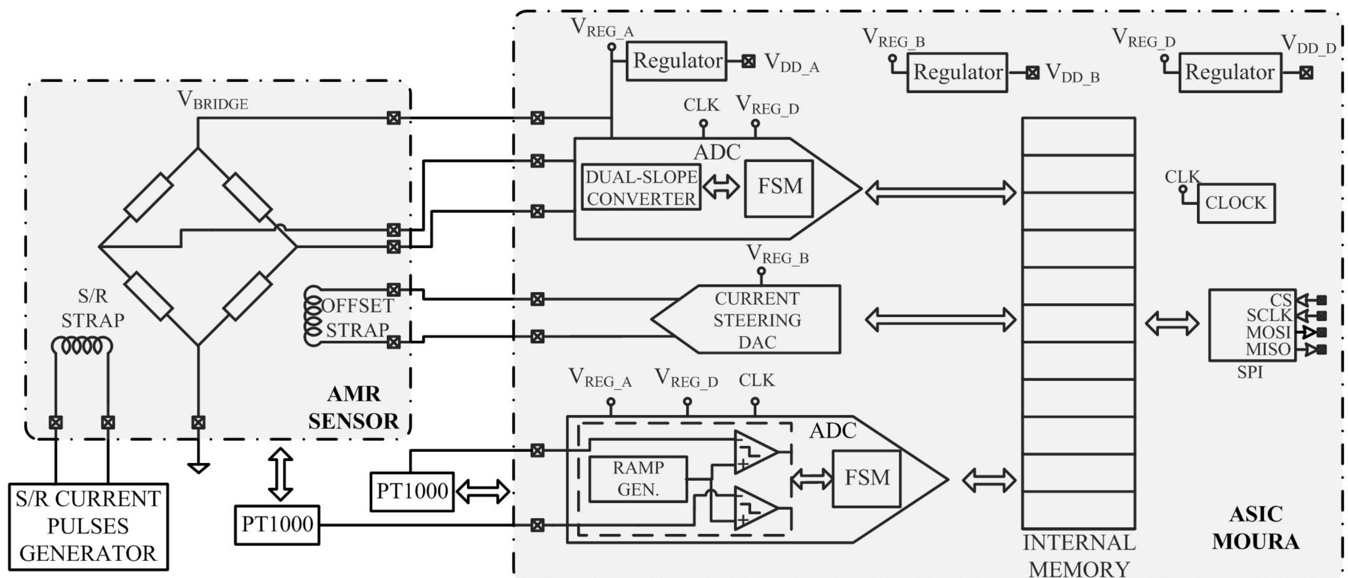

Figure 1: Block diagram of the full system, including external magnetic field and temperature sensors.

magnetic field in the sensitive direction. The second one is a mixed-signal ASIC wich is responsible for conditioning and digitizing the voltage signal from the sensor. The ASIC also performs calibration functions, and communications tasks to capture the ADC outputs and upload system configuration parameters. It has been designed with a high level of configurability that makes possible its use in other space applications with a need for a set of rad-hard low-speed high-resolution ADCs and/or DACs.

The ASIC has been designed in the 0.35 µm CMOS technology from AMS. The circuit is able to work with two alternative AMR sensors having different sensitivities. Their maximum ranges and resolutions are ±1 G, 30 µG for the high-sensitivity type and ±3.3 G, 100 µG for the type with low sensitivity. The ASIC contains six dual-slope 16-bits ADCs that permit the simultaneous capture of the signals from two triaxial magnetosensors. When a 100 Mhz main clock is used, the resolution of those ADCs is 16 bits (15 bits plus sign) at a maximum sampling frequency of 2.6 kS/s and 12 bits (11 bits plus sign) at 20 kS/s. In addition the chip contains four general purpose single-slope ADCs, using self-biased comparators, with a resolution of 15-bit at a maximum of 3 kS/s (10-bit at 77 kS/s) and three 9-bit monotonic current-steering DACs. Two finite-state machines (FSMs) control the operation of the dual-slope and the single-slope ADCs. All the operation and configuration options are programmed in an internal register bank that also stores the output values of the ADCs. The internal memory is read and written using a Serial Peripheral Interface (SPI). The converters clock frequency is programmable up to 100 MHz. The chip has a total area of 4.5 mm x 4.5 mm. The complexity of the digital part is approximately 7 kgates.

A detailed description of the circuit, covering the operation of the dual- and single-slope converters is given in [1].

III. SEE TESTS

A SEU Tests

SEU tests have been performed using as test vehicles the 208 bits of the configuration registers included in the chip. During SEU tests, the registers are written once and then read repeatedly under control of an FPGA through the SPI port at a rate of 35 times per second, comparing each time the values read with those previously written. Any discrepancy is considered a SEU and recorded in a file. Once a SEU has been recorded, the registers are rewritten and the upset monitoring process continued.

Irradiation was carried out at the UCL-HIF using ion cocktail #1 (high-LET). An efective flux of 10^4 $cm^{-2}\cdot s^{-1}$, was used for the ions with lower LET (up to Ar at 55º), and $5\cdot10^3$ $cm^{-2}\cdot s^{-1}$ for the higher LET ions. Irradiation was stopped after reaching a total fluence of 10^7 $ions\cdot cm^{-2}$ for the lower LET ions, or until $5\cdot10^6$ $ions\cdot cm^{-2}$ for higher LET ions. At least 200 errors were recorded in all tests with the lowest fluence. Two different ASIC samples were tested.

Because the ion energies are located around the Bragg peak, LET values have been corrected to take into account the effect of the top passivation, metal and oxide layers situated over the active surface of the sensitive junctions. Multiple bit errors in the same reading are assumed to be caused by SET and removed from the SEU error count. This is reasonable given the very low probability of two ions hitting the sensitive area within one polling period lasting only 35 milliseconds. Cross-sections for oblique incidence have been corrected to take into account geometric effects, assuming an RPP model, and adjusted to Weibull and Log-Normal curves [3]. The results are shown in Fig. 2, that also gives a comparison with the results obtained in measurements performed in other chips using an earlier version of the RHBD digital library [4]. LET threshold has increased from 12 to 16.5 $MeV\cdot cm^2\cdot mg^{-1}$, at the cost of a slightly larger saturation cross-section and power consumption. The new library shows a considerable level of hardening, with a FoM of $3.78\cdot10^{-10}$ $MeV^2\cdot cm^2\cdot mg^{-2}$ [5], resulting in an estimated upset rate of $3.59\cdot10^{-8}$ $upsets\cdot bit^{-1}\cdot day^{-1}$ for a 90% worst-case geostationary orbit with 100 mils of Al shielding [5].

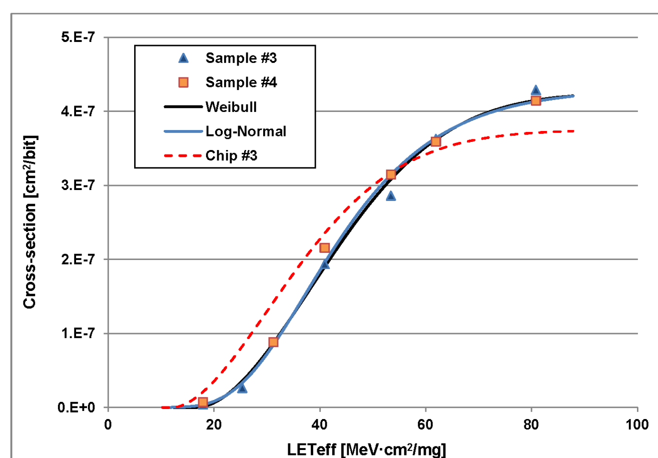

Figure 2: SEU cross-sections comparing current (MOURA) and previous (CHIP#3) RHBD libraries

B Data Converters

The analog circuitry of integrating converters, because of its inherent low-pass characteristic should not be much affected by SETs; however, the combinational and sequential elements in the digital counters and in the Finite-State Machines (FSMs) controlling the operation of the converters can be more sentitive to SEEs, and are assumed to be the reason for the output values showing large deviations from the expected value. Ion-hits in sensitive nodes of the analog circuitry can produce random charge injections that together with hits in the LSBs of the counters should be assumed to be responsible for any increase in the standard deviation (larger RMS error) in the output values. For those reasons, the effect of heavy-ion radiation on the A/D converters has been evaluated using two different metrics: the change in the RMS error (standard deviation) and the number of samples laying outside a +/-4σ interval centered in the mean value.

During the irradiation period a fixed input voltage, close to the middle of their positive range, was applied to the input of the data converters. The converters operated continuously with a clock frequency of 25 MHz, giving a conversion time of 2 ms for the dual-slope converters and 1.3 ms for the single-slope converters. The converter outputs were read 35 times per second, and their output values stored for later processing. Approximately thirty thousand values per converter were stored for each LET value.

Because the converters are reset at the beginning of each conversion, only the ion fluence during the conversion time has to be considered for each reading. Therefore the total fluence applied during the experiments has to be scaled by a factor given by the the ratio of conversion-time to time-between-readings (0.069 for dual-slope, 0.045 for single-slope).

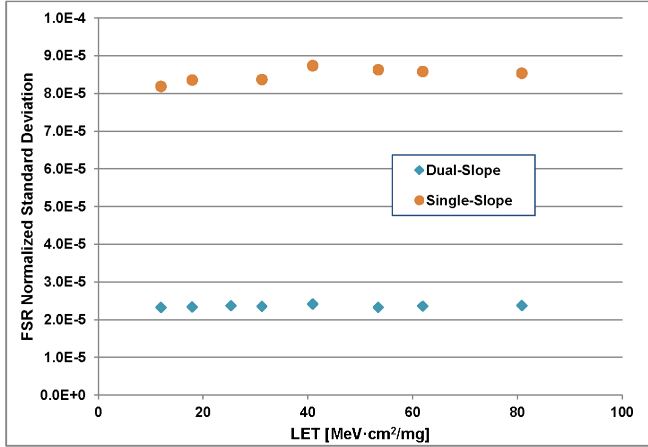

Figure 3: Normalized Standard Deviation versus LET for Single- and Double-Slope AD converters

The long series of experimental datapoints, collected for each LET value during an interval of around 15 minutes, shows drift caused by temperature, electrical interferences and TID effects that can be comparable or even larger than the RMS error. Therefore all those effects have to be removed as much as possible by postprocessing to be able to determine the number of errors that can be attributed to SEEs and not to other random errors. Post-processing of the converter data has been performed in four steps: a) the standard deviation for each converter was calculated, and those output values with a deviation larger than 4σ were excluded from the measurement set; b) linear detrending coefficients were then obtained from the reduced dataset and applied to the original data set; c) a new standard deviation was then calculated using the detrended original data, and the values beyond 4σ excluded to leave a new reduced data set; d) a moving average was applied to filter short-term baseline variations, and the final value for σ was obtained from that reduced dataset. Points falling outside four times the final σ have been considered as measurement upsets due to ion-hits in the converters and used to determine the converter error cross-section. The 4σ used to differentiate bad measurements corresponds to approximately 6 LSBs for the dual-slope converters, and 12 LSBs for the single-slope type.

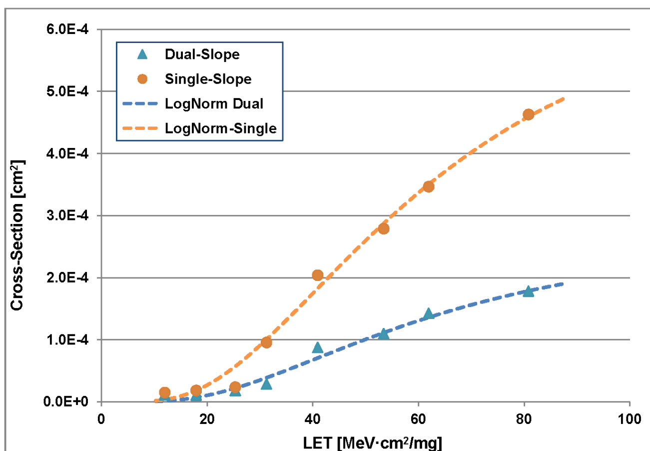

Figure 4: Log-normal cross-section of single- and dual-slope data converters for errors larger than 4σ

Figure 3 shows the the dependence with LET of the standard deviation normalized to full-scale range of the single and dual-slope ADC outputs. Although conditions in the irradiation chamber are not ideal for high resolution measurements, the recorded RMS errors are similar to those obtained in standard laboratory conditions, and are not affected at the highest LETs measured. After post-processing, eliminating the datapoints with deviations larger than 4σ, the RMS error is approximately 1,5 LSBs for the dual-slope ADC, and 2,5 LSBs for the dual-slope ADC.

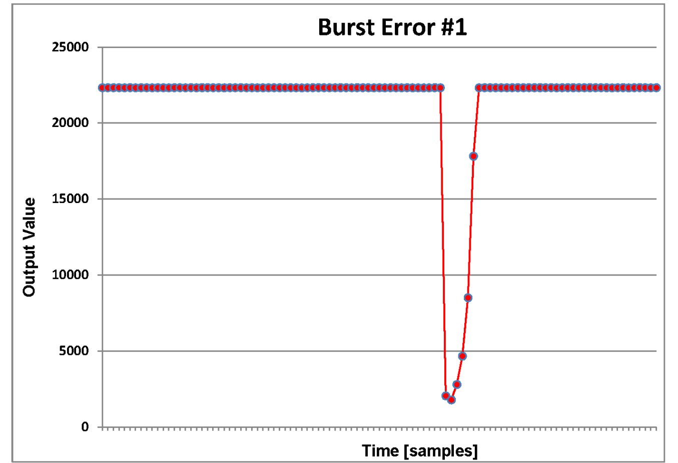

Figure 5: Burst error at the output of a single-slope converter

Fig. 4 presents the converter cross-sections for errors larger than 4σ and a log-normal approximation using a least-square fit of the data points. From the log-normal parameters the saturation values are $2.63 \cdot 10^{-4}$ cm^2 for the dual-slope converters, and $6.70 \cdot 10^{-4}$ cm^2 for the single-slope type.

The larger cross-section of the single-slope converters can be partly explained by the effect of ion-hits in the circuit for automatic adjustment of the ramp slope. Although the converter counters are reset at the beginning of every conversion cycle, an error in the ramp controller, which is common to all four converters will last for several cycles, effectively increasing the exposure time window and inducing a burst of erroneous measurements. An example of such an occurrence is shown in Fig. 5. The dots represent samples spaced 35 ms.

Table 1: Number and average length of burst errors

Ion	Angle	LET[Si]	Burst Errors	Average Length
Ne	55	11,9	0	0
Ar	0	17,9	0	0
Ar	55	31,2	2	2,5
Kr	0	40,9	12	3,0
Kr	40	53,4	22	4,4
Xe	0	61,9	32	3,2
Xe	40	80,8	72	3,6

The number of registered burst errors and their average

length (in number of measured samples) at different LET values is shown in Table 1. The errors happen simultaneously in all the four single-slope channels of a chip, confirming that their origin is in the ramp controller. It has to be taken into account that only one in 22 samples are read during the experiment, so for a converter running at full speed the length of the error bursts would need to be multiplied by 22.

C Converter Error Rate

To get an estimation of the converter error rate in geostationary orbit, the experimental cross-section data are translated to the probability of deposited energy over the track of the incident ions in the sensitive volume. To have a worst-case analysis, the largest drain diffusion in the FSM latches was taken as the sensitive volume to calculate the deposited energy. The integral spectral distribution of ions versus deposited energy in a given environment can be obtained using CREME-96 [6], and combining it with the measured cross-sections allows to estimate the error rate for that environment. As an example, for a geostationary orbit, at the maximum of cosmic rays flux, and with 100 mils of Al shielding, the estimated SEE error rate per converter (values outside 4σ) is $2.1\cdot10^{-5}$/day for the double-ramp converters operating continuously at 500 samples per second and $3.4\cdot10^{-5}$/day for the single-ramp converters operating at 770 samples per second.

IV. CONCLUSIONS

A complete mixed-signal design flow has been demonstrated and tested, using a RHBD digital library and radiation hardening rules for the analog part. The design flow has been applied to the design of a medium-complexity mixed-signal ASIC.

Heavy-ion radiation tests have proved a radiation tolerance to SEEs of the full chip adequate for geostationary orbit applications and for missions to Mars. The robustness against SEE of single and double slope converters is demonstrated.

V. ACKNOWLEDGMENT

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