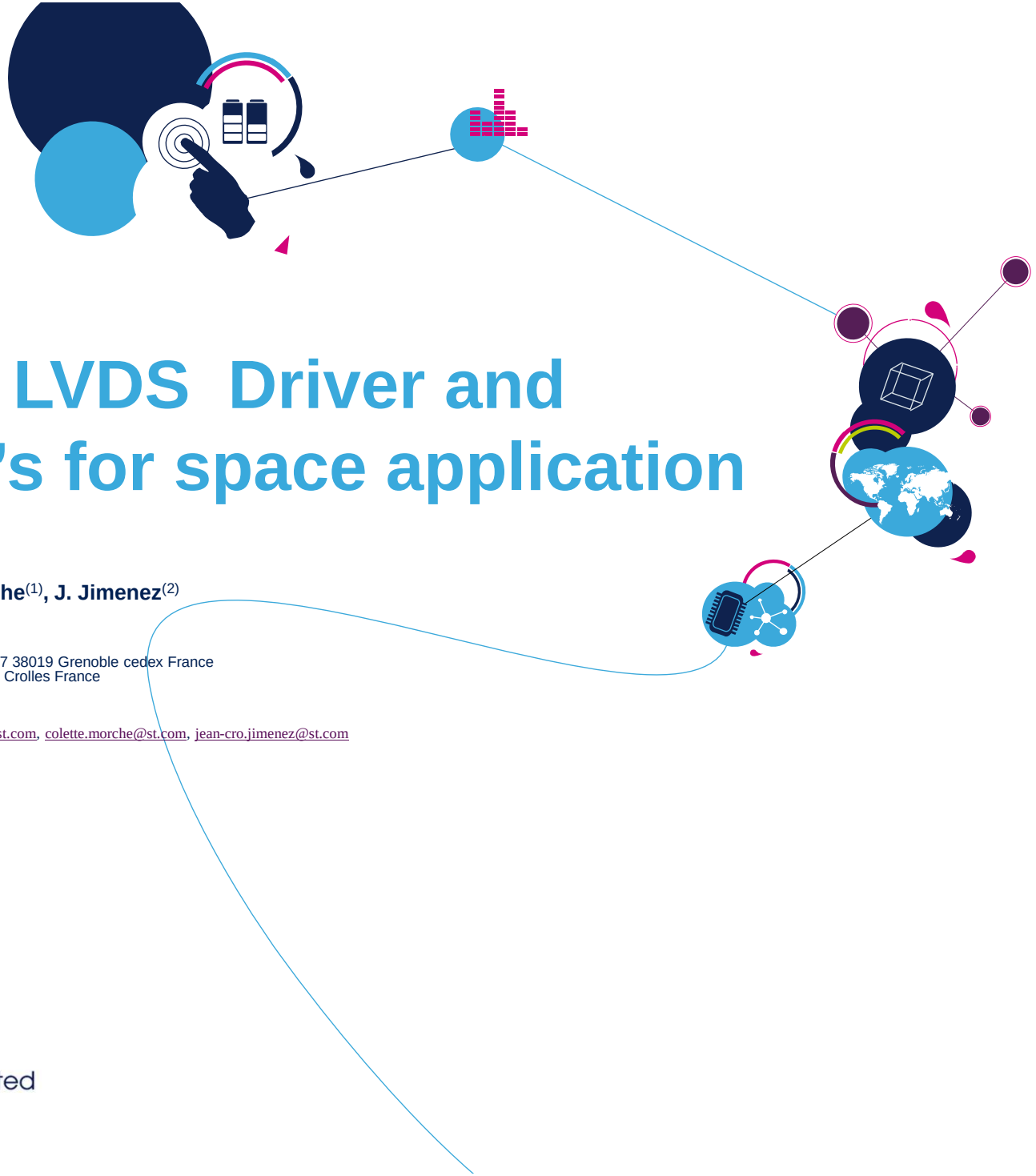

High Speed LVDS Driver and Receiver IC's for space application

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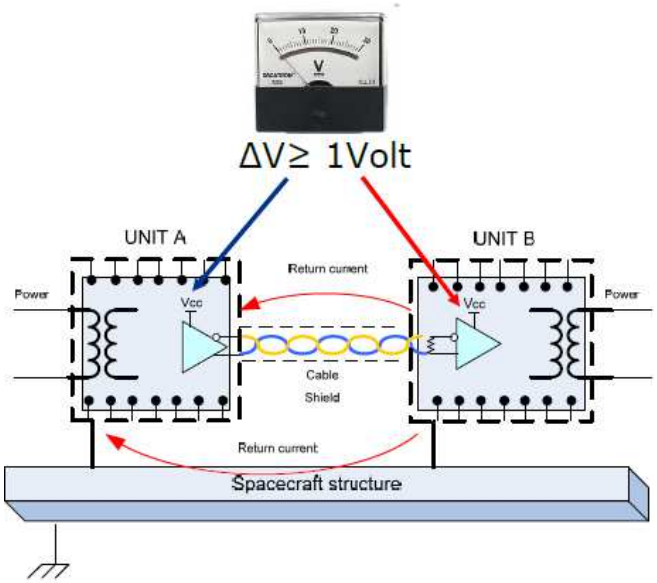
OUTLINE

- Motivation
- Technology
- Circuit design
  - Driver
  - Receiver
  - Cold spare operation
  - Esd protection
- Space specificities
- Measurement
  - electrical results
  - Radiation results
- Conclusion

Motivation

- Low Voltage Differential Signaling
  - LVDS is a serial Digital transmission at high frequency (400Mbits to 4Gbits)
    - Differential voltage +/- 400mV , common mode voltage 1.2 V

- In space application common mode of driver and receiver can be at different potential much higher than 1 volts
- Need at least -4, +5 Volts extended common operation for the receiver
- Need improved ESD performances for LVDS pins at least > 8 kV



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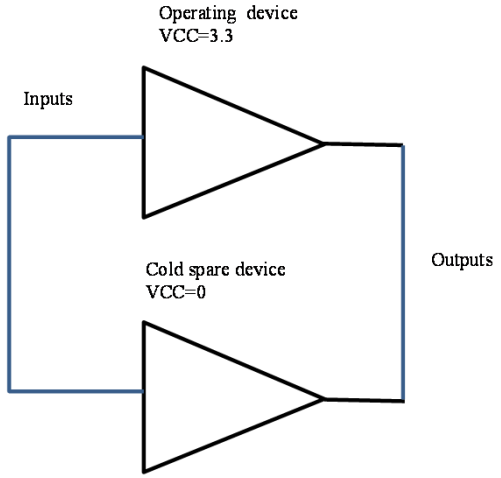
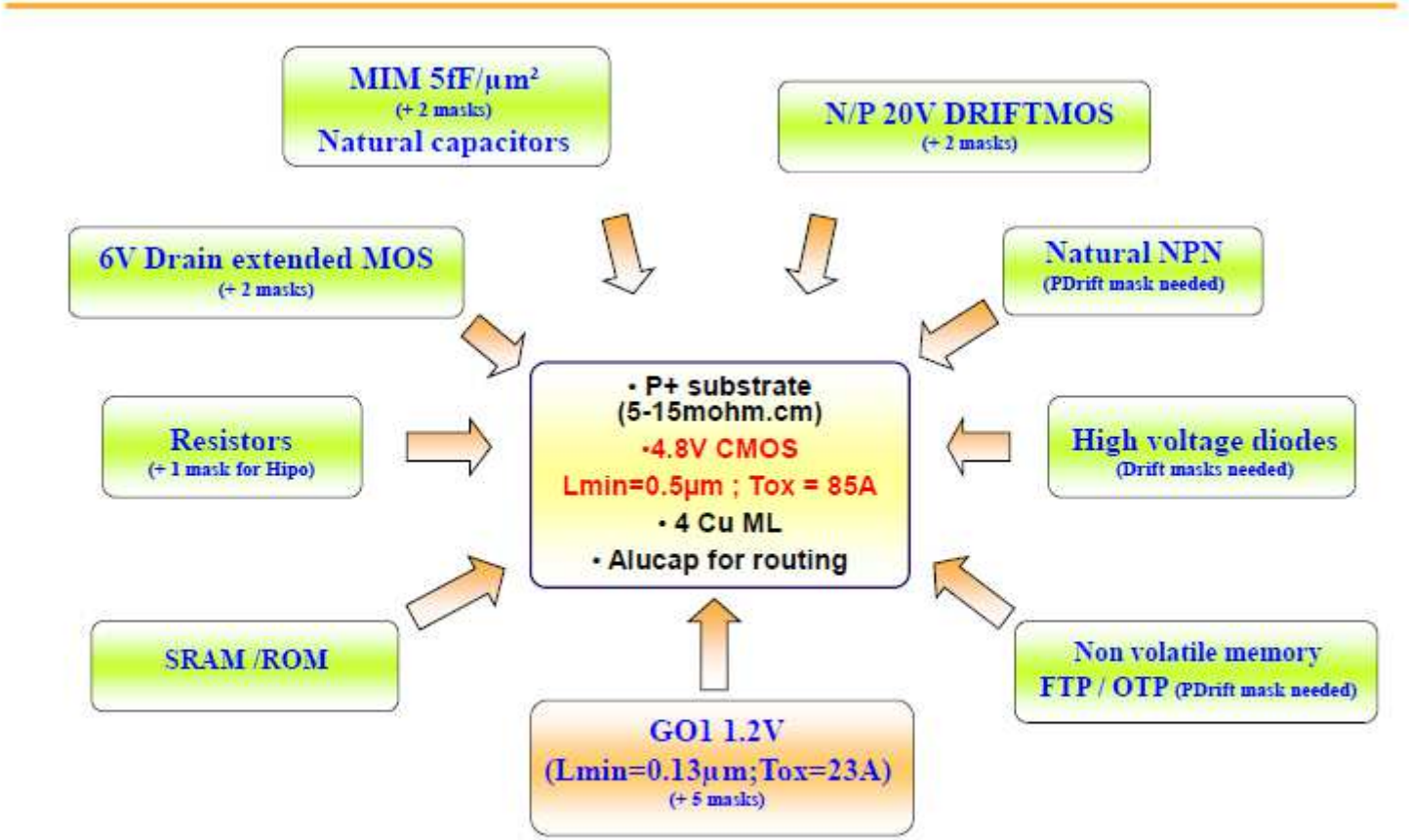
Motivation: Summary of the need

- 400Mb standard quad LVDS driver and receiver
- Extended common mode range for receiver
  - -4V,+5V
- 16 kV HBM to ground for LVDS pins
- Cold spare operation for all pins
- Fail safe operation
- Guaranteed up to 300 krad TID
- Heavy Ion SEL immune up to 115 MeV.cm²/mg (latch up)



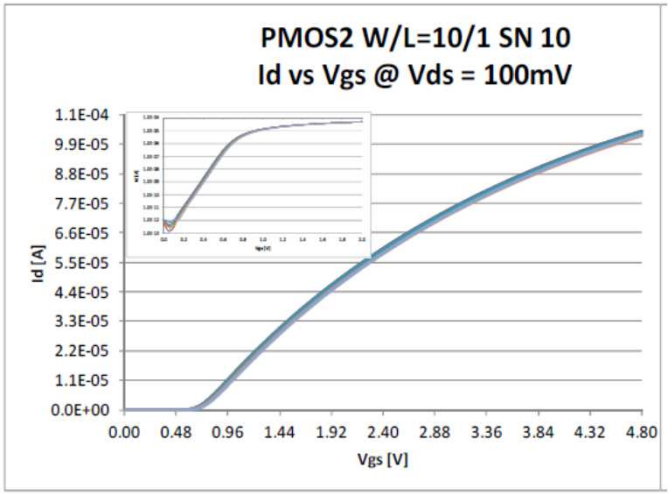
Process: H9A choice

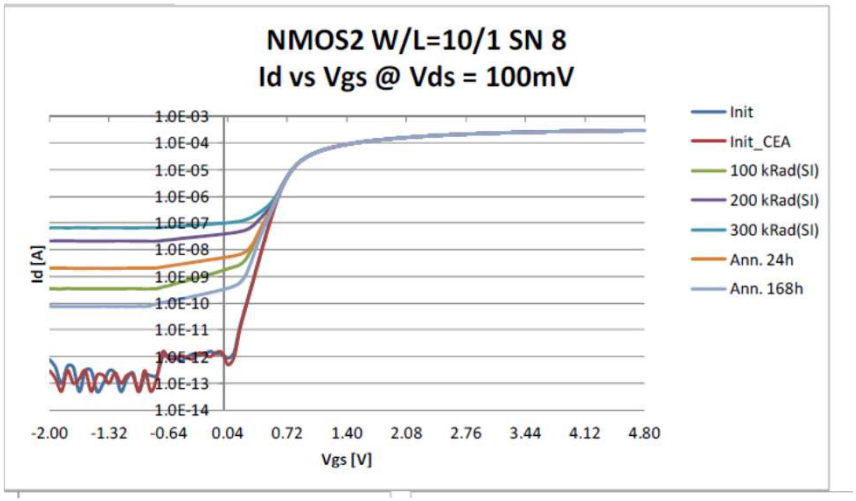
- Standard 0.13um cmos process with double oxyde



H9A: irradiation characterization

- Total ionizing dose (TID) test campaign done on all elementary components of H9A
  - The components have been radiated at high dose rate using a Co60 gamma ray source.





- No Threshold voltage shift observed for both pmos and nmos
- Some leakage on Nmos after 100krad before annealing
- 300 krad target reachable without specific care because schematic not sensitive to leakage current

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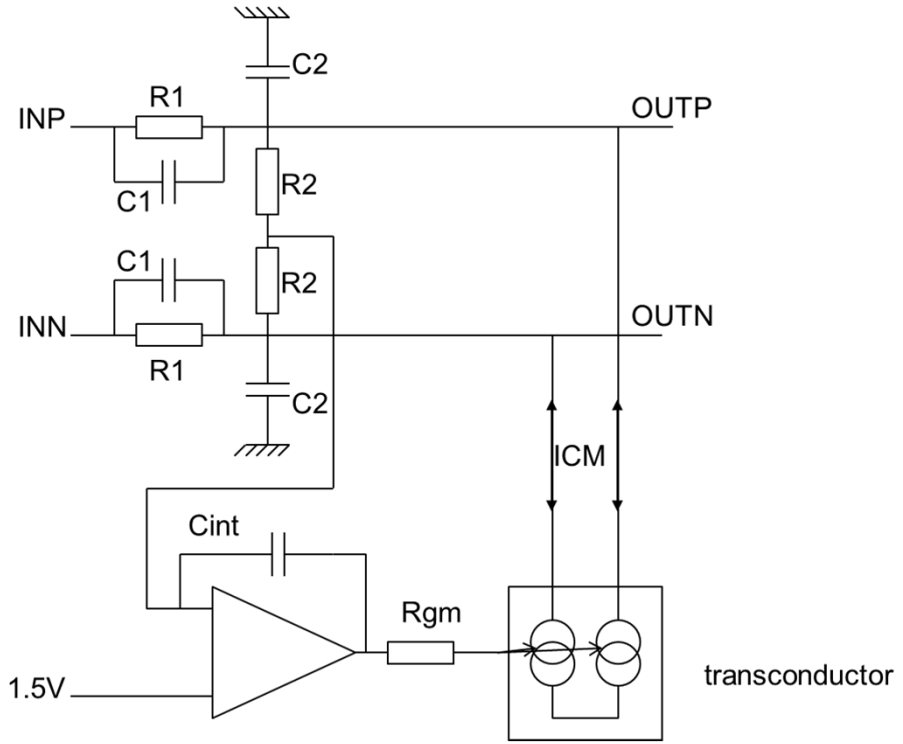
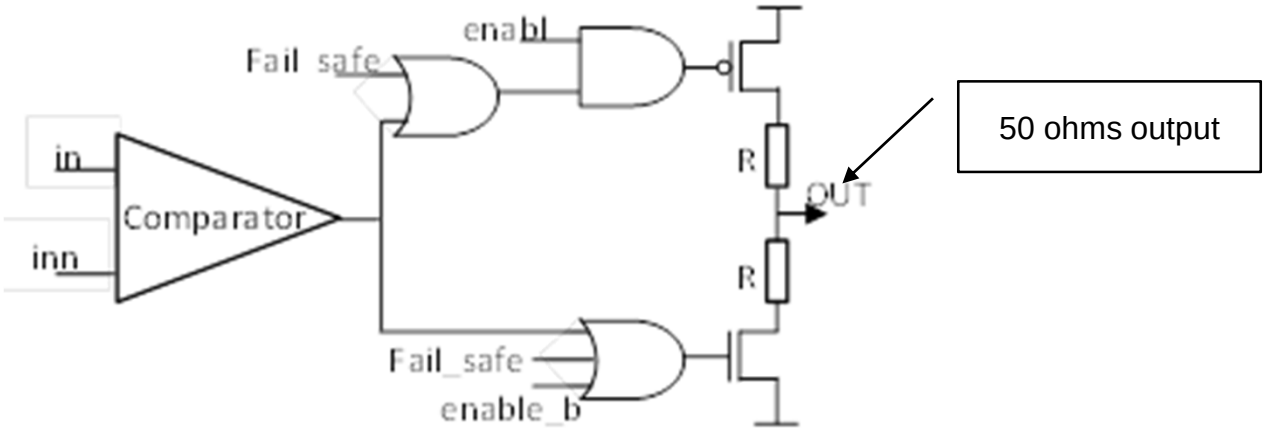
Common mode shifter in receiver

- Common mode voltage input -4, + 5Volts
- shift of common voltage through R1 with Common current ICM
- R2/Cint integrator to stabilize the loop
- C1 added to obtain high bandwidth
- R2/R1=C1/C2=8 to get almost constant gain over bandwidth



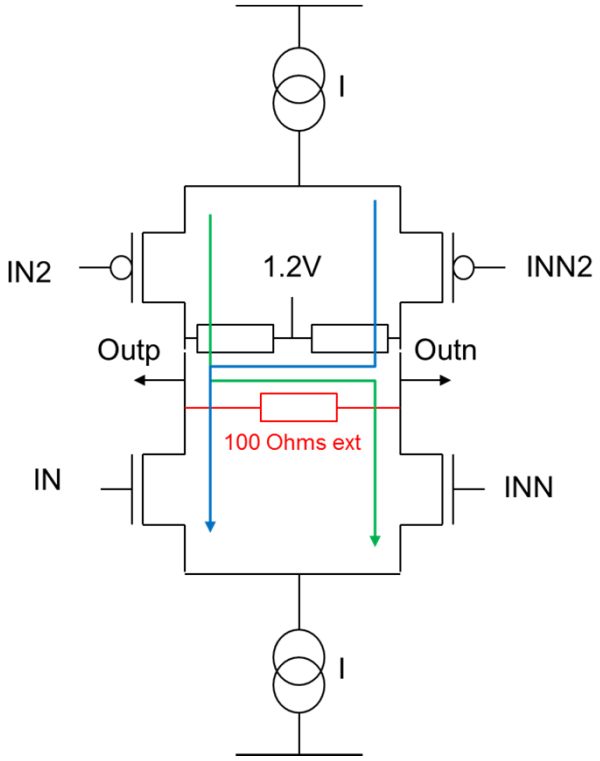
Receiver TTL output



- High speed comparator (1ns) with dynamic hysteresis to perform differential to single ended conversion
- Very large output stage with internal resistor to get 50 ohms constant output impedance over output voltage to minimize line reflection
  - 15 Ohms for transistors
  - 30 Ohms for resistors
- 1.8ns global propagation delay
- Huge peak current on supply voltage (28 mA)
  - High value decoupling capacitor added on chip

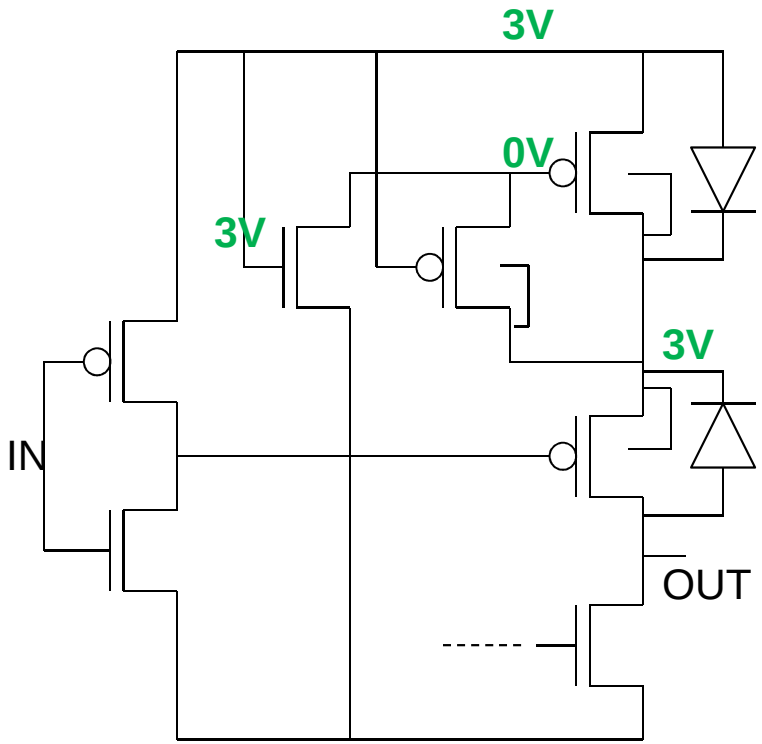
Driver output

- external 100 Ω termination resistor with a voltage swing of Vod=250 to 400mV.
- Output Common mode voltage forced to 1.2V through 2 internal 800ohms resistors connected to a bandgap voltage
- Specific care to match sink and source output current to get proper common mode output
- Typical propagation of whole driver chain 1ns

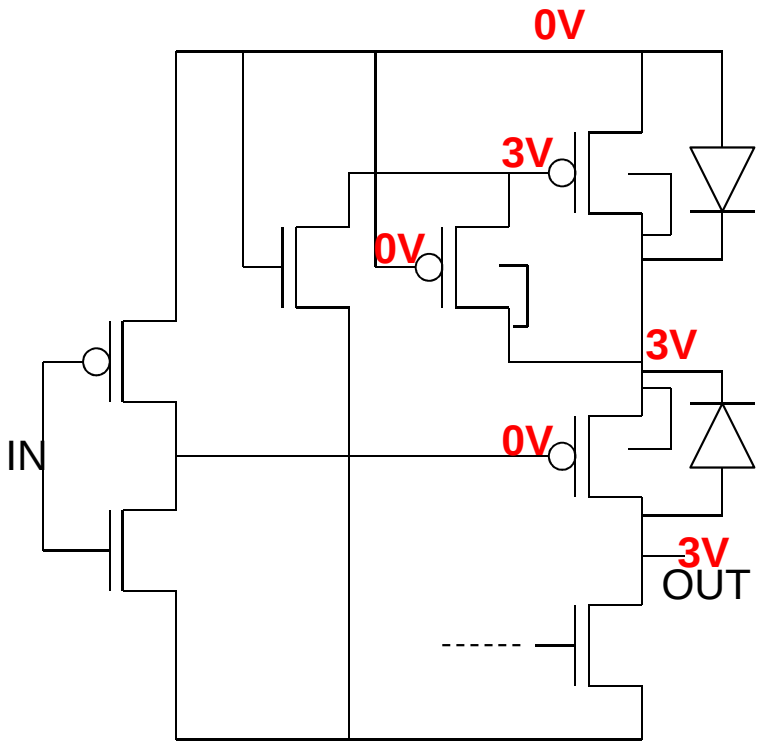


Cold Spare principle of receiver output stage

- Use switched nwell potential with 2 back to back schottky diodes and some tricky transistors



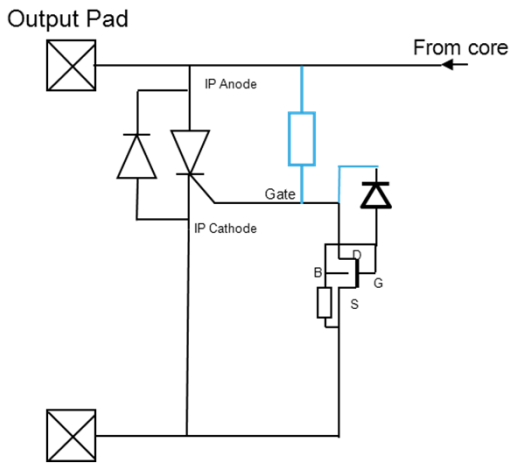
Normal operation

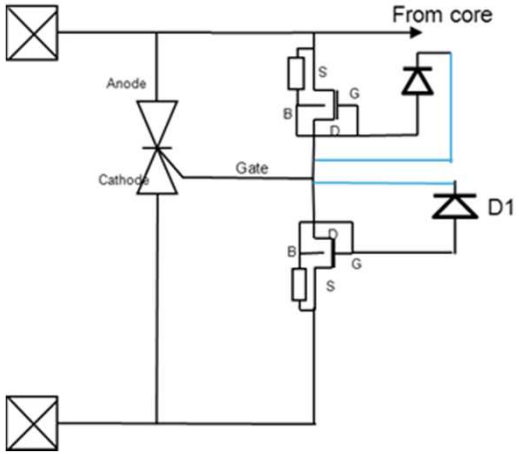


Cold Spare

LVDS ESD PROTECTION

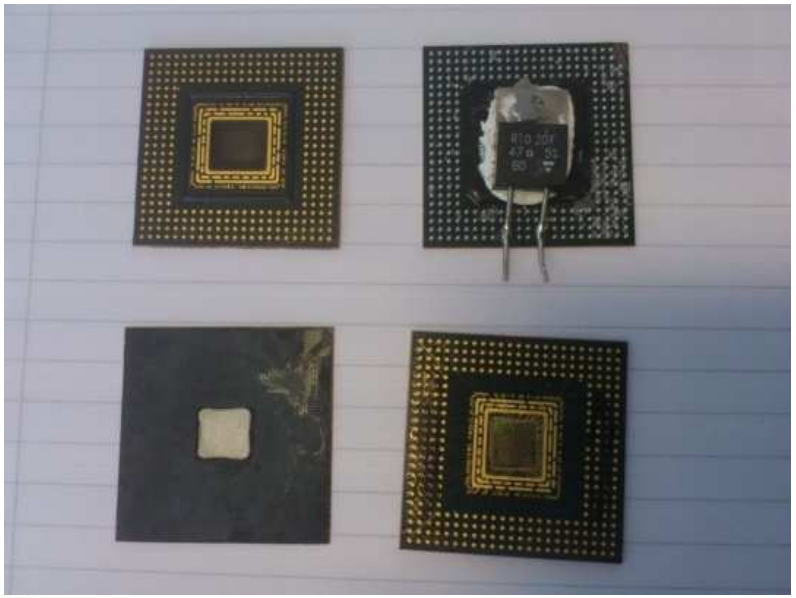
- 2 specific 16KV ESD protection developed by RD ESD team of ST Crolles
- Both protections sustain ±9 Amperes TLP with a maximum overshoot of 8.5Volts
- SCR for the driver output : -0.6 to 6 Volts
- TRIAC for Receiver input: dc -5 to +6 volts
- SEL immunity achieved by adding innovative isolation of triggering systems on second cut

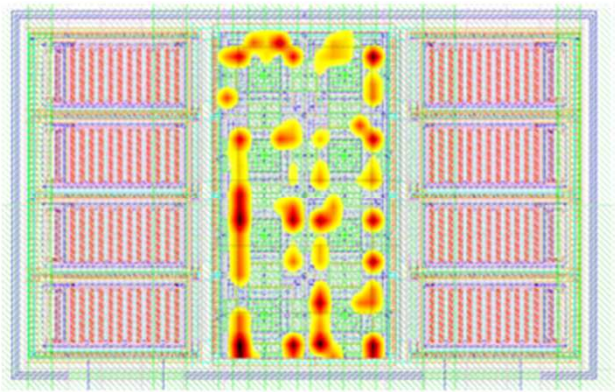




Rad Hard debug: Laser test

- Laser tests mandatory to finalize the specific ESD structures
- High energy pico laser beam (pulse energy up to 6nJ) focused on the backside of the die
- Special assembly done in SBGA package with removal of cover to get access to backside of the die

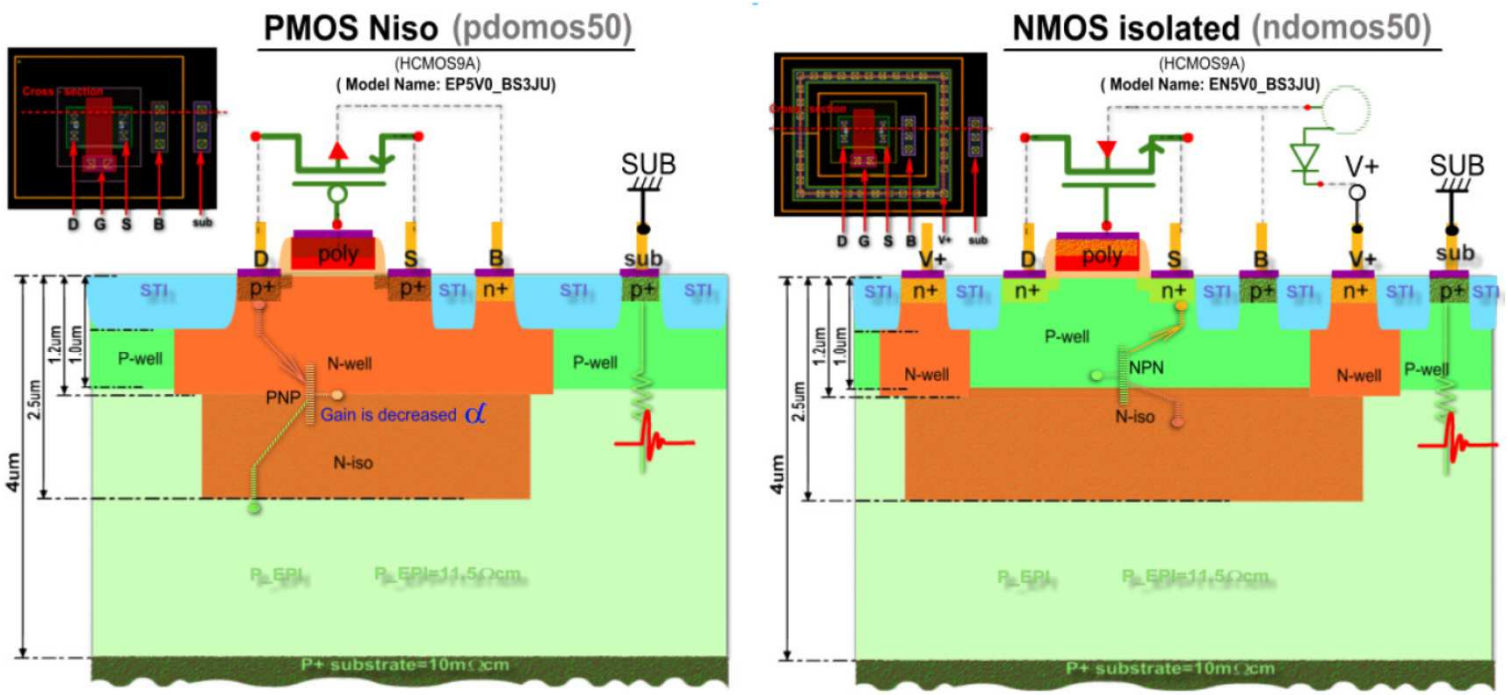




Sensitive areas of first version of Triac

H9A Rad-Hard guidelines

- Total dose immunity provided by process
- Single Event Latchup (SEL) immunity guidelines given by ST RD radhardening team at Crolles:
- 100% deep nwell coverage : all transistors are isolated



- Continuous well tapping at NWell & PWell edges
- Continuous substrate tapping at DNW edges

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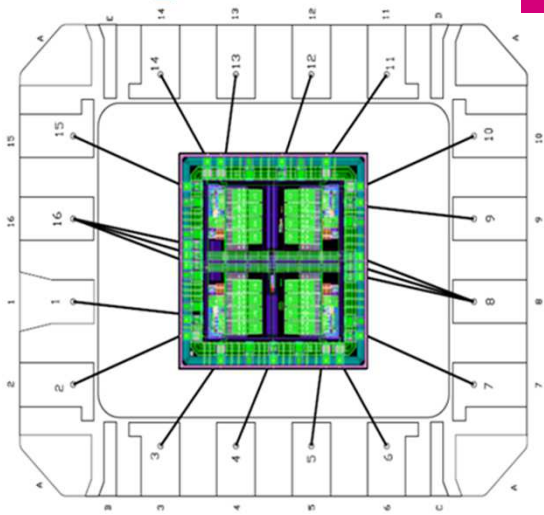
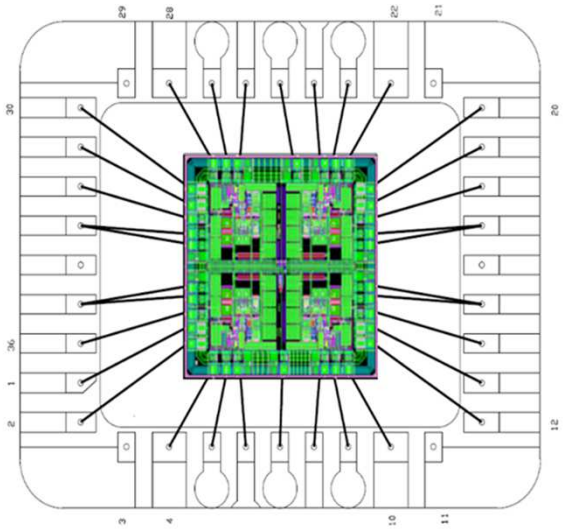
Package layout

- Flat 16 standard package for both quad drivers and quad receivers
- Both dies are 2.1*2.1mm
- For receiver huge peak current generated in TTL output buffers (> 120mA)
  - Large on chip decoupling capacitors added
  - One couple of supply pads per channel in order to minimize this crosstalk
  - Development of dedicated package to get a standard pinout



Driver, die and package

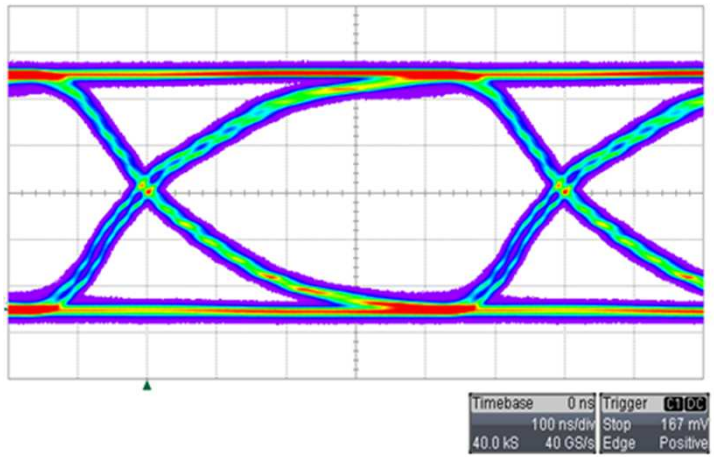


Receiver, die and package

Silicon Results

- Big efforts and specific equipment needed to measure propagation delays with good accuracy (better than 100ps).
- propagation delay measured around 1.85ns for the receiver with common mode input from -4 to +5Volts
- eye diagram done with a driver connected to a receiver through a long length line
  - Total jitter 600ps
  - Random jitter 20ps
  - determinist jitter of 330ps

LVDS Receiver, propagation delay



LVDS Driver +Receiver eye diagram

Silicon results summary

- 300krad in high dose rate successfully achieved
- No SELs observed with the LET equivalent value of 110MeV.cm²/mg
- No SET detected with a LET of 32.6 MeV.cm²/mg at 25 degrees

- Tables below summarize achieved performances

		Specification LVDS driver			Measure	Specification LVDS receiver			Measure
symbol	Parameter	Min	Typ	Max	Typ	Min	Typ	Max	Typ
ICCL	Total enabled supply current		20mA		16.5mA		15mA		12.5mA
tPHLD	Propagation delay time, high to low			1.9ns	0.95ns			3.1ns	1.85ns
tPLHD	Propagation delay time, low to high			1.9ns	0.95ns			3.1ns	1.85ns
tr / tf	Output signal rise / fall time		1.2ns		0.82ns		1ns		0.87ns
ESD	HBM: LVDS inputs		8kV		OK		8kV		OK
ESD	HBM: all other pins		2kV		OK		2kV		OK
TID	High Dose Rate (50-300 rad/sec)	300krad			OK	300krad			OK
Heavy-ions	SEL immunity (at 125) up to:	110MeV.cm²/mg			OK	110MeV.cm²/mg			OK

LVDS driver summary table

LVDS receiver summary table

Conclusion

- Quad LVDS driver and quad LVDS receiver described in this paper have been processed in a 0.13um standard CMOS STMicroelectronics technology
- The chips have been successfully validated
- Radiation characterization and stress test have been done, to ensure 300 krad TID , SEL free at 115Mev.cm2/mg and at least 8 KV ESD to ground on LVDS pins
- Both chips have been QML V qualified this quarter
- 2 other LVDS chips not in this presentation sharing same IP's
  - RHFLVDSD2R2:dual LVDS driver-receiver
  - RHFLVDS228A : dual 4x4 crosspoint LVDS switch

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- Thanks for your attention