Rad-hard High Speed LVDS Driver and Receiver

T. Masson[(1)], S. Nicolas[(1)], C. Morche[(1)], J. Jimenez[(2)]

(1) STMicroelectronics 12, rue Jules Horowitz BP 217 38019 Grenoble cedex France
(2) STMicroelectronics 850 Rue Jean Monnet 38920 Crolles France

Email : thierry.masson@st.com, sandrine.nicolas@st.com, colette.morche@st.com, jean-cro.jimenez@st.com

Abstract

A LVDS driver and a LVDS receiver have been processed in a 0.13um CMOS STMicroelectronics technology. It can operate over a large common mode input range from -4V to +5V, using a new architecture, to ensure immunity of ground shifting and driver offset voltage, while supply voltage is from 3 to 3.6V.To this aim, the common voltage input is sensed and adjusted to a fixed reference voltage 1.5V with an integrator loop and a class AB transconductor. These devices support data rates of 400 Mbps or 200 MHz .

These two LVDS circuits are designed for space applications. A total ionizing dose test campaign on elementary components has been performed to investigate the technology radiation hardness. The components have been radiated at high dose rate using a C060 gamma ray source. Specific mitigation techniques to achieve best in class hardness to total ionization dose and heavy ions have been applied. Moreover, the chosen technology has a substrate with very low resistivity which is very useful to decrease risks of latch up in general and more specifically Single Event Latch up.

One major challenge of these LVDS circuits has been to meet particular ESD specifications which were 16KV on LVDS receiver input and driver output combined with SEL immunity. Laser tests have been useful to best understand their behavior regarding latch up.

Both the receiver and driver have been evaluated in laboratory. Huge efforts and specific equipment have been necessary to measure properly propagation delays closed to 1.7ns with good accuracy (better than 100ps). Finally, 300 krad in high dose rate and 150 krad in low dose rate have been achieved. And heavy ions Single Events Effects tests have also been performed with good result

I. INTRODUCTION

A big challenge in data transmission is the constant increase in data-rate. Low Voltage Differential Signaling (LVDS), and high speed, low power general purpose standard interface is one of the key building blocks in transmission systems.

This paper presents LVDS driver and receiver circuits specifically designed, packaged and qualified for use in aerospace environment. The intended application of these devices (RHFLVDS31/32 quad drivers/receivers) is point to point baseband data transmission over controlled impedance media with a 100 Ω characteristic impedance. These devices support data rates of 400Mbps.

The Driver accepts low voltage TTL input levels and translates them to low voltage (350mV) differential output signals.

At the receiver side, a low voltage (100mV) differential LVDS input signals is transformed into TTL output levels. Moreover, a new architecture has been proposed in order to tolerate a large common mode input range (from -4V to +5V). It ensures immunity to ground shifting and to driver offset voltage, while supply voltage can vary from 3 to 3.6V.

These circuits feature an internal Fail-safe function to ensure a known state in case of shorted or floating inputs. In addition, all the pins have cold spare buffers to present a high impedance when VCC is tied to GND.

This paper is organized as follows: section II describes the configurations using these LVDS products. The design of driver and receiver are developed in section III. Section IV deals with Space specificities and cautions that have been taken in order to harden the design and the layout to the radiations.

Sections V et VI present respectively the ESD protections and the package used. Measurements results, electric and radiative follow in section VII. The paper ends with conclusion in section VIII.

II. SPACE WIRE CONFIGURATION USING LVDS

In this paragraph, we will first describe the different possible configurations for the LVDS cells in order to better understand the circuit requirements.

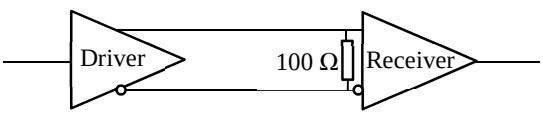


Fig. 1: **Point to point configuration schematic**

The **point to point configuration,** presented in Fig. 1, ensures the minimum discontinuities on the transmission line. It is interesting to avoid any stub problem on the line. A 100 Ω resistor, at the far end, terminates the two differential lines with matched impedance and provides the differential LVDS voltage with output driver current. Under the above conditions, the driver can drive a wire over 10 m at 200 MHz or 400 Mbps.

In the **bi-directional configuration,** shown in Fig. 2, data can flow in both directions, but only one a time. However the bus needs to be terminated at both ends. Therefore, two 100 Ω terminated resistors are necessary. These two resistors in parallel (100 Ω // 100 Ω = 50 Ω) will cut the output driver signal in half.

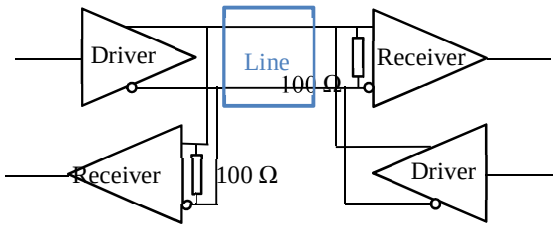


Fig. 2: **Bi-directional configuration schematic**

In the **multi-drop configuration,** described in Fig. 3, 10 receivers or more can be tied to the bus. Some receivers may be powered off while communication is from the driver to other receivers (powered on). However, if the stubs between line and the different receivers are too long, it may create reflections. It can also cause impedance discontinuity.

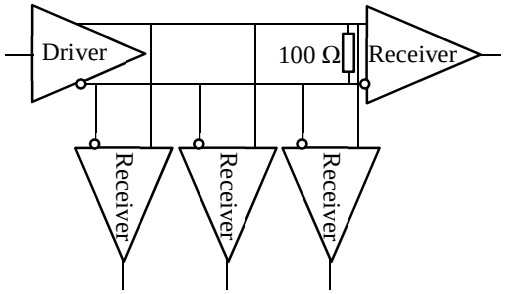


Fig. 3: Multi-drop configuration schematic

To solve this issue, a Receiver, followed by a Driver, can by use as a **Repeater** in the middle of the long line, as presented in Fig. 4.

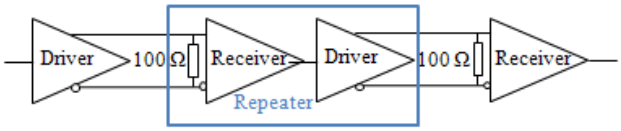


Fig. 4: Repeater configuration schematic

III. CIRCUIT DESIGN

A. *Driver*

The purpose of the Driver (Fig. 5) is to convert low voltage TTL input levels into low voltage differential output signals (350mV).

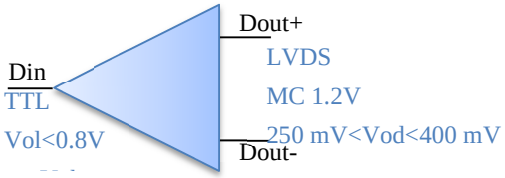


Fig. 5: Driver symbol

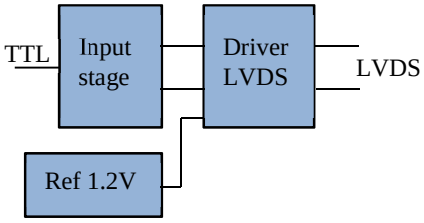


Fig. 6: Driver stages

For that purpose, the architecture depicted in Fig. 6 has been selected. The LVDS driver is mainly composed of two stages in cascade: the first stage is an inverters chain and the second stage a LVDS buffer.

Critical parameters are propagation delays (1.5 ns max), consumption (20 mA) and skew between two drivers (channel to channel skew 0.3 ns max).

The input stage architecture is described in Fig. 7:

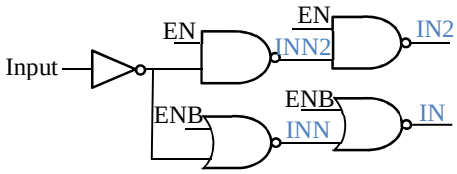


Fig. 7: Driver input stage schematic

A pull down in input, assures a low level in case of floating input. It is the fail-safe mode.

A CMOS band gap with vertical substrate pnp is used to generate the voltage reference of 1.2V stable versus supply and temperature. It is also used as current source for the other blocks.

As the driver block draws a high current, it can disturb the reference voltage. For that purpose, a buffer has been added between the bandgap and the driver in order to achieve a current isolation.

Based on the LVDS standard, defined in ANSI/TIA/EIA-644-A, the driver should be able to drive an external 100 Ω termination resistor with a voltage swing of Vod=250 to 400mV. Meanwhile, the common mode voltage of the output signal should remain within the range of Vos=1.125 to 1.45V. The following structure [1], presented in Fig. 8, has been chosen to meet consumption specifications (17 mA typical and 20 mA max).

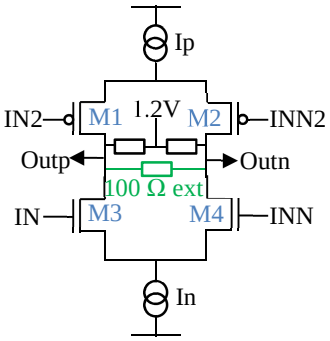


Fig. 8: Driver output stage

In this case, I=Vod/Rext=3.5 mA for 350mV. The drawback of this structure is that it is not 50 Ω matched. The common mode voltage is fixed by two 800ohms resistors connected to the 1.2 volts reference.

In order to minimize the common mode output voltage dc shift, the two current sources In and Ip must have values as closed as possible.

Some cautions, for the gates in input stage, have also to be taken to avoid simultaneous conduction, resulting in uncertainty zone for the outputs. In normal mode IN2=IN and INN2=INN.

For positive input, M1 and M4 are closed,

M2 and M3 are open.

For negative input, M2 and M3 are closed,

M1 and M4 are open.

This design structure is optimized for fast (or short) propagation time. As an example, by limiting the size of the output transistors, the parasitic capacitors are reduced thus improving the propagation time. At layout level, some precautions have also been taken to minimize routing of the critical nodes

B. Receiver

The Receiver, Fig. 9, converts low voltage (100mV) differential LVDS input signals into TTL output levels. It also can operate over a large common mode input range from -4V to +5V

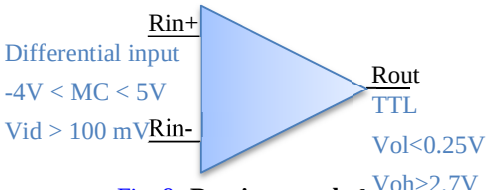


Fig. 9: Receiver symbol

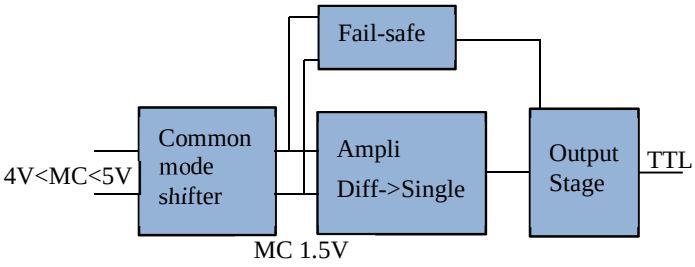


Fig. 10: Receiver stages

As shown in Fig. 10, the LVDS receiver is composed of three stages in cascade: the first one is a common mode shifter, the second one is a differential to single amplifier, and the third stage, an inverter chain, is the output stage.

In parallel with the second chain ,a fail-safe function stage is inserted

The input of the receiver should support a wide common voltage range: from -4V to 5V.The aim of the common mode shifter is thus to guarantee a stable 1.5V common voltage at the amplifier input, independently of this receiver common voltage, without attenuating the differential input signal. The high frequencies of the received signal put stringent requirements on the stability issue.

That's the reason why we finally came to the architecture described in Fig. 11.It has the advantage to isolate the input and the current sources thanks to an integrator.

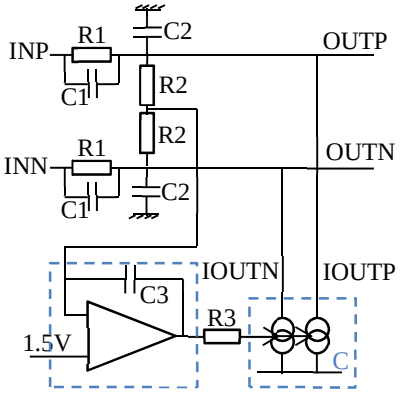


Fig. 11: Common mode shifter block diagram

The common mode shift is done through two resistors R1 in differential and two current sources Ioutp, Ioutn. The common voltage input is sensed and adjusted to a fixed reference voltage 1.5V with an integrator loop (noted I in Fig. 11) and a class AB transconductor, formed by R3 and a current conveyor C.

The system is equivalent to a high pass filter with respect to the common mode input voltage.

As stated before, the differential attenuation has to be as close as possible of unity. At low frequency, it is given by the following relation: DA=R2/(R1+R2)

R1 is chosen to meet input common range current specification for a 5.5V maximum common mode shift .

In parallel to the serial resistor C1, a small capacitor, is added to transfer the high speed LVDS signal (HF differential + HF common mode voltage). Moreover, an additional small capacitor C2 is added to get a flat gain from dc to high frequency. To keep the same attenuation at high frequency (Fig. 12), C2 should satisfy the following relationship:

DA= C1/(C1+C2) = R2/(R1+R2)

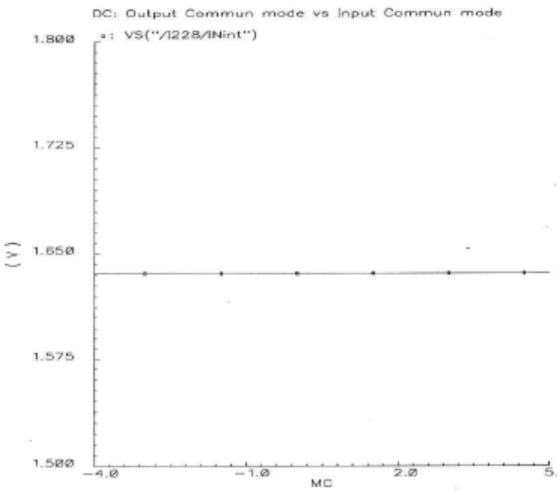


Fig. 12a: Common mode DC transfert function: common voltage is very well cancelled

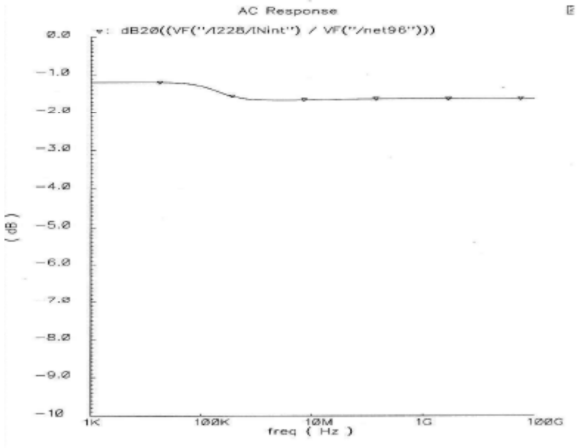


Fig. 12b:AC differential gain:attenuation:gain is only -1dB with a nearly flat response

However, these capacitors, **C1** and **C2**, cause poles at 200 kHz with **R1**, **R2** respectively. As a consequence to guarantee stability, the integrator cut off frequency (**R2C3**) has to be fixed much lower than these poles.

R3 is the feedback resistor of this current conveyor that fixes Ioutp=Ioutn=I(R3).

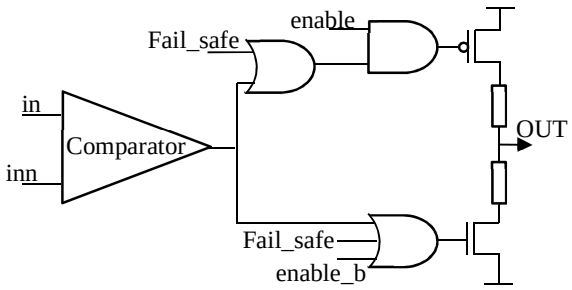


Fig. 13: Receiver principle schematic

Presented in Fig. 13, the differential to single amplifier is in fact a high speed comparator with dynamic hysteresis. The output of the main comparator is connected to one input of the differential pair responsible for the hysteresis.

To generate the TTL level the output stage of the receiver consists in a huge CMOS inverter.

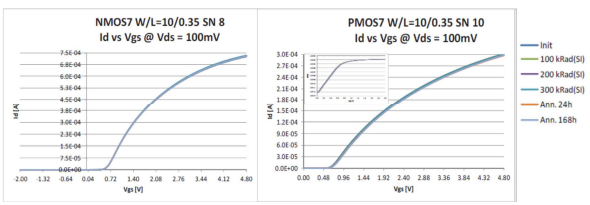
As the application imposes output impedance close to 50 ohms in order to minimize reflexions on line; serial resistors R have been added at the source of the output MOS transistors to reach this target. This constraint degrades speed performance. To compensate its impact, number of stages and area of output global stage have to be reduced. Finally, some optimized combination of NAND, NOR gates deal with signal, fail-safe and enable states. The output buffer manages the output drive of the receiver and its ability to drive a capacitance of 10pF

According to the common mode shifter block diagram, if V(IN) -V(INN) is lower than 100mV and if there is no more transition on these nodes, then we are considered in failsafe mode. This puts both output MOS transistors in high impedance mode by acting on their gate.

IV. SPACE SPECIFICITIES

The LVDS circuits are designed for space applications. A total ionizing dose (TID) test campaign on elementary components has been performed to investigate the technology radiation hardness. The components have been radiated at high dose rate using a Co60 gamma ray source. The results are presented in Fig. 14.

Fig. 14: NMOS and PMOS drift vs radiations



The TID test on PMOS confirms that threshold voltage shift is not an issue for advanced CMOS processes due to thin gate oxides. This is also confirmed on the NMOS components

with high W[3]. The CMOS G02 (gate oxide tox=8.5nm) can be considered rad-hard until a TID~100Krad (completely recovery of the Ioff leakage current). As our schematics are not sensitive to Ioff, they can support higher TID.

Moreover, the chosen technology has a substrate with very low resistivity which is very useful to decrease latchup risks in general and more specifically Single Event Latchup (SEL).

Some precautions have also been taken in order to harden the design and the layout to the radiations. The methodology was the following.

Firstly, Single Event Transient (SET) are simulated using double exponential current sources injected on each transistor. This allows us to evaluate the transistor sensitivity to the radiation Transient. Then, analyze has been done to identify the most sensitive transistors and the schematic has been improved accordingly to avoid too drastic events.

In layout, to prevent Single Event Latchup (SEL), all NMOS and PMOS have been layouted with deep nwell isolation as shown on the cross section below Fig. 15 .

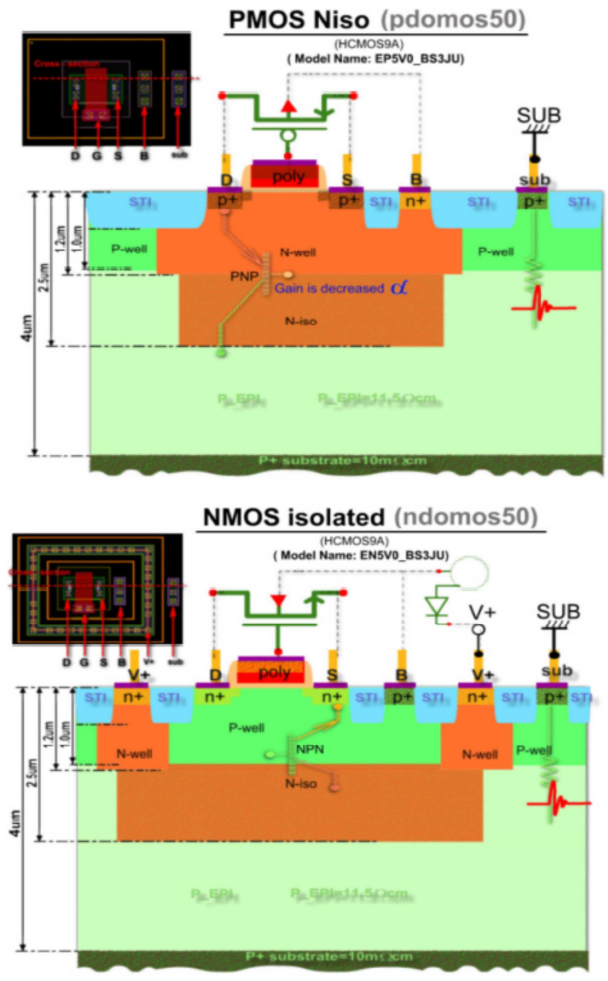


Fig. 15: Isolation layer and Guard ring for nwells , pwell

Systematic continuous tapping at NWELL & PWELL edges and also continuous substrate tapping at DNW edges have been used also.

A specific DRC for these SEL specificities was developed and used for final layout verifications.

V. ESD PROTECTIONS

One major difficulty to design these LVDS circuits has been to meet the particular challenging ESD specifications imposed at 8KV on LVDS receiver input and driver output combined with SEL immunity. The large common mode input range of -4V to +5Vwhich has to be tolerated at the receiver input makes the development even more difficult.

Two innovative ESD devices have been developed to protect input/outputs of LVDS links [8]. Both protections are isolated by deep well isolations layers for latch up immunity.

For outputs, a Silicon Rectifier (SCR) with its associate triggering system combined to a reverse diode has been used as standalone ESD protection. With this architecture output signal swing achieved was -0.7V up to 6V allowing large common mode.

Parasitic capacitance of overall output protection was 800fF for 16 KV HBM ESD target.

SEL immunity has been achieved using appropriate isolation strategy avoiding floating gate of SCR.

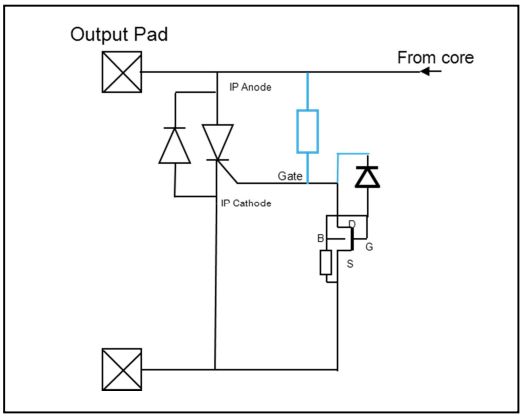


Fig. 16: Output ESD protection schematic.

Fig. 16 represent schematic of output ESD protection with, in blue, pull up resistor and well isolations linked SEL immunity.

For inputs, two back to back SCR, also called TRIAC with symmetrical triggering circuit have been used as standalone ESD protection. The use of TRIAC device allows us to achieve an input signal swing from -4 V up to 5V, compatible with large common mode voltage.

Parasitic capacitance of overall input protection was 960fF for 16 KV HBM ESD target. SEL immunity has been achieved using innovative isolation of triggering systems.

Fig. 17 shows schematic of input ESD protection with, in blue, well connection linked SEL immunity.

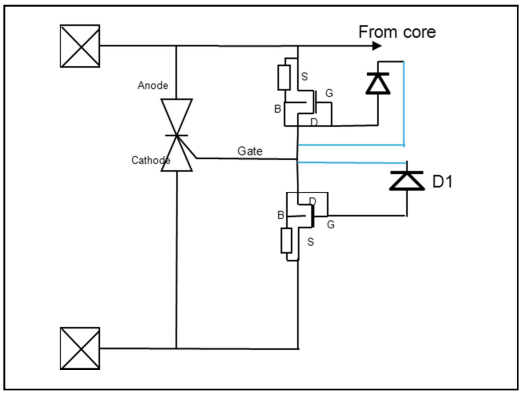


Fig. 17: Input ESD protection schematic.

ESD protection characterization has been done using Transmission Line Pulse (TLP) equipment. Equipment setup was 100ns pulse duration 10ns rise time to emulate energy of HBM ESD stress. Both protections were able to sustain ±9 Amperes TLP with a maximum overshoot of 8.5Volts. This performances show us the ability protection to sustain 16KV HBM stress. For final product qualification a conventional ESD tester has been used showing the ability of LVDS pins to resist to 8KV HBM (tester limit).

Laser tests have been useful to best understand their behavior regarding SEL immunity. The bench is composed of a microscope and a pico laser source (pulse energy from 100pJ to 6nJ). The laser beam is focused on the backside of the device. An infrared camera is used to visualize the internal structures through the silicon substrate. The consumption is monitored to detect every voltage breakdown.

VI. PACKAGE

These LVDS circuits: quad drivers and quad receivers are inserted in Flat 16 standard packages.

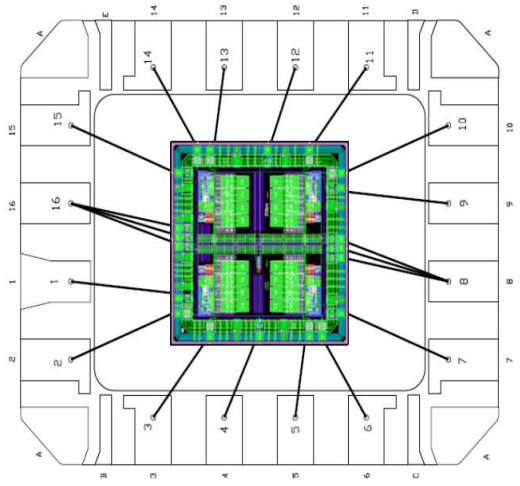


Fig. 18: LVDS31, die and package

The die size is defined to reduce bonding because the self-induced by bonding lead have an impact on dynamic performances.

Fig. 18 and Fig. 19 give the pictures of the 2.1 mm * 2.1 mm dies in the flat16 packages:

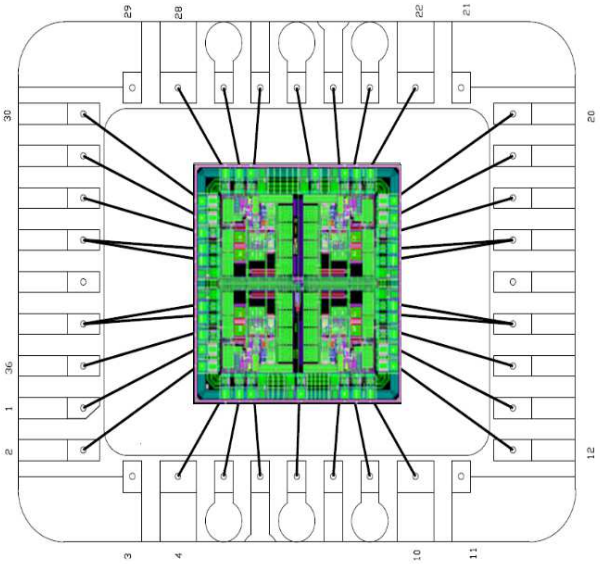


Fig. 19: LVDS32, die and package

For the receivers (LVDS32), as the output buffer signals have very short transition time (0.6ns) a huge peak current is taken from the power supply. In order to minimize inter channel cross talk, a lot of on chip decoupling capacitors have been added. Furthermore, each channel has its own couple of supply pads in order to minimize this crosstalk. A dedicated package with inter routing for power supplies has been developed in order to get a standard pinout.

VII. MEASUREMENT RESULTS

A. *Electrical*

Both the receiver RHFLVDS32 and driver RHFLVDS31 have been evaluated in laboratory. The evaluation boards are presented in Fig. 20 with measurement setup.

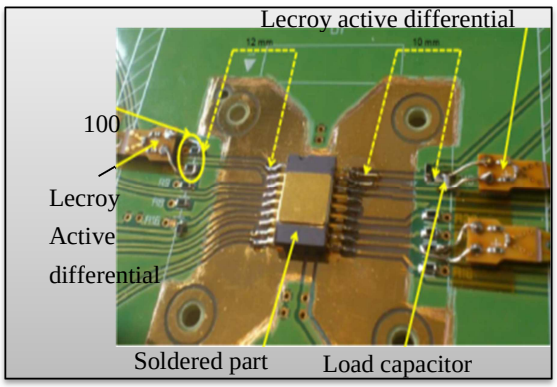


Fig. 20: Measurement evaluation board

Huge efforts and specific equipment have been necessary to measure properly propagation delays with good accuracy (better than 100ps).

Cautions have especially been taken on capacitive load, lines and reflections. Finally, propagation delays measured are around 1.85ns for the receiver as expected by the specification, as shown in Fig. 21.

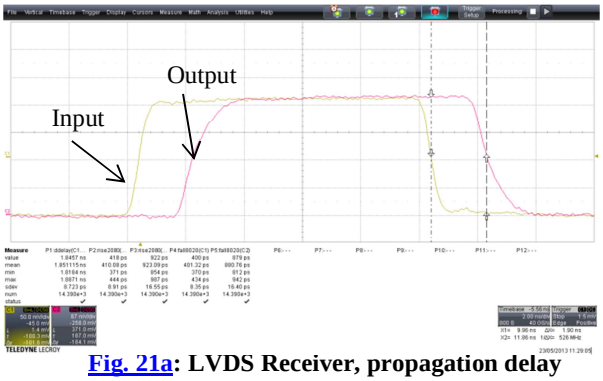


Fig. 21a: LVDS Receiver, propagation delay

The eye diagram below has been performed with a driver(31) connected to a receiver(32) through a 183cm length line. We have got a total jitter of 616ps, a random jitter of 20ps and a determinist jitter of 336ps.

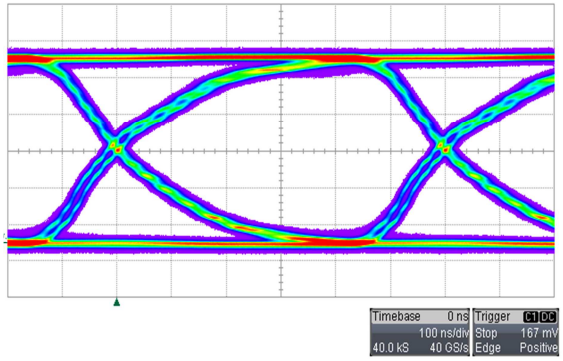


Fig21b: LVDS Receiver eye diagram

In the tables below (Fig. 22), major measurements results are compared versus specifications expected:

LVDS31		Specification			Measure
Symbol	Parameter	Min	Typ	Max	Typ
ICCL	Total enabled supply current		20 mA		16.5 mA
tPHLD	Propagation delay time, high to low			1.9ns	0.95 ns
tPLHD	Propagation delay time, low to high			1.9ns	0.95 ns
tSKP	|tPHLD-tPLHD|			0.3 ns	< 100 ps
tSK1	Channel to channel skew			0.3 ns	< 100 ps
tSK2	Chip to chip skew			0.7 ns	
tr / tf	Output signal rise / fall time		1.2 ns		0.820 ns
ESD	HBM: input LVDS		8 kV		OK
ESD	HBM: all other pins		2 kV		OK
TID	High Dose Rate(50-300 rad/sec)	300 k rad			OK
Heavy-ions	SEL immunity(at 125) up to:	110 MeV.cm2/mg			OK

Fig22a: Tables with major measurements results for Driver

LVDS32		Specification			Measure
Symbol	Parameter	Min	Typ	Max	Typ
ICCL	Total enabled supply current		15 mA		12.5 mA
tPHLD	Propagation delay time, high to low			3.1 ns	1.85 ns
tPLHD	Propagation delay time, low to high			3.1 ns	1.85 ns
tSKD	|tPHLD-tPLHD|			0.3 ns	< 100 ps
tSK1	Channel to channel skew			0.3 ns	< 100 ps
tSK2	Chip to chip skew			0.7 ns	
tr / tf	Output signal rise / fall time		1 ns		0.870 ns
ESD	HBM: input LVDS		8 kV		OK
ESD	HBM: all other pins		2 kV		OK
TID	High Dose Rate(50-300 rad/sec)	300 k rad			OK
Heavy-ions	SEL immunity(at 125) up to:	110 MeV.cm2/mg			OK

Fig22b: Tables with major measurements results for Receiver

B. Radiations

300krad in high dose rate and 150krad in low dose rate have been successfully achieved.

Heavy ions test were performed on both Driver and Receiver. The aim of the test was to evaluate the sensitivity of these devices versus SEL and SET.

No SELs were observed with the LET value of 67.7MeV.cm²/mg (Xenon heavy ions) at 125 degrees.

SETs were observed with a minimum LET of 67.7 MeV.cm²/mg. No SET was detected with a LET of 32.6 MeV.cm²/mg at 25 degrees.

VIII. CONCLUSION

The Rad-hard LVDS driver and receiver described in this paper, have been processed in a 0.13um CMOS STMicroelectronics technology with specific mitigation techniques, to achieve best in class hardness to total ionization dose and heavy ions.

The chips have been manufactured and verified from a functional perspective, as presented in this paper.

Radiation characterization and power-temperature stress test have also been done, to ensure 300 krad TID and 8 kV ESD on LVDS pins.

ACKNOWLEDGEMENTS

The authors would like to thank Francesco Toscano, Gilles Gasiot, Nicole DeBacker, Thibaut.Lardeau, Marc Rodary, Olivier Croisat, Jean-Louis Bernet, Andre Uguen, Adrien Soufflet, Gregory Gibault, Stella Gioanni for their major contributions to the success of this project.

REFERENCES

[1] Tajalli, Y. Leblebici, "A Slew Controlled LVDS Output Driver Circuit in 0.18 um CMOS Technology", *IEEE Journal of solid-state circuits, vol. 44, no. 2, February 2009.*

[2] M. Chen, J. Silva-Martinez, M. Nix, M. E. Robinson, "Low-Voltage Low-Power LVDS Drivers", *IEEE Journal of solid-state circuits, vol. 40, no. 2, February 2005.*

[3] F. Faccio and G. Cervelli, "Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors", *IEEE Transactions on nuclear science, vol.52, no. 6, December 2005*

[4] RHFLVDS31A Datasheet "Rad-Hard Quad LVDS driver" *ST, March 2013*

[5] RHFLVDS32A Datasheet "Rad-Hard Quad LVDS receivers" *ST, March 2013*

[6] LVDSR2D2 Datasheet "Rad-Hard Dual LVDS driver-receiver" *ST, March 2013*

[7] LVDS-MUX8 Datasheet "Rad-Hard Dual 4*4 Crosspoint Switch LVDS" *ST, March 2013*

[8] Jimenez, J., Galy, P., Bourgeat, J., Heitz, B. "High swing low capacitance ESD RF protections in advanced CMOS technologies ", *IC Design & Technology (ICICDT), 2012 IEEE International Conference on IC Design & Technology*