NEW ID MOS PDK for SPACE APPLICATIONS

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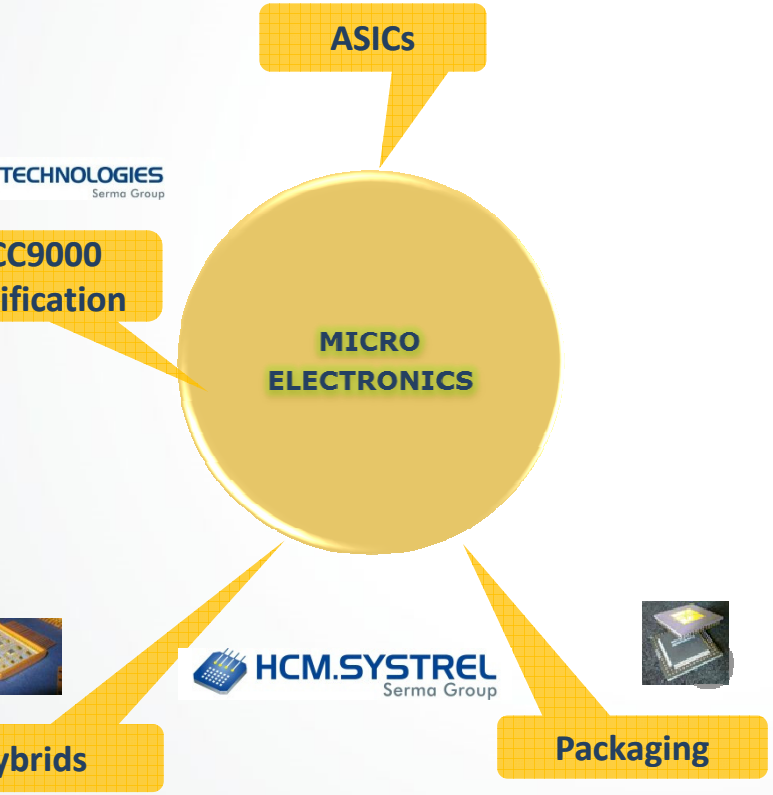
ID MOS
Serma Group

Productivity Engineering GmbH
Serma Group

ASIC Design & Production

AMICSA 2014

MICRO-ELECTRONIC CORE BUSINESS



ASICs

- Design - Production supply-chain
- 15 million units per year (small to medium size series)

Packaging

- Wafer dicing/ Inspection / Chip sort
- Ceramic Packages
- Specialised in high-constraint systems: medical implantation, oil exploration, space applications

Qualification

- Electrical/Physical/Chemical Expertise
- Microelectronics/Microsystems Expertise
- ESCC9000 Qualification
- Certification : ISO9001- EN9100 (on-going)

ID MOS & PE at a glance

- Fabless Semiconductor companies
- Turnover 15 MEuro in 2013
- 38 employees in France (ID MOS) & Germany (Productivity Engineering)
- 15 Million units delivered in 2013 (80 customers)
- 29 engineers design resource : 19 in-house & 10 in our remote design center in Bulgaria
- ~180 ASIC design history, about 12 new ASIC designs per year
- Core business:
  - Mixed-signal & Digital microelectronics
  - Technologies for harsh environments (low, high temperature & space)
  - Obsolete circuits redesign (ASIC or standard products)
  - Smart Power, RFID Smart Tag, Capacitive sensing (including off-the-shelf products)
- Dedicated methodologies for specific domains : DO254, ESCC...
- ISO9001 certified
- Full supply-chain monitoring (wafer sourcing, probing, packaging, test & packing)
- Sales offices in France, Germany & Italy

ID MOS ASIC / ASSP Application domains

INDUSTRIE

72%

15Million pieces

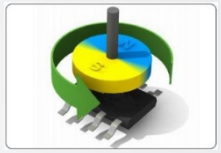
TRANSPORT

23%

HARSH ENV

5%

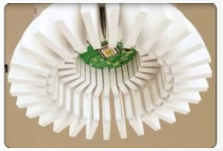
SENSORS

METERING

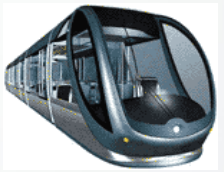


HOUSEHOLD & CONSUMER

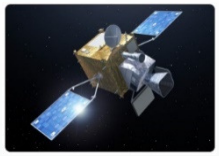




AVIONICS AUTOMOTIVE RAILWAY

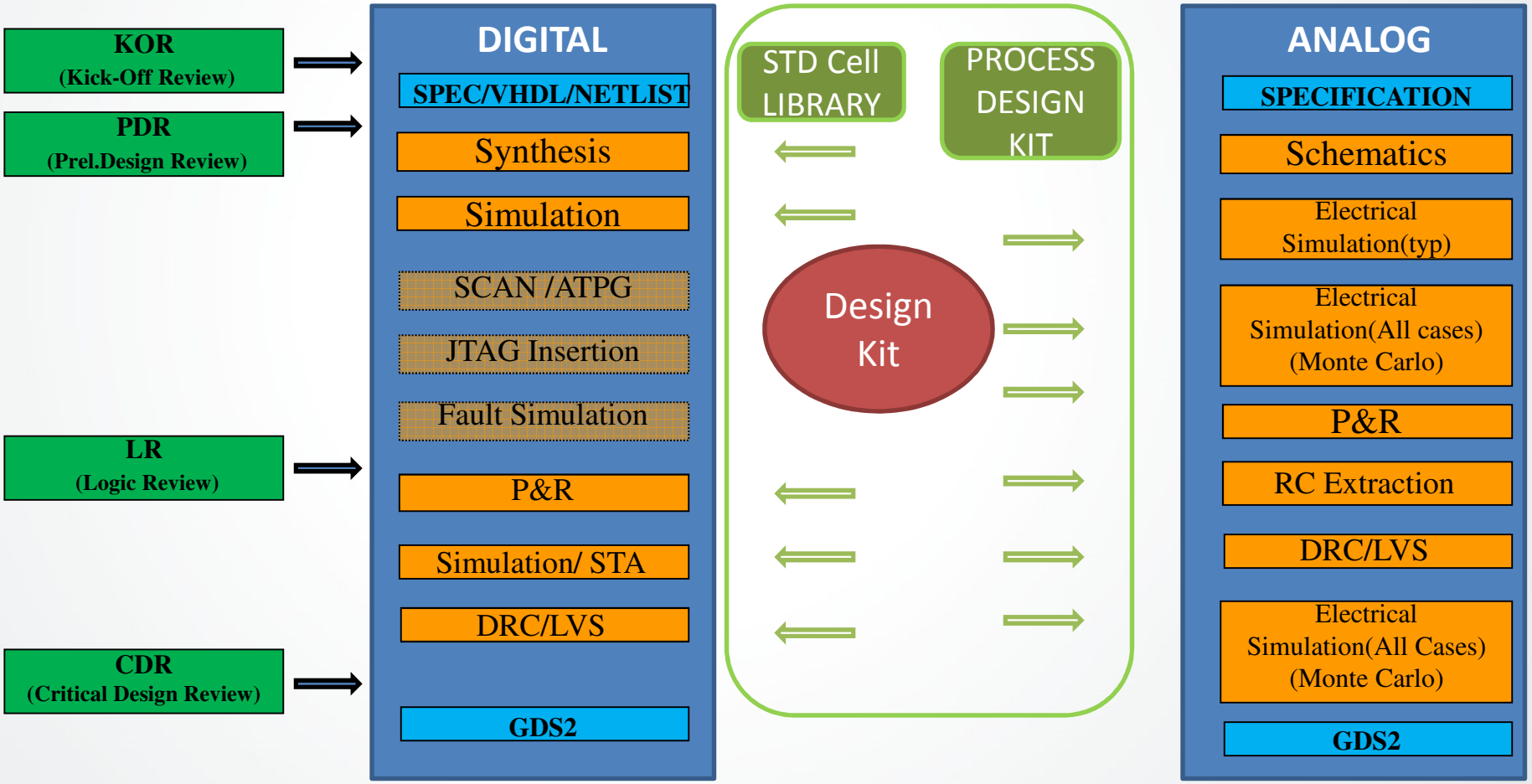





OIL SEARCH SPACE




Mixed A/D ASIC DESIGN FLOW



XH035 DK Development

TEST CHIP CHARACTERIZATION

- **SPECIFICATION**
- Development
- Fabrication
- Packaging
- Electrical Test
- Radiation Test (TID-SEL)
- Modelisation (-55°C / 125°C)
- **DESIGN KIT**

Technologie : XH035
Low Voltage : 3,3v
High Voltage : 90v

ESCC22900 TID

- **SERIALIZATION**
- Electrical Test (Low/High Temp.)
- Electrical Test (RT) Irradiation Electrical Test (RT)
- Annealing Test 24h (RT) Annealing Test 168h (100°C) Electrical Test (RT)
- **LOT Acceptation**

Irradiation Source : ^{60}Co
Dose rate : 0,31Krad(Si)/h
Temperature : 25°C
Supply : 3,3V
Biased Mode : 4 ON – 2 OFF
Steps : 0, 15,30,50, 100Krad (target)

ESCC25100 SEL

- **SERIALIZATION**
- Electrical Test (Low/High Temp.)
- Electrical Test (RT) Heavy IonExposure Device under test
- SEL Immunity (LET **67,7Mev.cm^2.mg$^{-1)}$**) Electrical Test (RT)
- **LOT Acceptation**

2 Samples
Temperature : 125°C
Supply : 3,6V

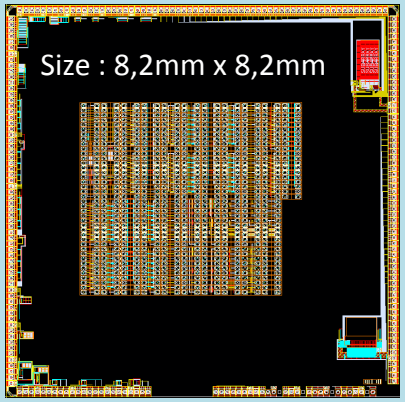
SEL Immunity (target) :
LET of 67,7Mev.cm^2/mg

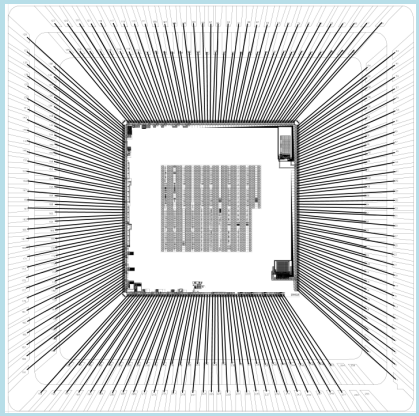
→ **ASIC DESIGN**

XH035 TEST CHIPs

TC_1 (LV)

- XH035
- 3,3v
- PGA256





XH035 Low Voltage TC-1

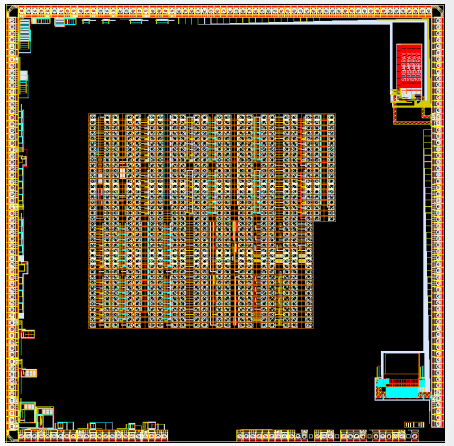
1. EEPROM256x16 (Std)
2. SRAM 512x16 (Std)
3. TOP DIGITAL :
- ✓ INV – NAND – Logic0 – Logic1 (Hardened(H))
- ✓OSC – ASYNC COUNTER (Std + H)

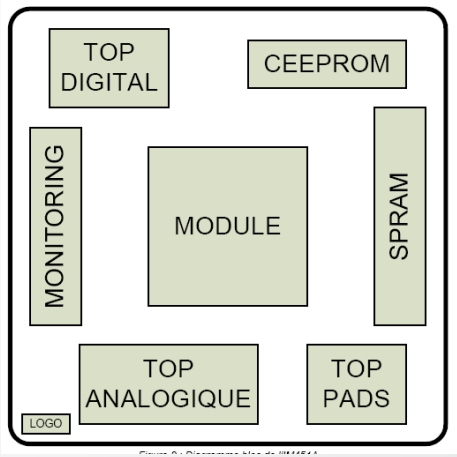
4. MODULE :
- All necessary basic elements for a SPACE APPLICATION

5. TOP ANALOG :
- AOP with differential pair NMOS or PMOS (H)
- BANDGAP (Std + H) (same output voltage/ Same Tr Sizes)
- COMPARATORS with differential pair NMOS or PMOS (H)
- CURRENT SOURCE (H)
- POWER ON RESET (H)
- CHARGE PUMP (EEPROM - H)

6. MONITORING:
- Basic elements for TID & SEL Radiation tests (H)
- NMOS (7) :Abutted(3), Not Abutted(3), ESD(1)
- PMOS (7) :Abutted(3), Not Abutted(3), ESD(1)

7. TOP PADS :
- DIGITAL / ANALOG / POWER (H)





XH035 TC-1 Radiation Results

- **NO ATYPICAL BEHAVIOUR DURING THE TID TEST**

- **ALL CELLS HARDENED by LAYOUT reach the targeted TID level => 101KRads**

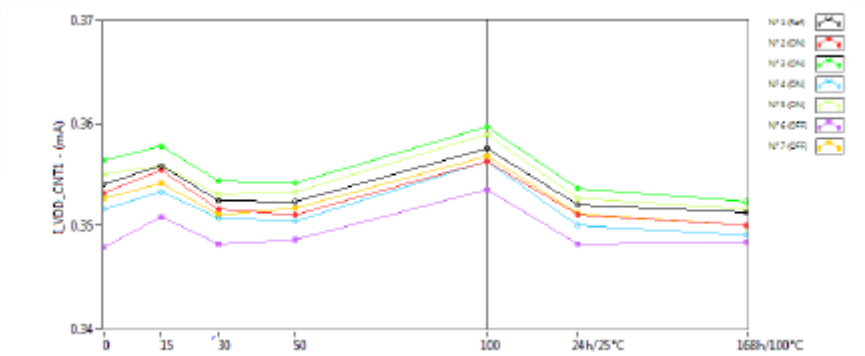
- **ALL CELLS HARDENED by LAYOUT reach the targeted SEL level : latch-up immunity tested up to a LET of 67,7Mev.cm²/mg (80,72Mev.cm²/mg 33°C tilt)**

- **The blocs designed with the standard library are very limited in term of TID and SEL.**

- **CEEPROM Failure observed for the part number 2, at 50 krad(Si) dose level**
  - **READ/Write Sequencer : Std**
  - **Charge pump : Hardened**

XH035 TC-1 RESULTS

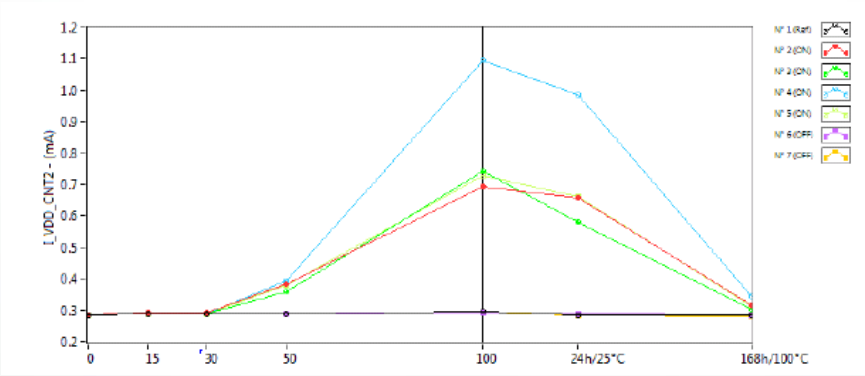
CNT1 : Asynchronous counter HARDENED by DESIGN



Imax ~0,36mA

CONDITIONS:
T=25°C
VDD= 3,3V
Fin = 10MHz

CNT2 : Asynchronous counter => Standard Library

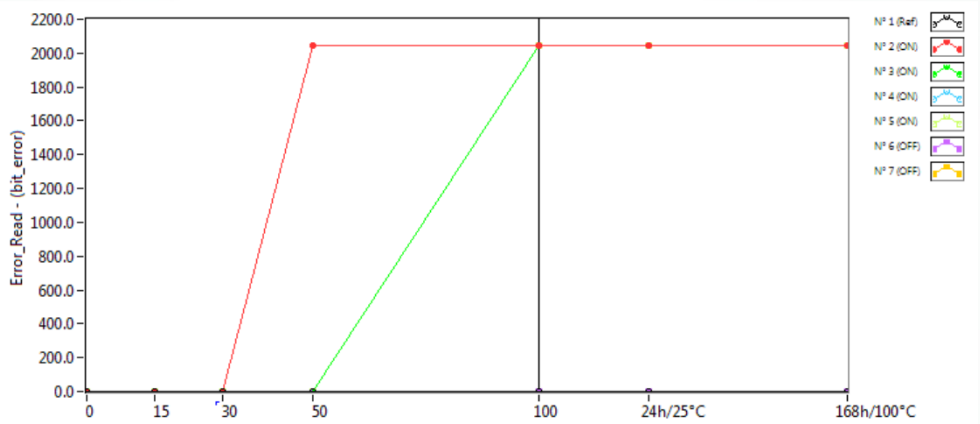


Imax ~1,1mA

XH035 TC-1 RESULTS

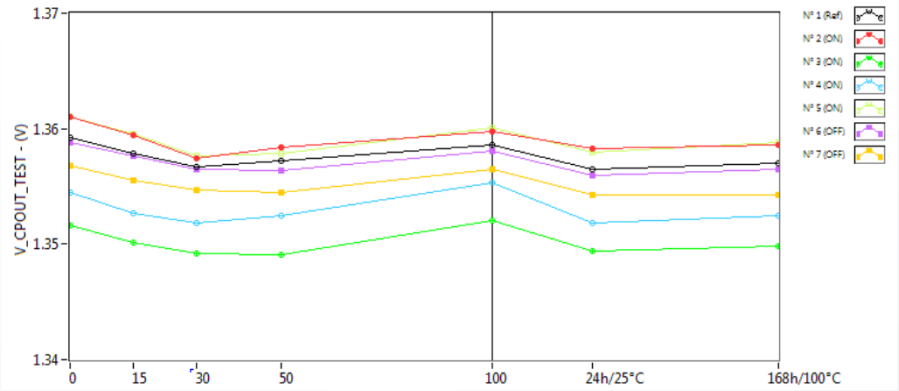
CEEPROM : Write-Read Error

CONDITIONS:
T=25°C
VDD= 3,3V
VBGN= +1.28V,
pattern = $AA55

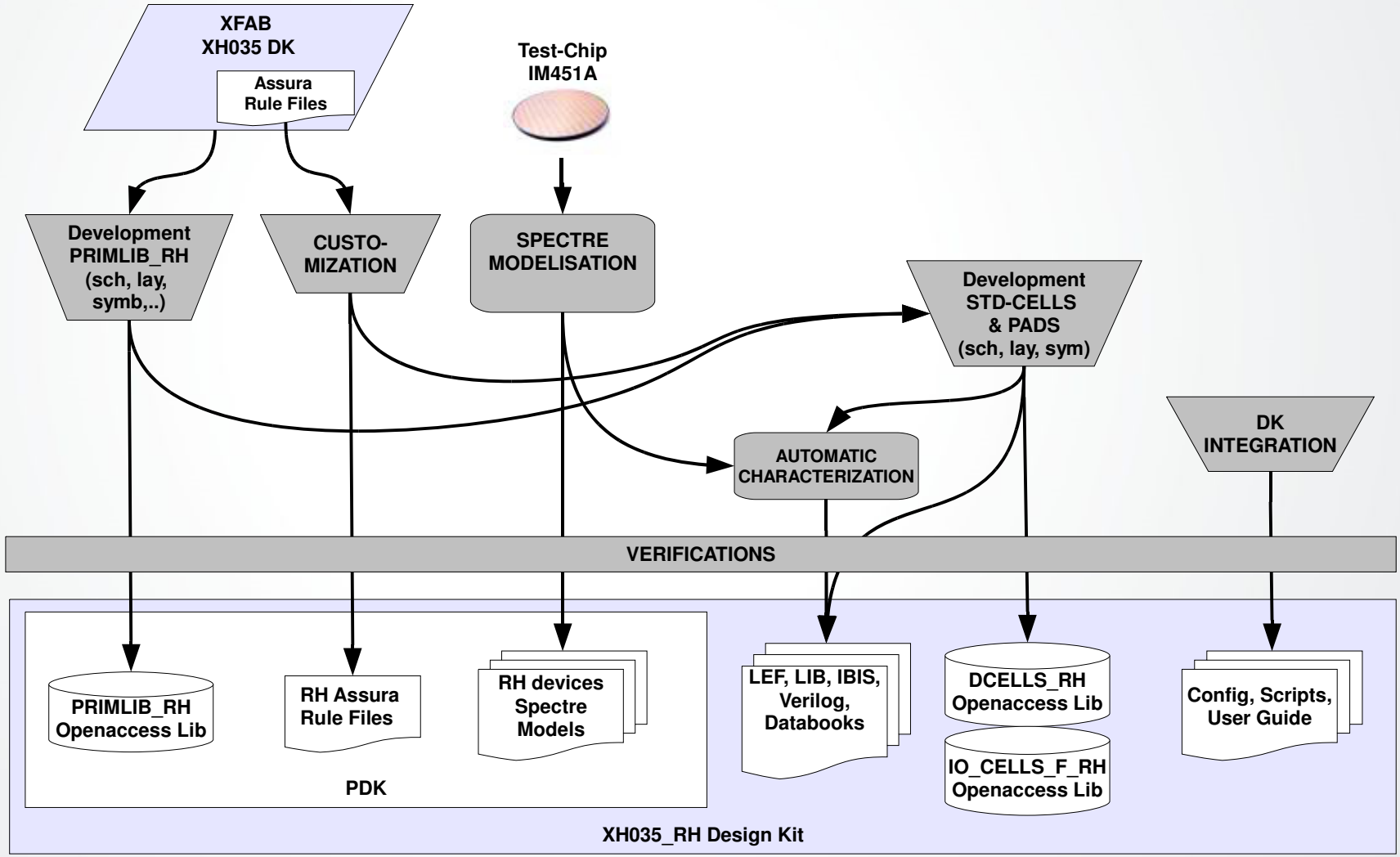


Charge Pump :

CONDITIONS:
T=25°C
CP_supp= +3.3V,
CP_VBGN= +1.28V,
CP_CPEN= +3.3V,
power on 100µs



XH035 Design Kit for SPACE Application



LIBRAIRIE PRIMLIB_RH

The PRIMLIB_RH Library provides pre-characterized Rad-hard annular transistors

nmos4_rh	4-pin regular annular NMOS
nmos3_rh	3-pin abutted annular NMOS, with Source and Bulk shorted
pmos4_rh	4-pin regular annular PMOS
pmos3_rh	3-pin abutted annular NMOS with Source and Bulk shorted
nha_rh	12V NMOS with thin oxide, fixed size
ioh_ne_rh	Special NMOS transistor for ESD protections, with two distinct sizes
ioh_pe_rh	Special PMOS transistor for ESD protections, fixed size

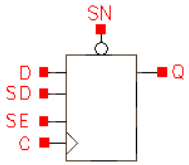
All regular low-voltage regular mosfets are defined as “scalar” components : Predefined layout templates are provided in the DK, but user can specify custom W & L parameters even if the corresponding layout is not predefined in the DK.

XH035 Design Kit for SPACE Application

Library name : DCELLS_RH

Deliveries :

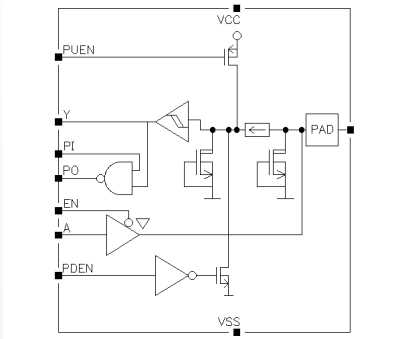
- Schematics + Layouts + Abstracts + symbols
- Libraries : Liberty, Verilog, LEF
- Tutorial(s)
- Detailed description of SEU-hardening procedure(s).
- Library databook
- **Sequential Cells : 7**
- **Combinatoric Cells : 30**
- **Density : ~4Kgates/mm²**
  : ~300 FF/mm²
- **Voltage Range : 1,8v to 3,6v**
- **Temperature Range : -55°C to 125°C**



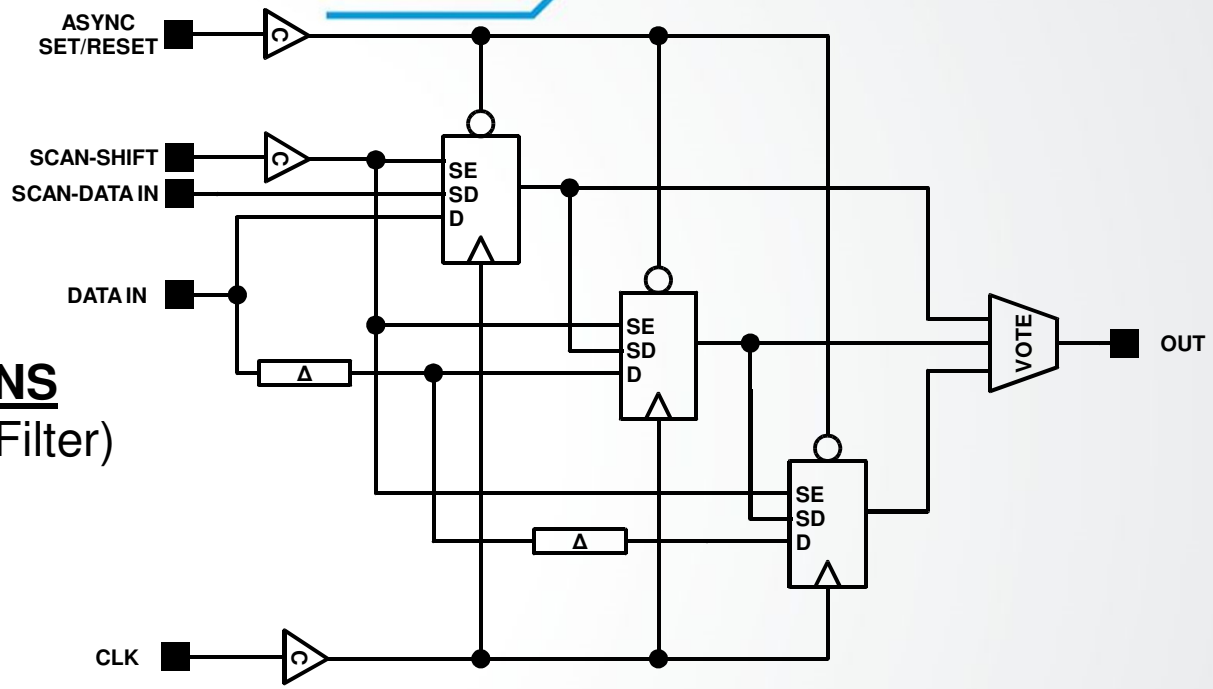
Library name : IO_CELLS_F_RH

Deliveries :

- Schematics + Layouts + Abstracts + symbols
- Libraries : Liberty, Verilog, LEF
- IBIS Models of Digital Pads
- Library databook
- Min Pad size : 80µm x 80µm
- **Digital Pads : 4 (3mA – 6mA)**
- **Analog Pads : 4**
- **Supply&Gnd Pads : 4**



XH035 Design Kit for SPACE Application



SET & SEU PROTECTIONS

- Anti SET Buffer (delay-Filter)

•Special delay cells (Δ cells) are inserted in front of 2 of the 3 flip-flops to protect the data inputs against SET spikes appearing synchronously with the active clock edge.
•Special anti-SET “C” buffers are implemented as leaf-buffers on the SCAN-SHIFT tree, on the asynchronous set/reset trees and on all clock-trees to protect these signals against SET-spikes.
•This flow is based on the use of ready-to-use RTL-compiler scripts, already included in the XH035_RH design-kit, and pre-built Rad-hard TMR-macrocells indented to be used as replacement cells in place of regular flip-flops.

CONCLUSIONS

BY HARDENING THE STANDARD XH035 LIBRARY, ID MOS REACHED THE TARGETED RADIATION LEVELS to START ASIC DEVELOPMENT FOR SPACE APPLICATIONS.

THE DESIGN KIT FOR LOW VOLTAGE APPLICATIONS IS READY.

- **One mixed Digital/Analog circuit in Development**
- **One Digital circuit in Fabrication**