Radiation-Tolerant Low-Voltage ASIC Library Evaluation for Space Applications

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Abstract

The needs for increasingly low cost, low space occupancy and reduced weight in the space industry have made mixed-signal ASIC integration mandatory. In a first contract, the CNES and ID MOS selected the mixed-signal XH035 LV ASIC process to design a set of rad-tolerant Low Voltage ELT transistors, checked their robustness up to 100Krads and their immunity to the SEL.
The aim of the project was to develop radiation tolerant libraries that enable designers to develop Analogue and Digital circuits for the Space Applications.

I. INTRODUCTION

ID MOS selected the XFAB XH035 mixed-signal technology for its modularity and the set of devices provided in the standard XFAB process to develop Analogue and Digital functions. This standard technology targets automotive, telecommunication and industrial applications; it has been widely used and tested for various applications, it is a mature technology. To develop circuits, a design kit is provided for each technology by XFAB. This tool box is based on the characterisation of basic devices (transistors, diodes, resistance, capacitor...), it includes the electrical, the synthesis, the simulation models and the layout of those elements, the standard cells, the I/O pads and all scripts to perform the verifications. The XFAB target is to access the markets with high volumes where the price unit is a key factor linked with the die size. To reach the objective, they have to optimize the layout of the basic elements to integrate the maximum of functions on a minimum of Silicon area. Unfortunately, it is incompatible with Space applications. The drawing of the basic transistors has to be completely redefined to reach the TID and SEU targets. A set of transistors covering most of the analogue low voltage applications have been selected and harden by ID MOS. A test chip including different modules, to perform the characterisation, to check the insensitivity to SEL and to reach the defined TID level has been launched for fabrication. This first step has been 100% successful allowing us to prepare the next phase.

The tasks performed in this contract are the following:

- Characterisation of the basic devices: P/N Transistors, Resistance, Capacitor.
- Development of the Spectre models for the electrical simulations.
- Development of the Process Design Kit (PDK)
- Development of the Standard cell library
- Development of the I/O pads library
- Update of the Verification tools
- Supply a set of scripts to add automatically digital functions to minimize SEU and SET effects: Triplication, pulse filter.
- Integration of those elements to provide a Design Kit
- Validation phase

II. THE TEST VEHICLE

To fulfil Space application projects, a LV radiation-tolerant test chip has been designed. Its target is to be characterized up to 100 krads. insensitive to SEL up to 67, 7 Mev/cm²/g.
From the XFAB library the following N and P transistors have been selected:

- NMOS (nmos4, nmos3, nha, ioh_ne)
- PMOS (pmos4, pmos3, ioh_pe)

Those transistors have been hardened using an enclosed layout (ELT) and guard rings. Structures have also been used to break leakage paths. Those cells have been tested electrically before and after TID.
As example, we can compare the I/V curve of the nmos transistor extracted from the standard XFAB libray and the equivalent ELT transistor before and after TID. We choose the smallest enclosed transistor size used for digital cells (W/L=5.4/0.35µm)

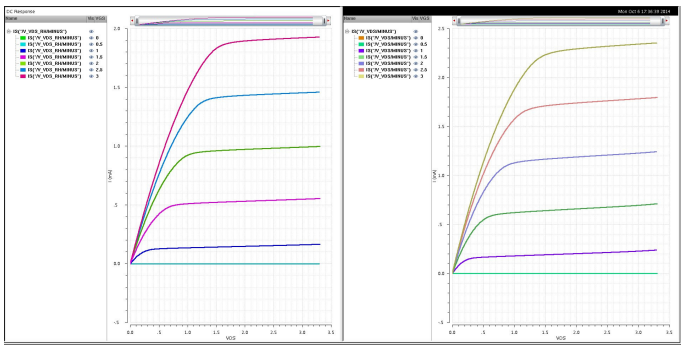

Figure 1: I/V curve (With and without ELT)

I (mA) VDS = 3,3v	nmos3 (rh)	nmos3 (rh_100Krad)	nmos (std)
VGS= 1.0v	0.16 mA	0.17 mA	0.21 mA
VGS= 1.5v	0.55 mA	0.56 mA	0.70 mA
VGS= 2.0v	0.99 mA	1.00 mA	1.22 mA
VGS= 2.5v	1.46 mA	1.47 mA	1.80 mA
VGS= 3.0v	1.92 mA	1.93 mA	2.35 mA

Table 1: I/V curve

For a same size the curve are slightly different between standard and enclosed transistor nmos before radiation, but no significant deviation before and after radiation (100Krads) for the enclosed transistor.

A. *Description :*

The test chip includes seven blocks:

- Digital : Basic digital cells & functions
- Monitoring : Basic devices with ESD protection
- Analogique : Basic analogue cells & functions
- Pads : Input/Output/Bidirectional
- Memories : Std XFAB SRAM/CEEPROM
- Module : Basic devices

The peripheral blocks are used for Electrical and Radiation tests. The bloc Module is used for characterization.

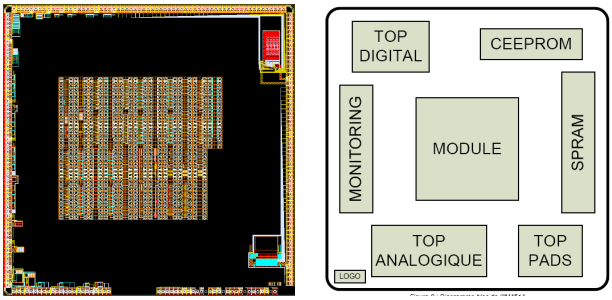

Figure 2 : Low Voltage Test Chip

B. *Description & results of the radiation tests:*

The total dose tests have been carried out with a Cobalt 60 source on 6 reference pieces up to 100 krads at a low dose rate of 310 rad/h. An annealing of 24h/25°C plus 168 h/100°C has been performed.

The SEL tests have been performed at the university of LOUVAIN (Belgium) using Xenon ions with energy of 1217 MeV and a LET on die surface of 67.7 MeV.cm²/mg at a temperature of 125°C.

TID tests have shown no functional or parametric problems up to 100 krads on hardened structures. The non-RT Cells are limited: The non-hardened oscillator and counter present an important increase of their supply current at 30Krads.

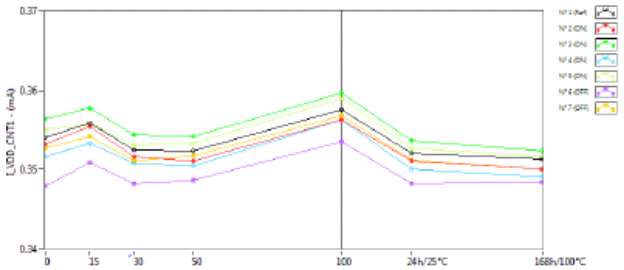

Figure 3: Asynchronous counter based on RT Cells

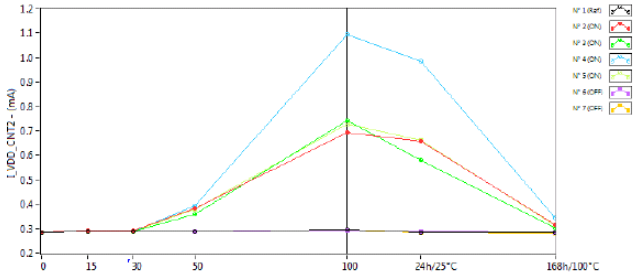

Figure 4: Asynchronous counter based on Std Cells

No SEL has been detected on the Rad-Tolerant cells.
SELs were observed on the non-hardened counter, the non-hardened oscillator and the non-hardened E2PROM. It justifies the necessity to implement protections against SEL.

III. Description of the Design Kit

The ID MOS Radhard Design Kit is an extension of the official XH035 DK provided by XFAB. The advantages are multiple: maintenance, enhancement, no training, no time lost in using it.
It provides a database of models, primitive devices, digital cells, I/O cells, configuration scripts and tools needed to design Rad-Hard-by-Design mixed-signal Analogue/Digital Integrated circuits, according to ID MOS custom rules.

A. *Project Design Flow*

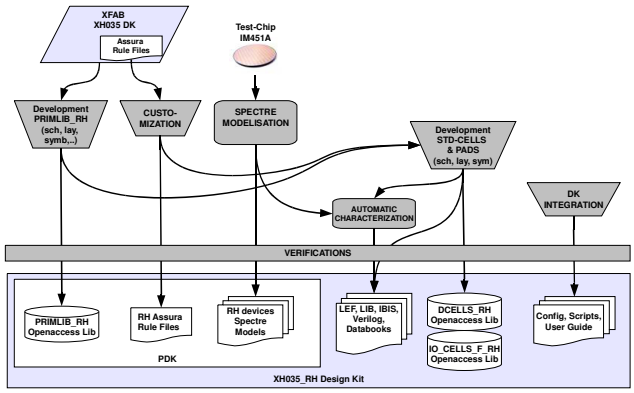

Figure 4: Project Design Flow

B. *Process Design Kit (PDK)*

The PDK is the core of the RH Design Kit. It includes all the low-levels Cadence libraries, configuration files and scripts to develop and simulates Rad-hard functions.

It provides the following primitive devices:

- ⇨ 4-pin regular annular NMOS
- ⇨ 3-pin abutted annular NMOS (Source/Bulk shorted)
- ⇨ 4-pin regular annular PMOS
- ⇨ 3-pin abutted annular PMOS (Source/Bulk shorted)
- ⇨ 12V NMOS with thin oxide
- ⇨ Special NMOS transistor for ESD protections
- ⇨ Special NMOS transistor for ESD protections

It consists of three main parts.

1) SPECTRE Models :

The spectre models of annular transistors are “Scalar” allowing to simulate devices of various shape. They are compliant with the devices identified by the extraction tool (ASSURA) and with the primitive cells embedded in the PRIMLIB_RH Cadence Library (consistent names and parameters).

2) ASSURA Tool Kit :

It is a Customization of XFAB Assura rule files to add support of annular transistors, both for LVS and DRC.

3) Library PRIMLIB:

The PRIMLIB is composed of a set of low voltage transistors hardened against radiation.

This library is backward compatible with the original one. They can be used simultaneously. The models are scalable and allow different shape

Gate Length (µm)	Gate Width (µm)
0.35	5.4, 6.5, 7.6, 8.7 (1.10 µm step)
	10.8, 21.6, 43.2 (10.8 × 2N µm)
0.70	6.8, 8.2, 9.6, 11.0 (1.4 µm step)
	13.6 , 27.2, 54.4 (13.6 × 2N µm)
1.4	9.6, 19.2, 38.4 (9.6 × 2N µm)
2.8	15.2, 30.4, 60.8 (15.2 × 2N µm)
5.6	26.4, 52.8 (26.4 × 2N µm)

Table 1: W/L Combinations for PRIMLIB_RH nmos and pmos Transistors

C. STD-CELLS & I/O Libraries

It includes a library of digital standard cells (~40) and 3V digital/analogue standards pads (~15) suitable for logic synthesis and automatic P&R:

- ⇨ Schematics + Layouts + Abstracts + symbols
- ⇨ Liberty library
- ⇨ Verilog Library
- ⇨ LEF Library
- ⇨ Tutorial(s)
- ⇨ Detailed description of SEU-hardening procedure(s).
- ⇨ IBIS Models of Digital Pads
- ⇨ Library databook

1) Electrical Characterization conditions :

- Voltage : 1,8V up to 3,6v
- Temperature : -55°C ; 25°C ; 125°C
- Process : Slow/Fast
- With/without radiation

D. Design Kit Integration :

The integration of the design kit consists in assembling all the libraries and configuration files into a portable database, and to allow easy access to this database from user's working environment, together with the XFAB mainstream DK.

IV. DESIGN KIT VALIDATION

A set of verifications has been done to ensure:

- ⇨ The main features of the PDK;
- ⇨ The efficiency of the ASSURA toolkit
- ⇨ The reliability of analogue simulations
- ⇨ The expected behavior of standard-cells and pads;
- ⇨ The capacity to synthesize a complex digital VHDL model targeting the Rad-hard standard-cells library.
- ⇨ The capacity to automatically Place & Route the standard-cells.
- ⇨ The capacity to produce a DRC-free and LVS-free complex digital design.
- ⇨ The capacity to run accurate post-extracted simulations of analogue and digital circuits.

A. PDK Verification :

1) Spectre.

The Analogue macrocells, embedded on the test-chip (POR, Band-gap, Ring-Oscillator, AOP, and Current Source) have been simulated (from schematics or from extracted layout views) and the results compared to the measurement results.

2) PRIMLIB

All standard-cells and Standard-pads have been simulated, using the PDK.

3) ASSURA ToolKit

All the standard-cells and pads have been checked using the Assura toolkit. (DRC/LVS)

B. DK Verification :

1) D-CELLS & I/O-CELLS

All the deliveries listed have been realized and checked
The whole design has been validated on a representative circuit of about 1 KGates (including pads), with scan-test insertion. (Synthesis, simulations, P&R, final DRC/LVS verification)

2) DK INTEGRATION

The installation instructions and Usage guidelines of the final Design Kit are detailed in the “Reference Manual”

V. CONCLUSION

The XH035-RH Design Kit is ready to be used by ID MOS for Space Applications. The two first circuits will help to intensively use it. A full digital circuits (40Kgates) has been fabricated and electrically tested successfully, the density reaches 4Kates/mm²
The next step is to extend the Design Kit for High Voltage Applications. It is the object of a new project by using the same methodology.

References

Single event effects test method and guidelines ESA/SCC basic specification N°25100 Iss 1, oct 95
Space Product Assurance-ASIC and FPGA development (ECSS-Q-ST-60-02C)
ESA-ESTEC- Space engineering, product assurance
Techniques for Radiation Effects Mitigation in ASICs and FPGAs (ESA-HB-XX-XX rev. 6)