Scalable Sensor Data Processor: A New Mixed Signal Processor ASIC for Harsh Environments

R. Trautner[a], B. Glass[a], R. Jansen[a]

[a]ESA/ESTEC, 2200 AG Noordwijk, The Netherlands

Roland.Trautner@esa.int

Abstract

Digital Signal Processors (DSPs) are key components for many data processing applications due to their high speed and low power consumption. This is also true for systems working in harsh environments such as those found in space and in some terrestrial application areas. Due to the specific requirements posed by these environments commercial components can be used only with severe restrictions, or not at all. For these cases specific components based on inherently reliable designs and processes must be used.

The Scalable Sensor Data Processor (SSDP) is a DSP component that meets the requirements of space applications and many specific terrestrial use cases. It is based on a well-tested prototype design and silicon-proven key architectural elements. Key specs include 1 GOps of processing power, up to 1 Mrad of Total Ionizing Dose (TID) tolerance, radiation hardened design, integrated mixed signal elements including ADCs, and low power consumption.

The development of this ASIC is ongoing and rad-hard prototypes are expected for end 2015, with flight models following 1 year later. The ASIC will be commercialized as a standard component.

I. Digital Signal Processing for Space Applications and other Harsh Environments

High Performance Digital Signal Processors are generally by far superior to General Purpose Processors in terms of power efficiency, performance for digital signal processing, and in real-time applications. In space applications, this makes them often the preferred type of processor for payload data processing units and similar subsystems. The only existing European space qualified DSP (TSC21020) is now completely outdated and at the end of its product lifecycle. Therefore, system and payload developers urgently need a reliable high performance replacement. In recent years, the European Space Agency has followed several technology routes for the development of new chips that can satisfy the user requirements.

The main properties that differentiate space qualified integrated circuits from typical commercial parts is the high reliability, radiation hardened design, and large operating temperature range. Therefore, ASICs developed for space applications are typically also compatible with the requirements of some terrestrial applications in harsh environments, such as those in R&D areas like particle physics or fusion research, and in nuclear industry (research facilities or nuclear power stations), or in specific application niches (high altitude platforms, borehole technology, etc.).

Due to the high cost of development and qualification or validation of space ASICs and the small production volumes the unit cost of space qualified ICs is typically orders of magnitude higher than that of similar commercial parts. However, the high reliability of these devices may still justify their use in some terrestrial applications where high reliability and / or high availability (minimized downtime) are key to success which may be the case in several of the aforementioned use cases.

The development of the SSDP ASIC therefore also considers terrestrial application cases where possible, and the authors appreciate feedback from potentially interested users.

II. Key SSDP Requirements

The main goal of the SSDP development is to satisfy the processing needs of typical space applications in particular in the areas of space exploration and earth observation. In addition to processing performance requirements, low mass and low power along with user friendliness as well as compliance to interface standards are considered essential [1]. The key SSDP requirements can be summarized as follows:

- Processing power > 1000 MOps
- Total Ionizing Dose (TID) tolerance >100krad (Si), with a goal of >300 krad (Si) … 1 Mrad (Si)
- Radiation hardened design (memories, registers, clock trees via EDACs / triplication etc.)
- Industry standard interfaces (SpaceWire, CAN, SPI, GPIO) and space standard peripherals (rad-hard frontend ASICs and detectors, SRAM, NVM, SRAM)
- High Quality Software Development Environment (SDE) and tools, DSP libraries
- High reliability, low power consumption, low mass
- Integration of analogue / mixed signal features, including ADCs and circuitry for housekeeping data acquisition from typical sensors
- No access restrictions for European users (ITAR free)

Based on these requirements, and on additional inputs from prototype testing / evaluation and future users, the final specification of the SSDP ASIC will be established.

III. SSDP HERITAGE

The development of the SSDP ASIC is based on several technology development activities that have been performed under ESA management in the recent past.

A. MPPB

The first one of those developments, the Massively Parallel Processor Breadboard (MPPB), demonstrated European fixed point DSP IP cores in combination with scalable Network-On-Chip (NoC) technology on FPGA based hardware [2]. It supports space typical features such as LEON2 general purpose processor (GPP) including the typical AMBA bus system and peripherals, SpaceWire (SpW) interfaces, ADC/DAC bridges, on-chip memories and other features. This system demonstrated the basic functionality of the individual elements and the scalability and significant bandwidth offered by the NoC. Data streams across the chip between DSP cores, on-chip memories, external memories, interfaces and external ADC/DAC were coordinated by the GPP by means of IRQs and DMAs, and the DSP core performance was demonstrated by means of relevant benchmarks [3].

Figure 1: FPGA based MPPB hardware (credits: RECORE)

On the software side, an SDE was developed and adapted that allows programming of the platform in C and assembly language. In addition to an API that supports efficient use of the architectural elements, an IEEE754 compatible floating point library was developed. The MPPB hardware was evaluated independently by external parties, and several improvements were implemented based on their feedback.

B. DARE+ Application ASIC

Following the successful design and development of the MPPB, a DSP prototype chip was developed in order to prove the key elements of MPPB in DARE180 [4] based silicon. This work, which was part of a larger activity (called DARE+, [5]) aimed at development and debugging of library elements for IMEC's DARE180 technology, was intended to pave the way towards future space DSPs based on the demonstrated technologies. The so-called DARE+ Application ASIC, which was implemented as a Multi-Project Wafer (MPW) based chip, included the following elements:

- Xentium® VLIW fixed point DSP with local instruction and data memories
- NoC routers
- Bridges to space qualified external ADC and DAC (STM RHF1401, ADI AD768)
- On-chip memory tile (also serving as DSP instruction memory)
- UART/GPIO programming interface
- SpW interface with RMAP target functionality

The basic architecture of the chip is illustrated in the following figure.

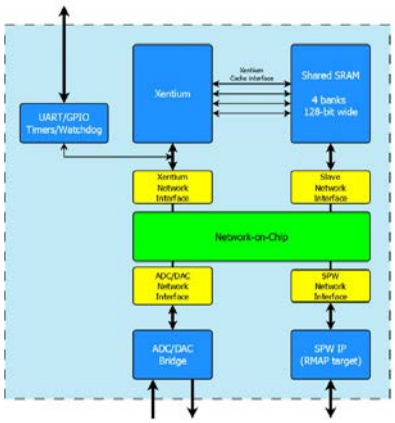

Figure 2: DARE+ Application ASIC architecture

The prototype chip has been fabricated successfully in DARE180, re-using a package that was developed for a previous activity. The chip was found to be functionally correct, with DSP core, interfaces, memories including EDAC protection, and other architectural elements working correctly also under exposure to radiation. The foreseen maximum clock speed of 100 MHz was however not reached due to excessive IRdrop (voltage drop across the on-chip power supply network) when performing DSP kernels with high memory access rates. This resulted at a reduced maximum clock speed of 50 MHz at slightly increased supply voltage. This problem, which is related to the limited chip/pad area available on the MPW-based prototype, will be analysed in detail and corrected as part of the SSDP prototype development. Figure 3 shows an image of the DARE+ Application ASIC die. The die used pads on only 3 of 4 sides due to MPW die size constraints.

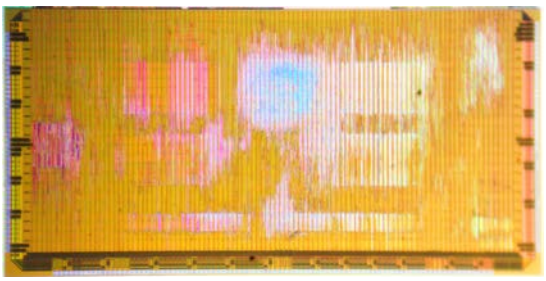

Figure 3: DARE+ Application ASIC die

A. *MPPB Evaluation by future SSDP Users*

Following the development of MPPB, independent external users with strong background in space data processing including Astrium (UK) [5] and RUAG (Austria) [6] have evaluated the platform with positive results, and have provided suggestions and requirements for future related chip designs and associated processor boards. These are taken into account for the final design of the SSDP ASIC.

IV. SSDP Baseline Architecture

The Scalable Sensor Data Processor (SSDP) is foreseen to replace the previous DSP (TSC21020), exceeding its performance significantly in particular for fixed point DSP applications, and become a key control, interface and DAQ ASIC especially for instrument designs. The baseline design features an architecture very similar to MPPB, providing a LEON General Purpose Processor (GPP), 2 VLIW Xentium® DSP cores, high-bandwidth NoC, and space typical interfaces (SpaceWire, ADC/DAC, CAN, SPI and others) for the digital part. Like the DARE+ prototype, the ASIC will be based on DARE180 technology which allows incorporation of analogue/mixed signal elements. It is expected that several mixed signal blocks will be integrated, such as a fast (up to 100 MSps) ADC for instrument data acquisition (15/16 bit), a second slow (ca 100 kSps) ADC with multiplexers for housekeeping data acquisition (12 bit), and others. Glue-less interfacing to external ADC/DAC, analogue frontend ASICs, next generation imagers and standard sensors will also be supported. The ASIC will run at a target clock speed of up to 100 MHz, providing in excess of 1 Giga-Ops for 16-bit data and 500 MOps for 32 bit fixed point data. The GPP will provide a floating point unit, and on-chip memories will be provided for fast data access in addition to external memories such as SDRAM, SRAM, and PROM. The ASIC will feature high radiation hardness (300krad min) and high reliability as well as low power consumption.

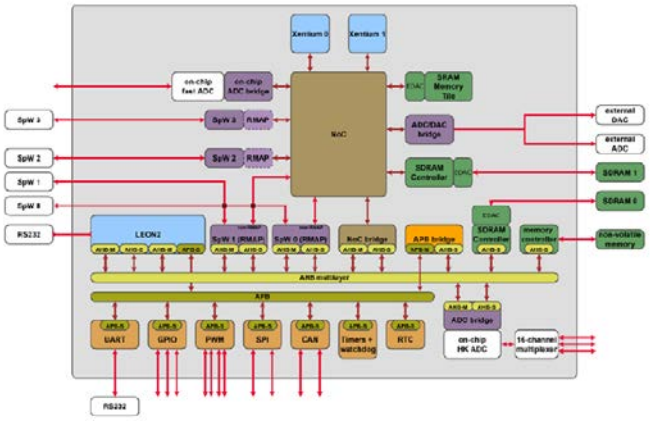

Figure 4: SSDP Baseline Architecture

The final chip architecture will be defined based on the requirements analysis and various trade-offs on memory architecture, adopted interfaces, on-chip memory sizes, package options and other key design factors. The core architecture of 1 LEON GPP with FPU plus 2 fixed point DSP cores will however be maintained.

V. Project Schedule

The development of the SSDP prototypes started in Q2 2014 with the kick-off of the corresponding contract with prime contractor TAS-E (Spain) [7] and key subcontractors IMEC (Belgium) providing the DARE180 technology and RECORE Systems b.v. (NL) as the key digital IP provider. Mixed signal IPs are provided by Arquimea Ingeniera S.L.U. (Spain), and ICsense N.V. (Belgium). The availability of SSDP prototypes and evaluation boards is expected in Q3/Q4 2015. An additional contract for the engineering model (EM) and flight model (FM) development and space qualification will be established in the second half of 2014, with availability of these chips expected in late 2016. The start of the commercialization phase for chips, SDE, and evaluation boards, along with customer support for these products, is expected for the same timeframe.

VI. Conclusions

Based on previous successful technology developments, the development of a successor to the TSC21020 space DSP is now underway. Due to its high performance, high radiation hardness, integrated mixed signal elements and low power it is expected to be suitable for both space applications and specific terrestrial applications in harsh environments. Chips for terrestrial applications and prototyping as well as evaluation boards should be available before 2016. Qualified / validated components for space use are expected by 2017. The progress of the activity will be publicized via relevant ESA webpages and at events announced there [8].

VII. References

[1] R. Trautner, " Next Generation Processor for On-board Payload Data Processing Application – ESA Round Table Synthesis", TEC-EDP/2007.35/RT, 2007. The report is available via [9].

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[9] ESA On-board Data Processing Website, http://www.esa.int/TEC/OBDP/

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