# Scalable Sensor Data Processor: A New Mixed Signal Processor ASIC for Harsh Environments

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**Digital Signal Processors (DSPs) are key components for many data processing applications due to their high speed and low power consumption. This is also true for systems working in harsh environments such as those found in space and in some terrestrial application areas. Due to the specific requirements posed by these environments commercial components can be used only with severe restrictions, or not at all. For these cases specific components based on inherently reliable designs and processes must be used. The Scalable Sensor Data Processor (SSDP) is a DSP component that will meet the requirements of space applications and many specific terrestrial use cases. It is based on a well-tested prototype design and silicon-proven key architectural elements. Key specs include 1 Giga-Ops of processing power, radiation hardened design based on DARE180, up to 1Mrad of Total Ionizing Dose (TID) tolerance, integrated mixed signal elements including ADCs, and low power consumption. The development of this ASIC is ongoing under ESA management with key industrial contractors TASE, IMEC, and RECORE Systems b.v. ASIC prototypes are expected for end 2015. The ASIC will be commercialized as a standard component.**

## SSDP Key Requirements

The most important requirements for the SSDP ASIC can be summarized as follows:

- Processing power > 1000 MOps
- Total Ionizing Dose (TID) tolerance >100krad (Si), with a goal of >300 krad (Si) … 1 Mrad (Si)
- Radiation hardened design (memories, registers, clock trees via EDACs / triplication etc.)
- Industry standard interfaces (SpaceWire, CAN, SPI, GPIO) and space standard peripherals (rad-hard frontend ASICs and detectors, SRAM, NVM, SRAM)
- High Quality Software Development Environment (SDE) and tools, DSP libraries
- High reliability, low power consumption, low mass
- Integration of analogue / mixed signal features, including ADCs and circuitry for housekeeping data acquisition from typical sensors
- No access restrictions for European users (ITAR free)

## A Processor for Harsh Environments

SSDP is primarily developed for space applications. Key features of space qualified integrated circuits include high reliability, radiation hardened design, and large operating temperature range. Therefore, ASICs developed for space applications are typically also compatible with the requirements of some terrestrial applications in harsh environments, such as those in R&D areas like particle physics or fusion research, in nuclear industry (research facilities or nuclear power stations), or in specific application niches (high altitude platforms, borehole technology, etc.). Due to the high cost of development and qualification, space ASICs typically cost significantly more than similar commercial parts. However, the high reliability of these devices may still justify their use also in some terrestrial applications where high reliability and / or availability (minimized downtime) are key to success which may be the case in several of the aforementioned use cases.

The development of the SSDP ASIC therefore also considers terrestrial application cases where possible, and the authors appreciate feedback from potentially interested users.

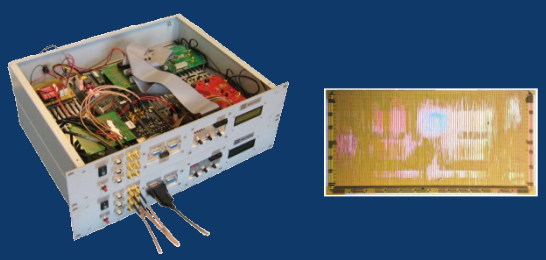

*Fig. 2: SSDP heritage. The development of the ASIC is based on successful prototyping of the architectural design on FPGA, and on validation in DARE180 based silicon of the DSP core and key IP blocks.*

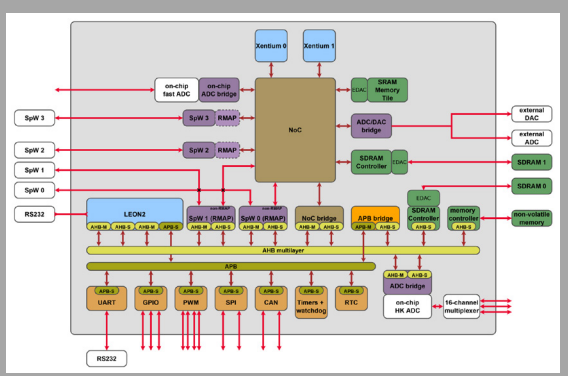


*Fig. 1: SSDP baseline architecture. The GPP and its bus system is shown below, while the NoC and DSP cores as well as fast interfaces are depicted in the upper part of the figure.*

## SSDP Baseline Architecture

The baseline design features an architecture very similar to the FPGA-based MPPB prototype, providing a LEON General Purpose Processor (GPP), 2 VLIW Xentium® DSP cores, high-bandwidth NoC, and space typical / industry standard interfaces (SpaceWire, ADC/DAC, CAN, SPI and others) for the digital part. Like the prototype chip, the ASIC will be based on DARE180 technology which allows incorporation of analogue / mixed signal elements. It is expected that a fast (up to 100 MSps) ADC for instrument data acquisition (15 / 16 bit), a second slow (ca 100 kSps) ADC with multiplexers for housekeeping data acquisition (12 bit), and some housekeeping sensor interfaces will be integrated. Glue-less interfaces to external rad-hard sensors and other chips will be provided. The ASIC will run at a target clock speed of up to 100 MHz, providing in excess of 1 Giga-Ops for 16-bit data and 500 MOps for 32 bit fixed point data. The GPP will provide a IEEE compliant floating point unit, and on-chip memories will be provided for fast local data access in addition to external memories such as SDRAM, SRAM, and PROM. The ASIC will feature high radiation hardness (300krad min) and high reliability by design, as well as low power consumption.

## Summary

**Based on previous successful technology developments, the development of a new, powerful and robust DSP is now underway. Due to its high performance, high radiation hardness, integrated mixed signal elements and low power consumption it is expected to be suitable for both space applications and specific terrestrial applications in harsh environments. Chips for terrestrial applications and prototyping as well as evaluation boards should be available before 2016. Qualified / validated components for space use are expected by 2017. The progress of the activity will be publicized via relevant ESA webpages and at events announced there.**

**ESA On-board Data Processing Website, http://www.esa.int/TEC/OBDP/**

*Credits for figures / images: ESA, RECORE Systems b.v., IMEC*