# Very High Resolution Analog-to-Digital Converter at 1kHz for Space Applications

K. Makris[1], D. Fragopoulos[1], L. Crespy[2], M. Karaolis[1], A. Hachemi[2], O. Dokianaki[1], C. Papadas[2], B. Glass[3]

(1) Integrated Systems Development (ISD S.A.), Athens, GREECE

(2) Advanced System Technology and User Service (ASTUS S.A.), Grenoble, FRANCE

(3) European Space Research and Technology Center (ESA/ESTEC) – Microelectronics Section (TEC-EDM), Noordwijk, THE NETHERLANDS

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# Outline

- Introduction
- Requirements and specifications
- System architecture
- Detailed design
- Design flow
- Radiation hardening
- System modeling
- Layout
- Simulation results
- Conclusions and next steps

# Introduction

- Availability of high resolution hardened ADCs is rather limited
- Certain space instrumentation applications require low frequency and high resolution performance
  - Low frequency, low noise instrumentation and data acquisition
  - High resolution monitoring for housekeeping function implementation
- ADC development supported by an ESA contract

**Commercial High-Rel ADCs**

| Vendor | P/N | Resolution (bits) | architecture | process | power supply | power (mW) | speed |
|---|---|---|---|---|---|---|---|
| Aeroflex | RHD5940 | 14 | SAR | N/A | +5V | N/A | 25ksps |
| MAXIM | MAX1069 | 14 | SAR | BiCMOS | +5V | <5 | 1ksps-58.6ksps |
| ST Microelectronics | RHF1401 | 14 | pipeline | CMOS 0.25um | 2.5V | 85 | 20Msps |
| Datel | ADS937 | 16 | flash | BiCMOS | +/-5V, +/-15V | 1100 | 1Msps |
| Burr-Brown | ADS7809 | 16 | SAR | CMOS | +5V | 150 | 100ksps |
| Maxwell Technologies | 7809LP | 16 | SAR | CMOS | +5V | 150 | 100ksps |
| LT | LTC1604AIG | 16 | SAR | CMOS | +/-5V | 220 | 333ksps |
| ADI | AD977A | 16 | R-2R-ladder/SC | BiCMOS | +5V | 100 | 200ksps |
| MAXIM | MAX1169 | 16 | SAR | BiCMOS | +5V | <5 | 1ksps-58.6ksps |

# Requirements

- ✓ **Rad-hard**
- ✓ **High resolution**
- ✓ **Very low speed**

| | |
|---|---|
| **Resolution** | 24 bit |
| **Analog input bandwidth** | 0.1mHz-1kHz |
| **Effective resolution** | 16+bit @ 1kHz |
| **Dynamic Range** | > 100dB @ 0.1 mHz to 1 kHz |
| **SINAD** | > 100dB @ 0.1 mHz to 1 kHz |
| **Maximum sampling rate** | ≥ 5 kHz |
| **Monotonicity** | Full code range |
| **Power dissipation** | < 70 mW |
| **LET for SEL immunity** | ≥ 70 MeV/mg/cm$^{-2}$ |
| **SEU immunity** | Protection of critical memory cells |
| **SET immunity** | Protection of the digital part |
| **TID tolerance** | ≥100 krad |
| **Temperature range (functional)** | -55 °C < T < 125 °C |
| **Temperature range (full performance)** | 0 °C < T < 50 °C |

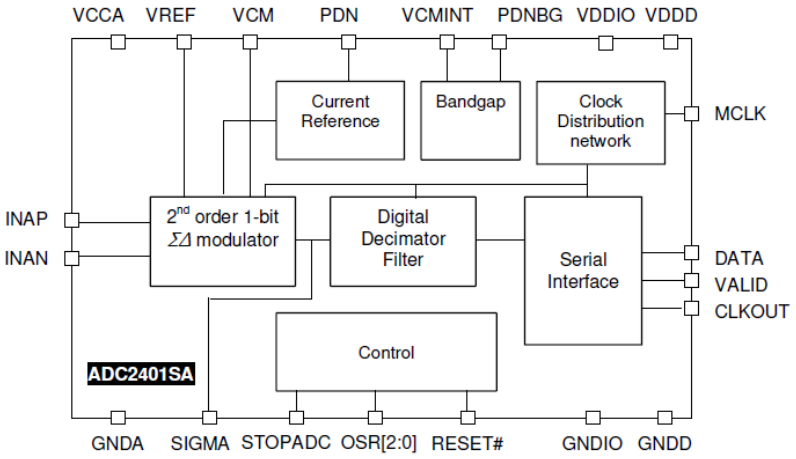
# Features

- Single-bit (inherently linear) ΣΔ modulator
- Single clock domain
- Very low sampling frequency operation
- Correlated double sampling input stage
- Differential or single-ended voltage drive
- ΣΔ modulator can be combined with external DSP core
- Simple serial output interface
- Selectable oversampling ratios allow sampling rates up to **96kSa/s**
- Analog bandwidth from **DC to 16kHz**
- 1.8V/3.3Vpower supplies (3.3V I/O)
- Embedded or external voltage reference
- Radiation hardened against SEE and TID

**Available in two versions**

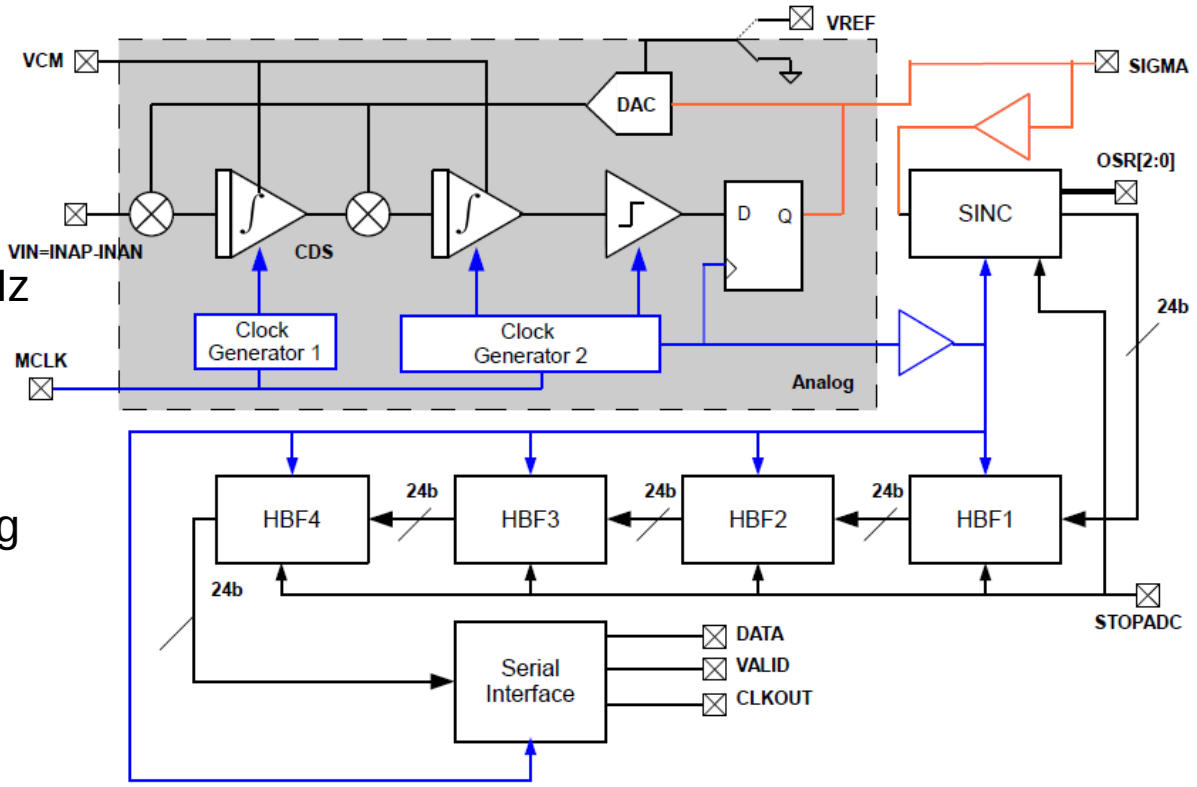
- **ADC2401S**: stand-alone packaged version with serial output interface
- **ADC2401E**: IP macro version featuring parallel output interface for embedding into larger SoCs

- **Technology**:
  **Atmel ATMX150RHA 0.15µm CMOS on SOI**
  - **5 metals, 1 poly**
  - **Fully SPICE modeled and characterized devices**
  - **Rad-hard proven logic**
  - **DTI option, annular devices, HV…**



# System overview

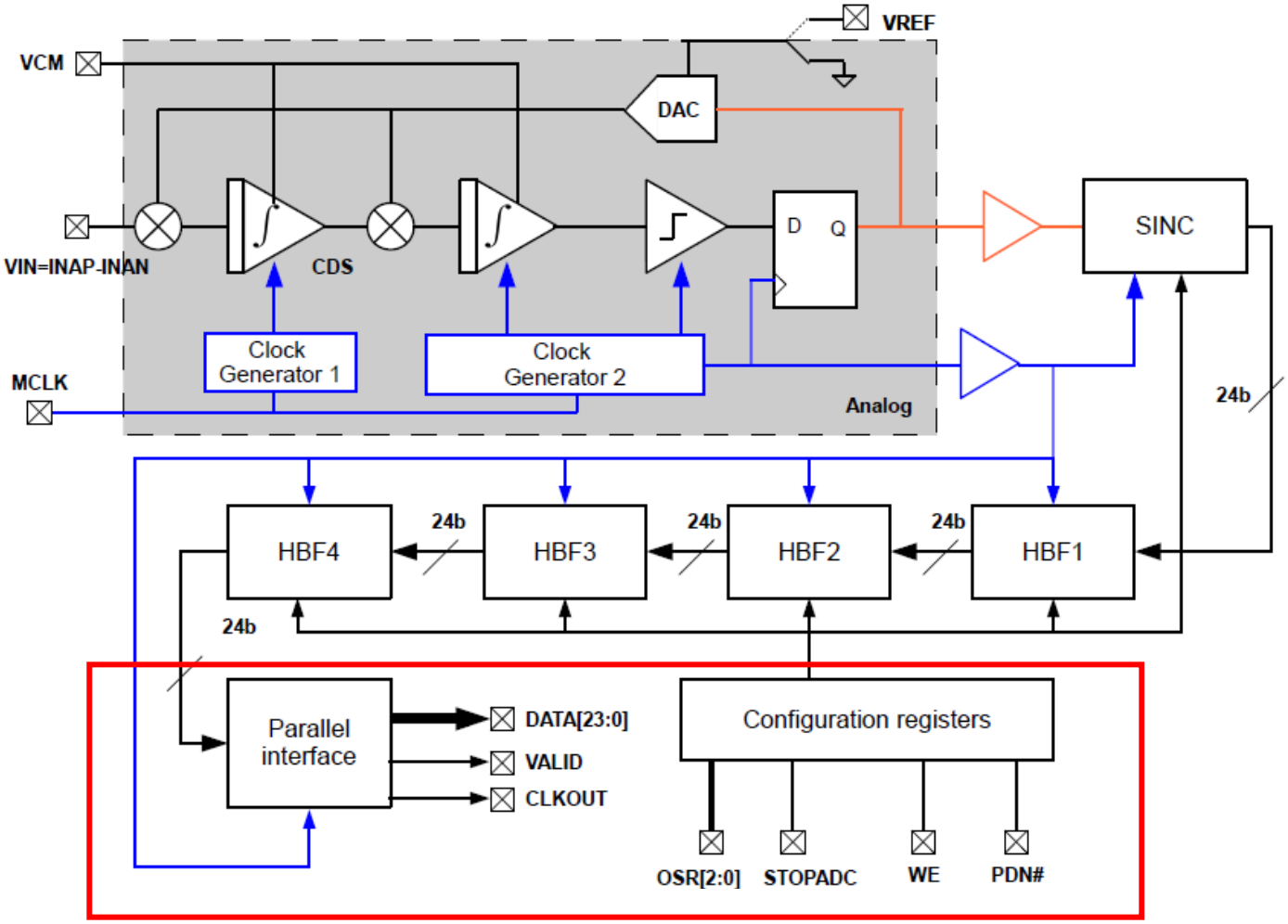
- Discrete time (switched capacitor), 2nd order ΣΔ modulator architecture
- 1 bit internal quantizer
- Single global clock @ 6MHz
- Programmable oversampling ratio: **64x – 1024x**
- Correlated double sampling
- Embedded clock phase generators




| SNR (dB) | BW (kHz) | OSR | ENOB |
|---|---|---|---|
| 125 | 1 | 1024x | 20 |
| 110 | 2 | 512x | 18 |
| 95 | 4 | 256x | 15,4 |
| 80 | 8 | 128x | 13 |
| 65 | 16 | 64x | 10,8 |

➔ Highly scalable architecture

# Embedded IP version

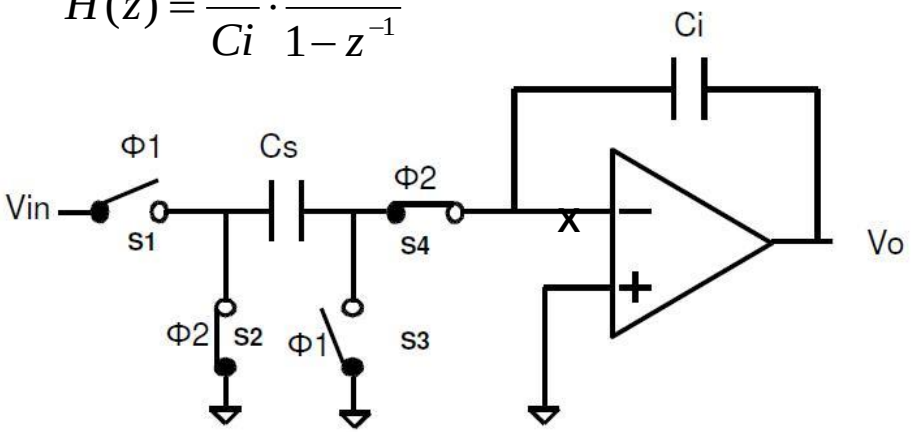


# Why discrete time?

| | Discrete time (DT) | Continuous time (CT) |
|---|---|---|
| Signal bandwidth | Low-medium | Medium – high |
| Application of noise reduction techniques | Easy | More complex |
| Clock jitter sensitivity | Low | High |
| Anti-aliasing filter | Required | Inherent present |
| Process robustness | High | Low |
| Loop filter scalability | Yes | No |

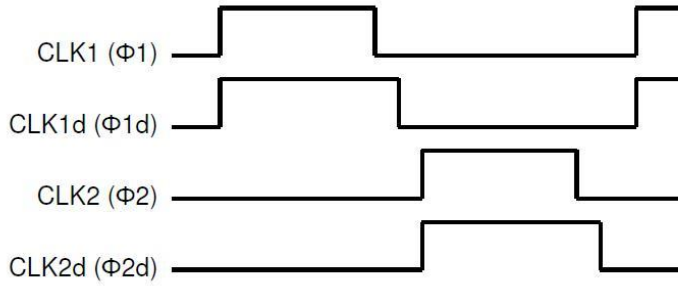
# Stray insensitive SC integrator

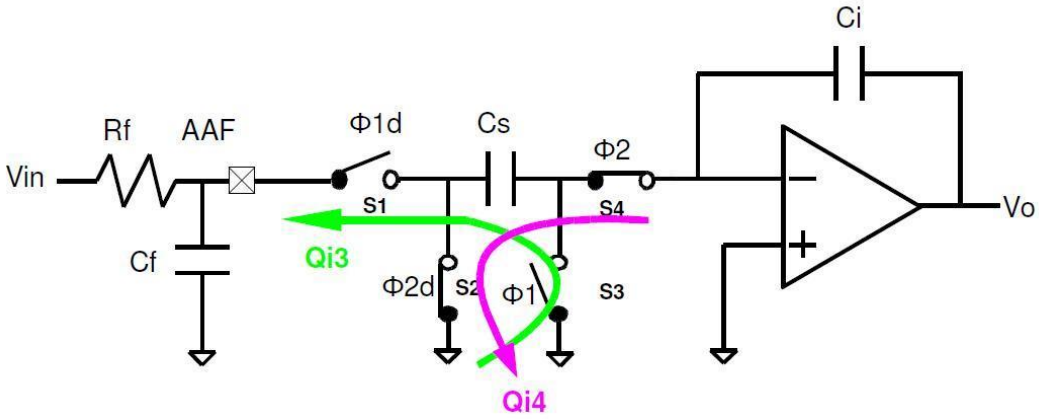
$$H(z) = \frac{Cs}{Ci} \cdot \frac{z^{-1/2}}{1 - z^{-1}}$$




**4-phase non-overlap clock** *[Haigh, Singh ISCAS83]*

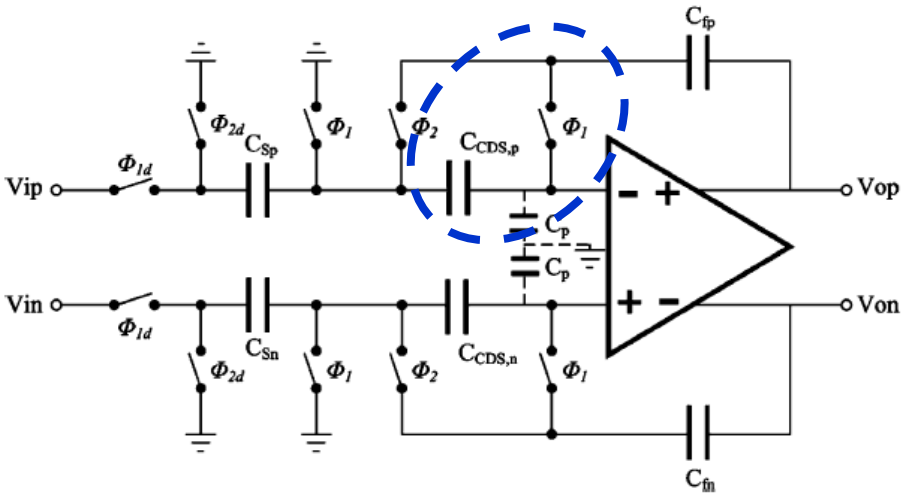
- **Non-inverting SC integrator topology**
- **4-phase non-overlapping clock minimized charge injection in MOS switches**
- **Operation**
  - **Φ1 → sampling mode**
  - **Φ2 → integration mode**
- **Stray insensitive to voltage depended junction capacitance of S3 and S4 (node X)**



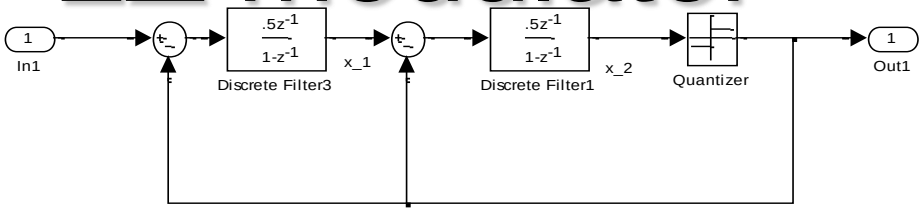
# Correlated Double Sampling

- Reduces 1/f noise
- Reduces offset (AZ)
- Amp noise and noise are sampled twice in each clock period
- Does not limit amplifier bandwidth
- Lowers the effect of finite amplifier gain
- Requires non-overlapping clocks
- Requires 2 additional capacitors and switches



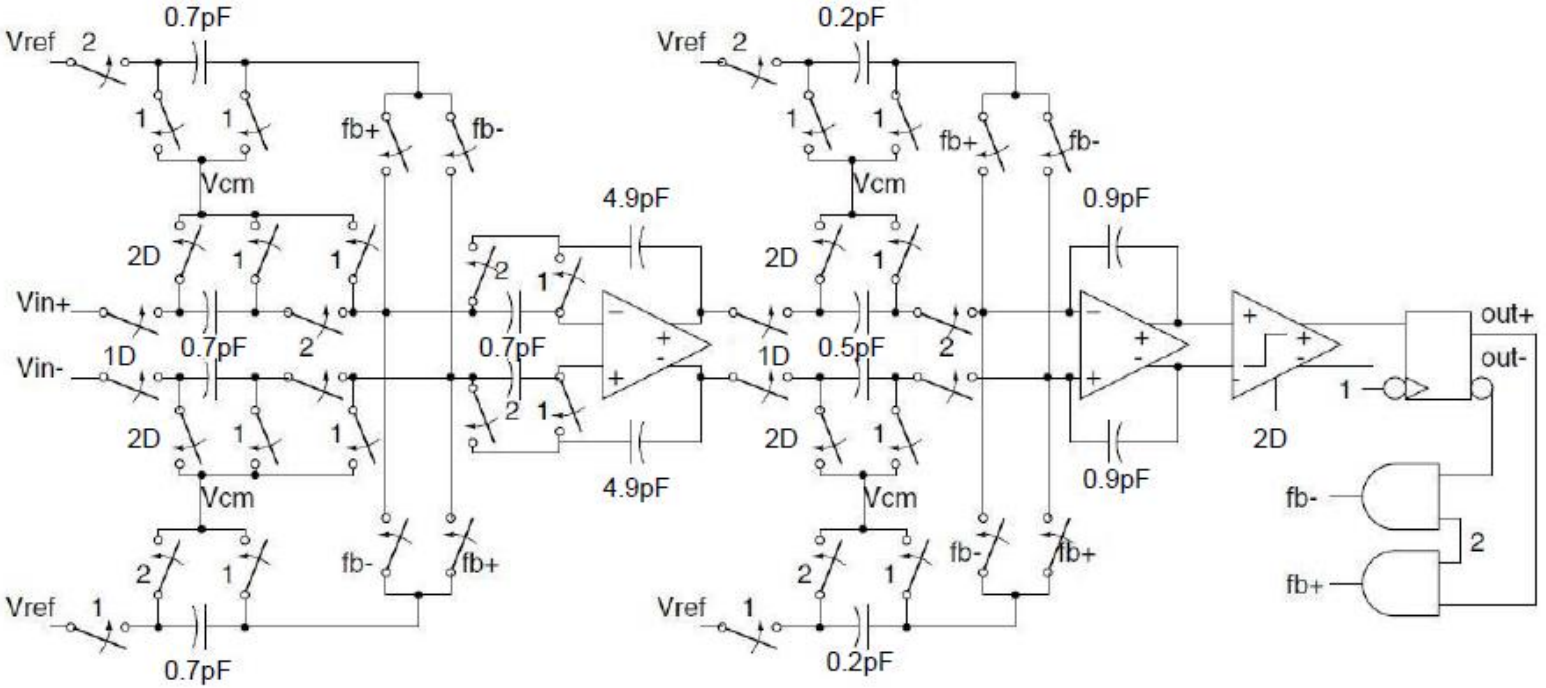

*[C.Enz, G. Temes, 'Circuit Techniques for Reducing the Effects of Op-Amp imperfections', 1996]*

# ΣΔ modulator



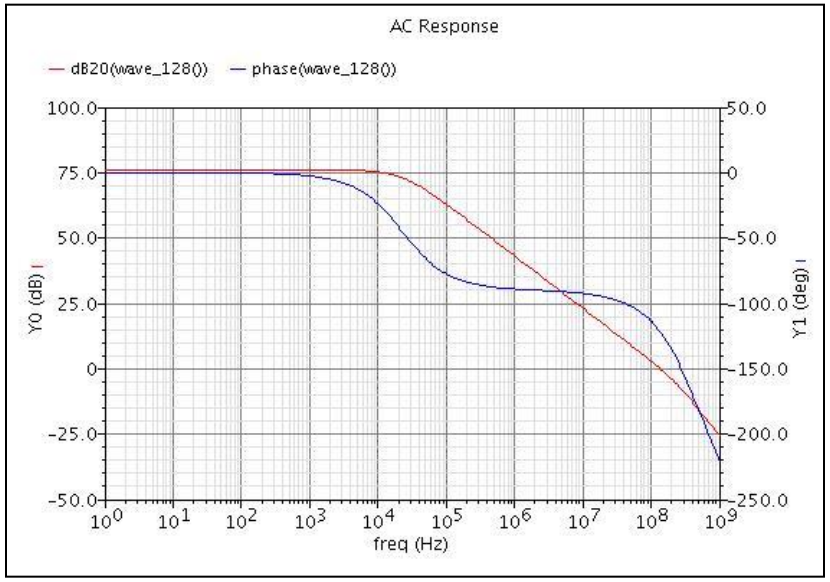

- 1-bit quantizer
- Two fully differential OTAs
- Pass gates as analog switches
- Single-ended Vref input
- 1-bit feedback DAC

Model introduced by *[Norsworthy S.R., R. Schreier, G.C. Temes, 1997]*

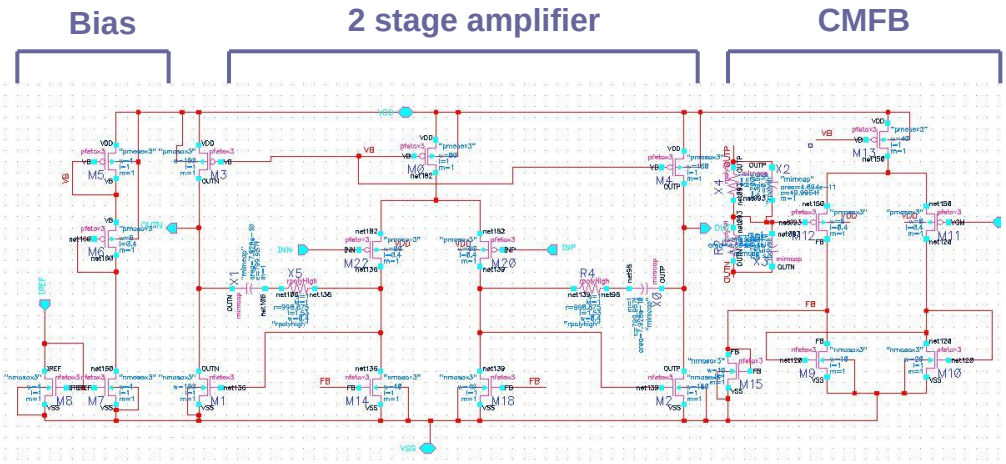


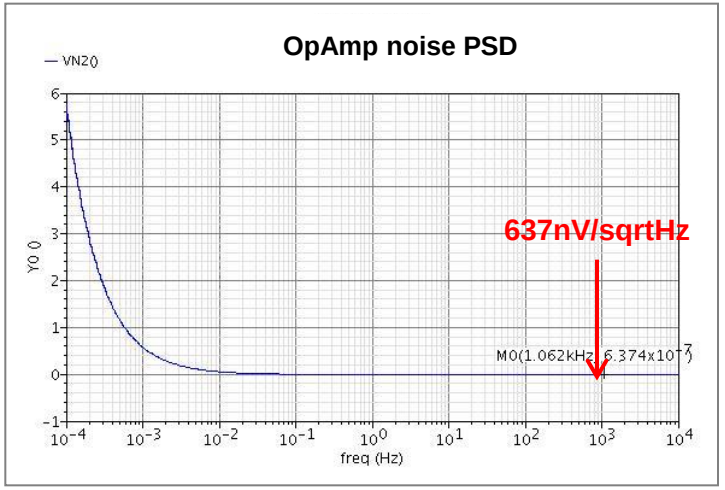

architecture based on *[Nieminen T. and Halonen K, NORCHIP 2010]*

# OTA specifications

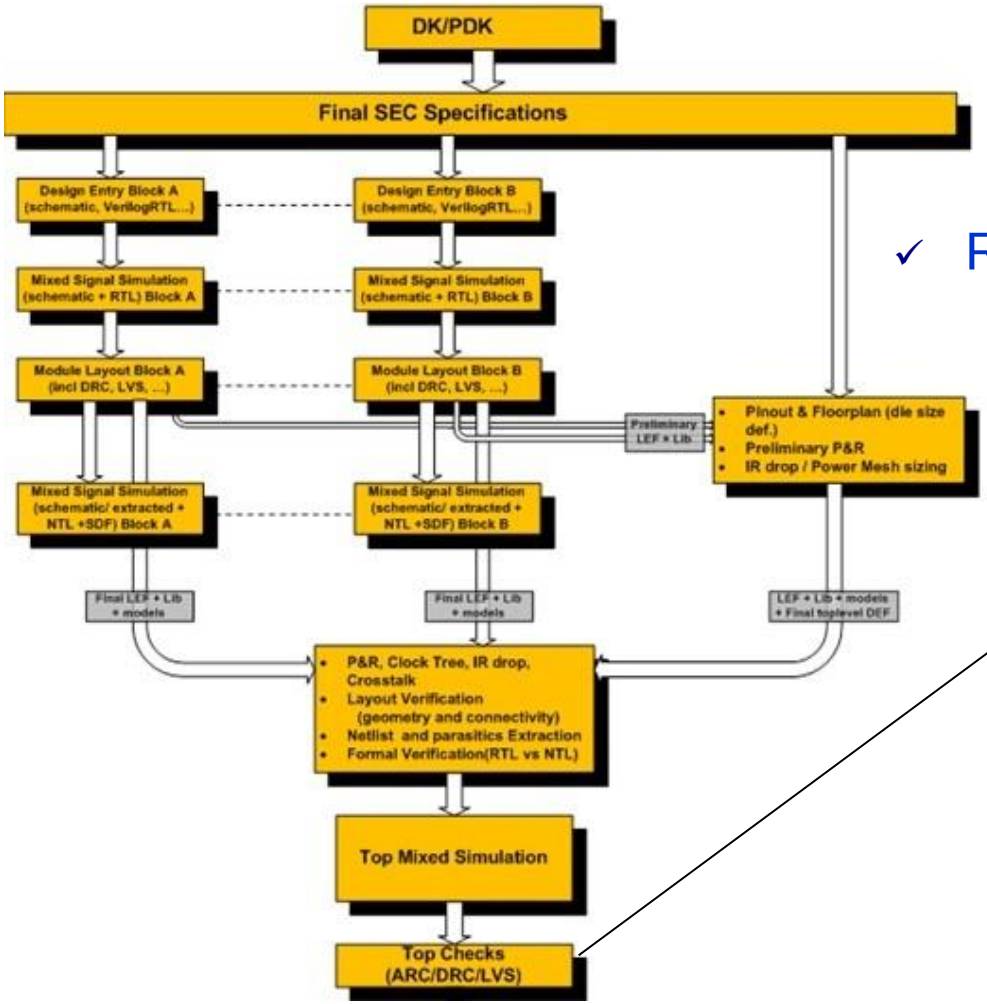



| | |
|---|---|
| Current consumption | 610 uA |
| Open-loop gain | 76.7 dB |
| Phase margin | 58 Deg. |
| Gain margin | -15.5 dB |
| Bandwidth -3dB | 22.3 kHz |
| GPBW | 146 MHz |
| Slew-rate | 225 V/us |
| Common mode output | 1.65 V |
| Current mode input range | 0.35 – 2.95 V |
| Noise @ 1kHz | 637nV/Hz |



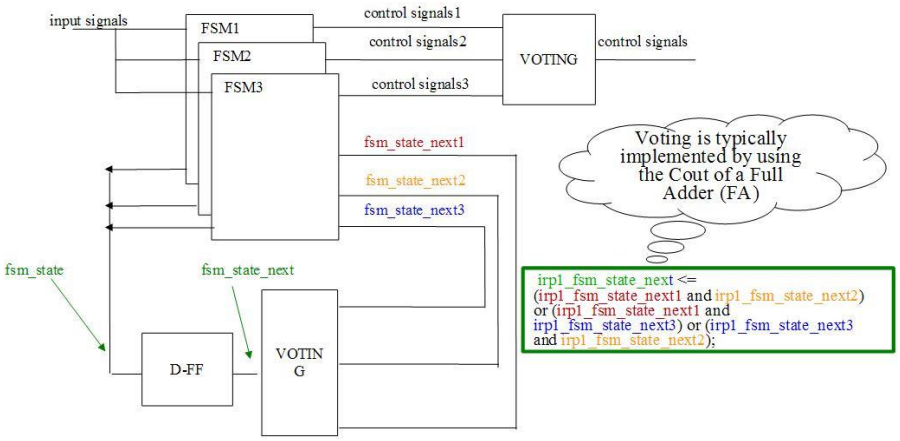
# at77k PDK flow

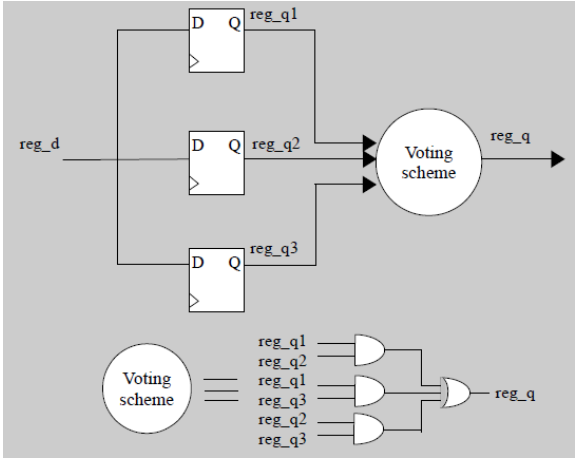



- ✓ Rigorous and consistent AMS flow

# Radiation hardening: digital part

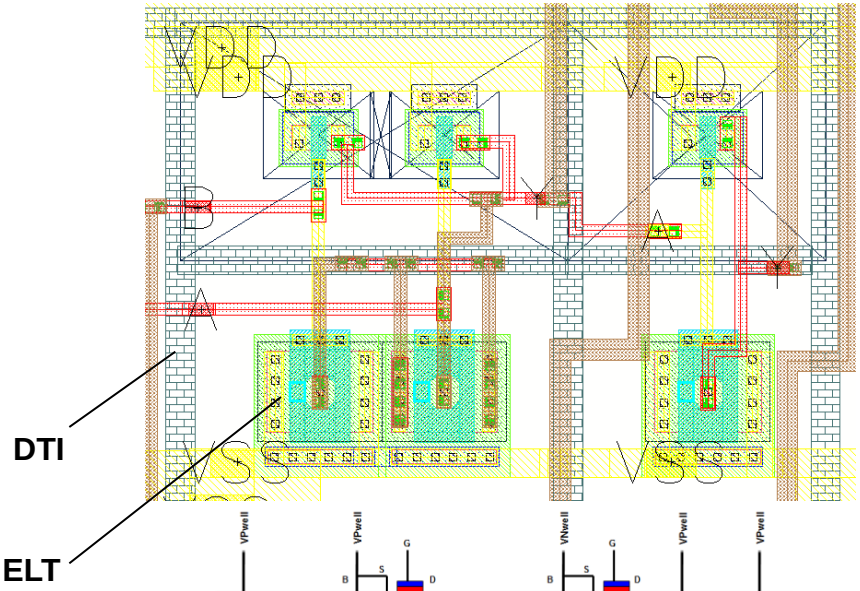
- Triple Modular Redundancy (TMR) with voting scheme
- Each flip-flop is triplicated and a voting mechanism passes the majority result
- Proven fault tolerance technique highly effective in masking random errors (SEE)
- Synchronous reset
- Rad-hard proven cells (at77k PDK libraries)



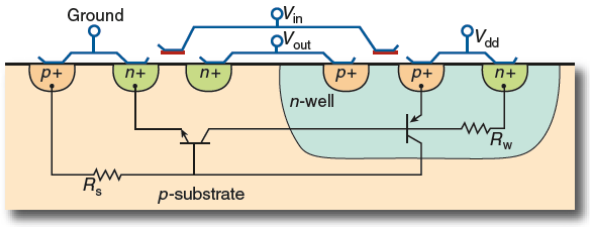
# Radiation hardening: analog part

- Deep Trench Isolation (DTI) option cuts away the parasitic structures between PMOS and NMOS that may trigger SEL
- All NMOS transistors are of enclosed layout type (ELT) which greatly improve analog degradation due to TID effects (overconsumption due to severe leakage currents at edge formed parasitic channels)
- Relaxed layout rules





- Radiation induced charges are trapped in the oxides or at Si interface.
- Overconsumption due to severe leakage currents at edge formed parasitic channels may lead to total loss of circuit functionality.

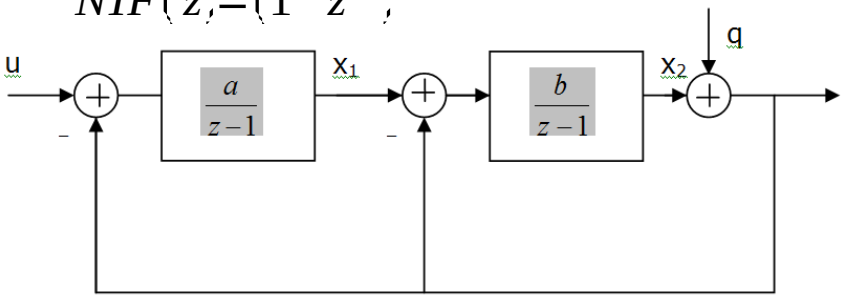



*[fig: R. Mauerer, et.all, 2008]*

# System modeling

1. SNR vs amplitude for various 1st integrator gains *[Schreier, R., 2011, 'Delta Sigma Toolbox for Matlab]*.
2. Root locus of the modulator poles for *a*=0.45 and variable 2nd integrator gain *b* (0, 2.58)
3. Theoretical SQNR 140dB for OSR 2048x and 125dB for 1024x (375Hz sine input at 0.6 FS)

$$NTF(z) = (1 - z^{-1})^2$$

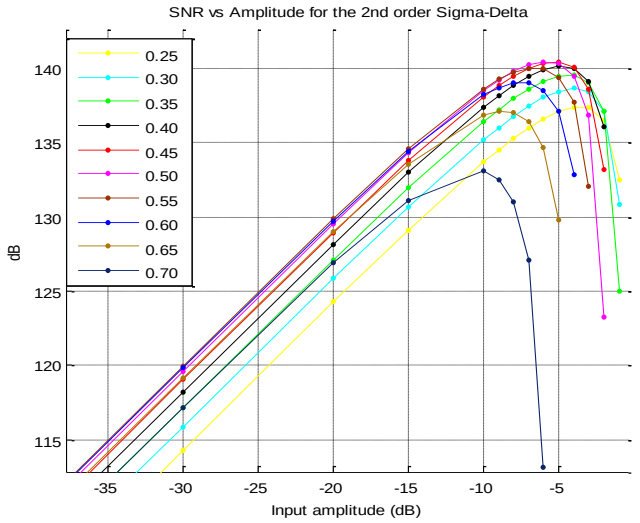



**Linearized model of the ΣΔ modulator**

$$C_{min} = \frac{8kT\,SNR^2}{3V_{DD}^2 OSR}$$ *[R. Schreier, G.C. Temes, 2005]*

- Actual Cs = 0.7pF → SNR 119dB

1

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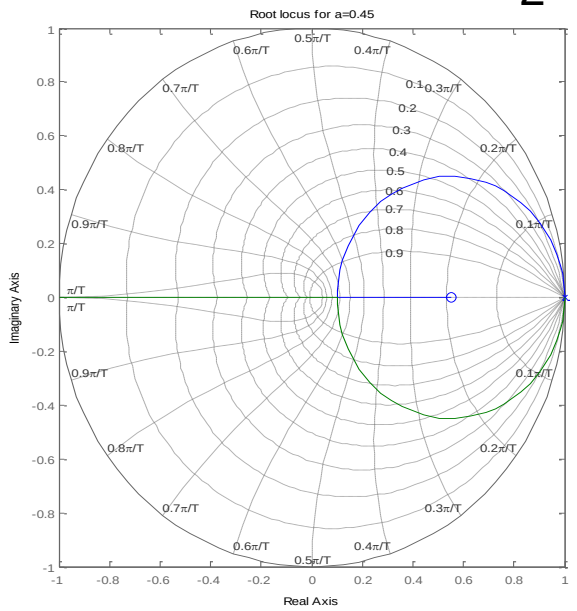
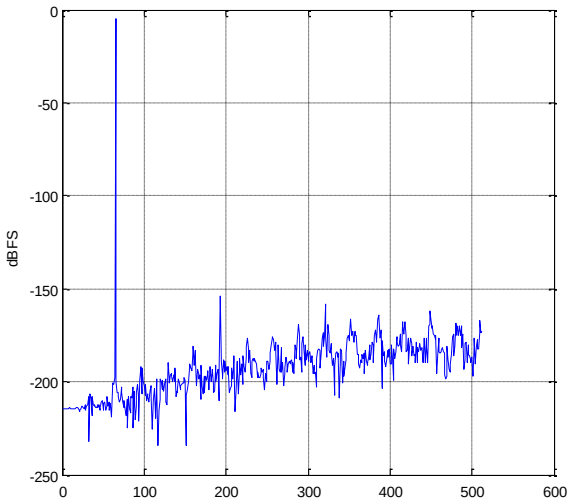
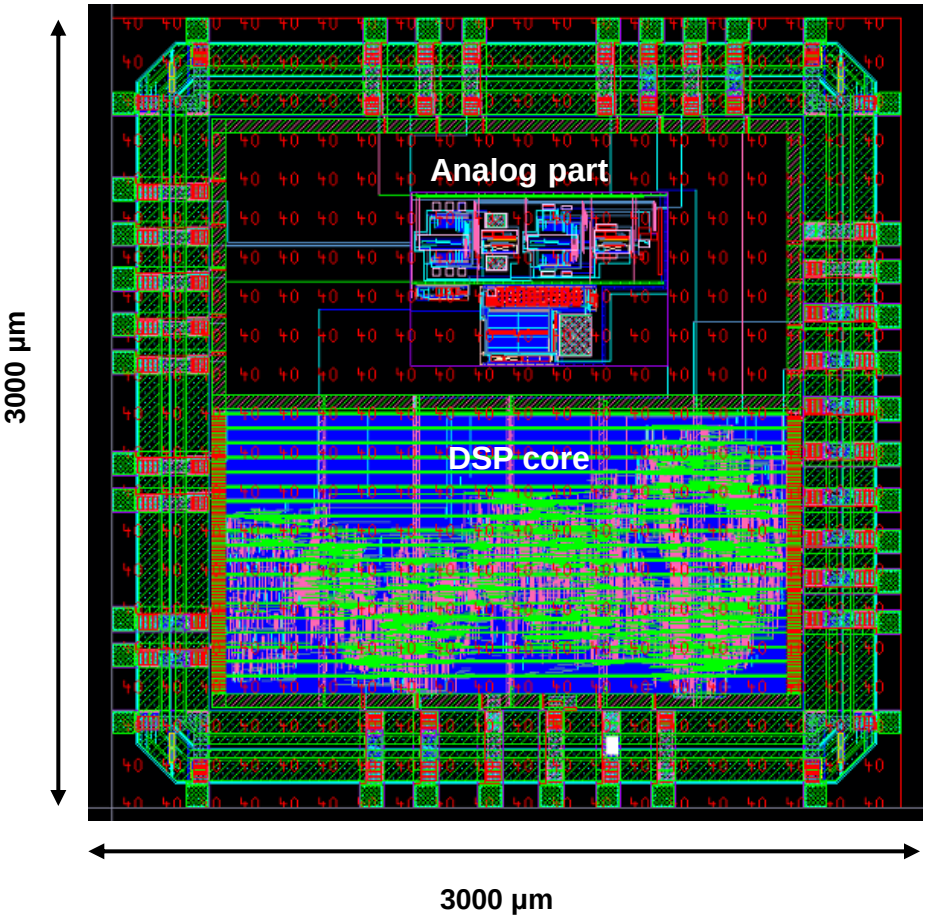
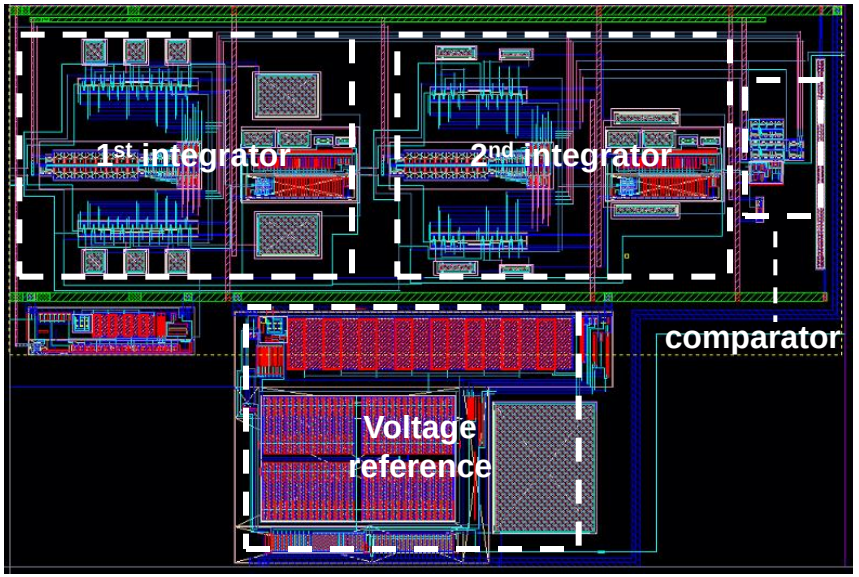



3



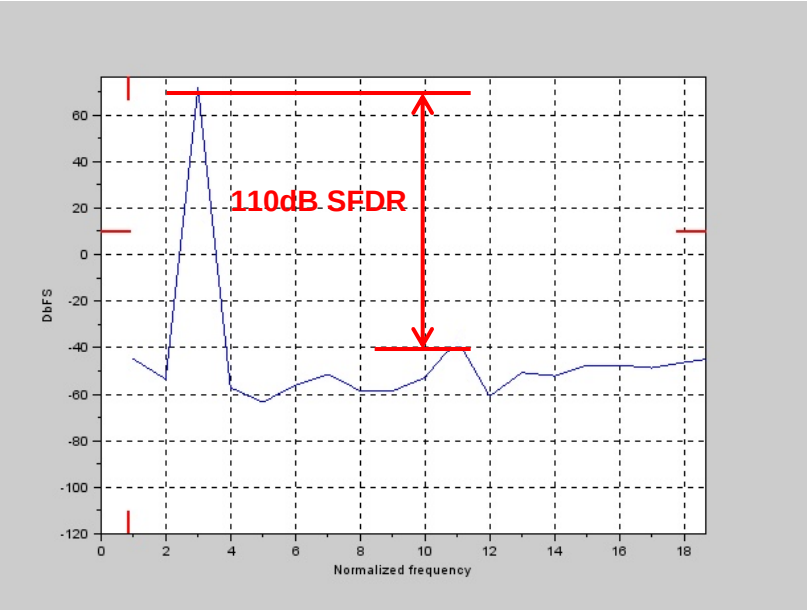
# Floorplan & layout

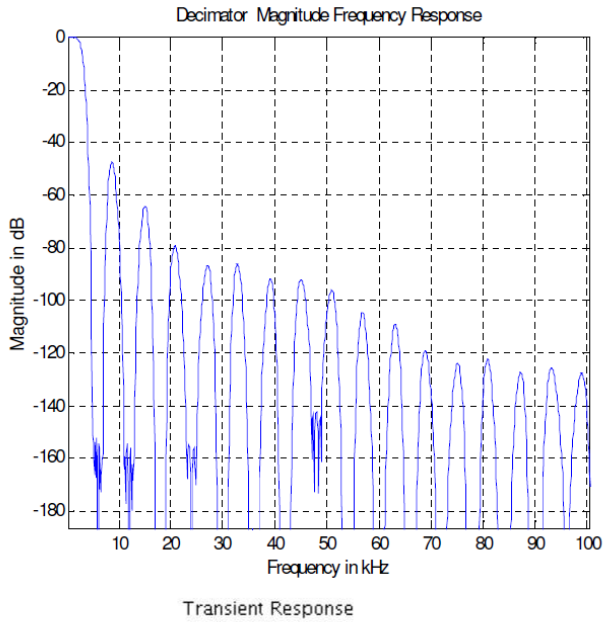


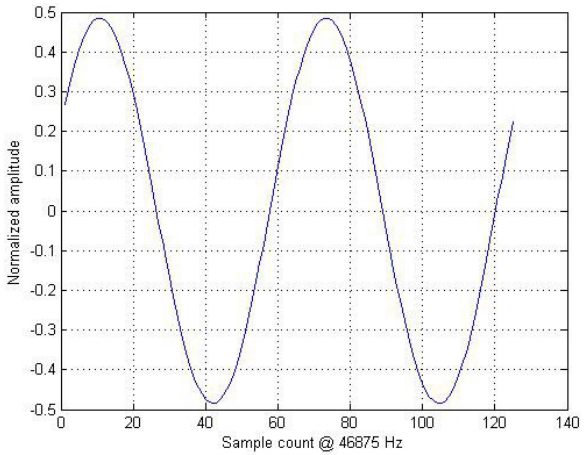
# Simulation results

**FFT sine 750Hz 0dBFS differential input (extracted layout) @ 25°C**



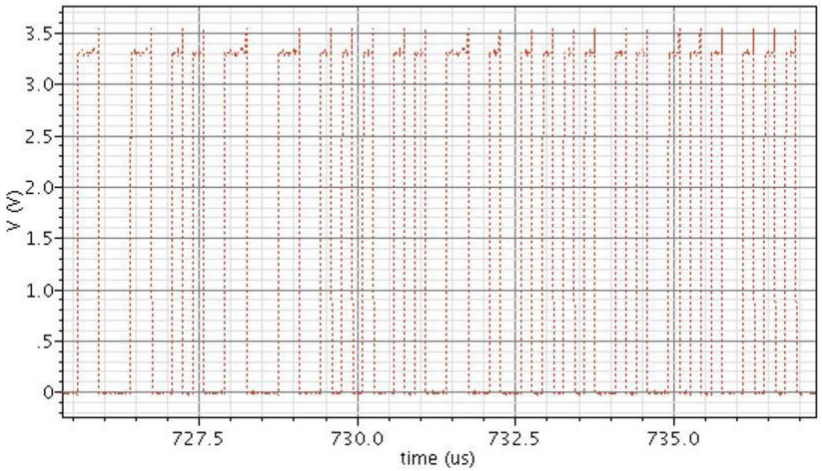




**Reconstructed sine wave at the output of the decimator**




Transient Response

**/OUTPΣΔ modulated output sine 750Hz 3.2Vpp differential**



# Conclusions and next steps

- ENOB of 18bit simulated
- Layout challenging due to increased OSR and precise timing requirements
- Full performance validation in Si will follow
- Full radiation evaluation of prototypes (heavy ions, TID)


## Acknowledgments

We would like to thank Mr. **Michel Porcher** and Dr. **François Braud** of Atmel S.A.S for their continuous support

# Thank you for your attention!

## Questions?